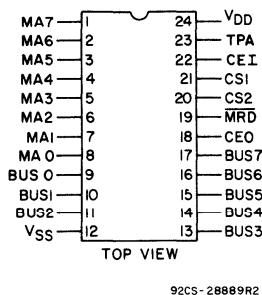


# CDP1833, CDP1833C, CDP1833BC



## CMOS 1024-Word x 8-Bit Static Read-Only Memory

### Features:

- CDP1833BC is compatible with the CDP1802BC 5 MHz microprocessor
- On-chip address latch
- Interfaces with CDP1800-series microprocessors without additional components
- Optional programmable location within 64K memory space
- Three-state outputs

### TERMINAL ASSIGNMENT

The RCA-CDP1833, CDP1833C, and CDP1833BC are static 8192-bit mask-programmable CMOS read-only memories organized as 1024-words x 8 bits and are completely static; no clocks are required. They will directly interface with the CDP1800-series microprocessors without additional components.

The CDP1833, CDP1833C, and CDP1833BC respond to a 16-bit address multiplexed on 8 address lines. Address latches are provided on-chip to store the 8 most significant bits of the 16-bit address. By mask option, this ROM can be programmed to operate in any 1024-word block within 64K memory space. The polarity of the high-address strobe (TPA), CEI, CS1, and CS2 are user mask-programmable.

The Chip-Enable output signal (CEO) is "high" when the device is selected. Terminals CEO and CEI can be

connected in a daisy chain to control selection of RAM memory in a microprocessor system without additional components.

The CDP1833C and CDP1833BC are functionally identical to the CDP1833. The CDP1833 has a recommended operating voltage range of 4 to 10.5 volts, and the CDP1833C and CDP1833BC have a recommended operating voltage range of 4 to 6.5 volts. The CDP1833BC is designed to interface with the CDP1802BC microprocessor.

The CDP1833, CDP1833C, and CDP1833BC are supplied in 24-lead hermetic dual-in-line side-braced ceramic package (D suffix) and 24-lead dual-in-line plastic package (E suffix). The CDP1833C is also available in chip form (H suffix).

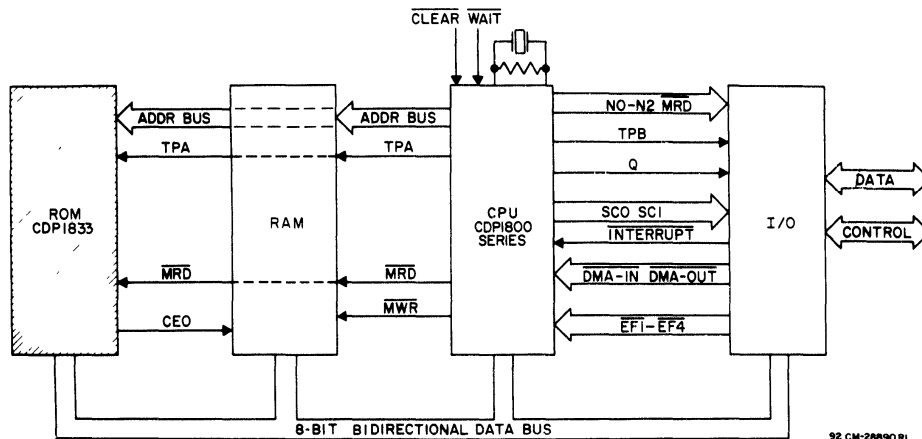


Fig. 1 - Typical CDP1800 Series microprocessor system.

# CDP1833, CDP1833C, CDP1833BC

**MAXIMUM RATINGS, Absolute-Maximum Values:**

DC SUPPLY-VOLTAGE RANGE, (V<sub>DD</sub>)  
(Voltage referenced to V<sub>SS</sub> terminal)

CDP1833 ..... -0.5 to +11 V  
CDP1833C, CDP1833BC ..... -0.5 to +7 V

INPUT VOLTAGE RANGE, ALL INPUTS ..... -0.5 to V<sub>DD</sub>+0.5 V

DC INPUT CURRENT, ANY ONE INPUT ..... ±10 mA

POWER DISSIPATION PER PACKAGE (P<sub>d</sub>):

For T<sub>A</sub> = -40 to +60°C (PACKAGE TYPE E) ..... 500 mW  
For T<sub>A</sub> = +60 to +85°C (PACKAGE TYPE E) ..... Derate Linearly at 12 mW/°C to 200 mW  
For T<sub>A</sub> = -55 to +100°C (PACKAGE TYPE D) ..... 500 mW  
For T<sub>A</sub> = +100 to 125°C (PACKAGE TYPE D) ..... Derate Linearly at 12 mW/°C to 200 mW

DEVICE DISSIPATION PER OUTPUT TRANSISTOR

For T<sub>A</sub> = FULL PACKAGE-TEMPERATURE RANGE (All Packages) ..... 100 mW

OPERATING-TEMPERATURE RANGE (T<sub>A</sub>):

PACKAGE TYPE D ..... -55 to +125°C  
PACKAGE TYPE E ..... -40 to +85°C

STORAGE TEMPERATURE RANGE (T<sub>stg</sub>) ..... -65 to +150°C

LEAD TEMPERATURE (DURING SOLDERING):

At distance 1/16 ± 1/32 in. (1.59 ± 0.79 mm) from case for 10 s max ..... +265°C

**OPERATING CONDITIONS at T<sub>A</sub> = -40° to +85° C**

For maximum reliability, operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS				UNITS
	CDP1833		CDP1833C, CDP1833BC		
	Min.	Max.	Min.	Max.	
DC Operating Voltage Range	4	10.5	4	6.5	V
Input Voltage Range	V <sub>SS</sub>	V <sub>DD</sub>	V <sub>SS</sub>	V <sub>DD</sub>	V

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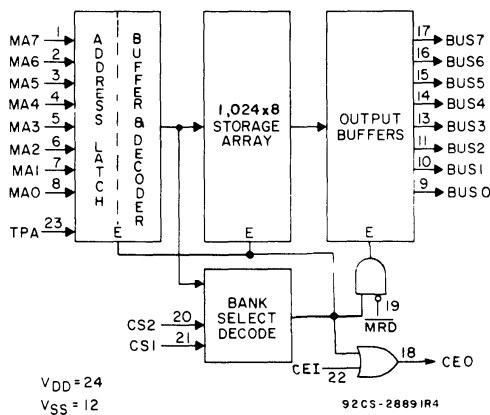


Fig. 2 - Functional diagram.

# CDP1833, CDP1833C, CDP1833BC

STATIC ELECTRICAL CHARACTERISTICS at  $T_A = -40$  to  $+85^\circ\text{C}$ ,  $V_{DD} \pm 5\%$ , Except as noted

CHARACTERISTIC		CONDITIONS			LIMITS						UNITS
		$V_O$ (V)	$V_{IN}$ (V)	$V_{DD}$ (V)	CDP1833			CDP1833C, CDP1833BC			
					Min.	Typ.*	Max.	Min.	Typ.*	Max.	
Quiescent Device Current	$I_{DD}$	—	5	5	—	0.01	50	—	0.02	200	$\mu\text{A}$
		—	10	10	—	1	200	—	—	—	
Output Low Drive (Sink) Current	$I_{OL}$	0.4	0, 5	5	0.8	—	—	0.8	—	—	mA
		0.5	0, 10	10	1.8	—	—	—	—	—	
Output High Drive (Source) Current	$I_{OH}$	4.6	0, 5	5	-0.8	—	—	-0.8	—	—	mA
		9.5	0, 10	10	-1.8	—	—	—	—	—	
Output Voltage Low-Level	$V_{OL}$	—	0, 5	5	—	0	0.1	—	0	0.1	V
		—	0, 10	10	—	0	0.1	—	—	—	
Output Voltage High Level	$V_{OH}$	—	0, 5	5	4.9	5	—	4.9	5	—	V
		—	0, 10	10	9.9	10	—	—	—	—	
Input Low Voltage	$V_{IL}$	0.5, 4.5	—	5	—	—	1.5	—	—	1.5	V
		1, 9	—	10	—	—	3	—	—	—	
Input High Voltage	$V_{IH}$	0.5, 4.5	—	5	3.5	—	—	3.5	—	—	V
		1, 9	—	10	7	—	—	—	—	—	
Input Leakage Current	$I_{IN}$	Any	0, 5	5	—	$\pm 10^{-4}$	$\pm 1$	—	$\pm 10^{-4}$	$\pm 1$	$\mu\text{A}$
		Input	0, 10	10	—	$\pm 10^{-4}$	$\pm 2$	—	—	—	
3-State Output Current	$I_{OUT}$	0, 5	0, 5	5	—	$\pm 10^{-4}$	$\pm 1$	—	$\pm 10^{-4}$	$\pm 1$	$\mu\text{A}$
		0, 10	0, 10	10	—	$\pm 10^{-4}$	$\pm 2$	—	—	—	
Operating Device Current	$I_{DD1}\dagger$	—	0, 5	5	—	7	10	—	7	10	mA
		—	0, 10	10	—	14	20	—	—	—	
Input Capacitance	$C_{IN}$	—	—	—	—	5	7.5	—	5	7.5	pF
Output Capacitance	$C_{OUT}$	—	—	—	—	10	15	—	10	15	

\* Typical values are for  $T_A = 25^\circ\text{C}$  and nominal  $V_{DD}$ .

† Outputs open-circuit; cycle time =  $2.5 \mu\text{s}$

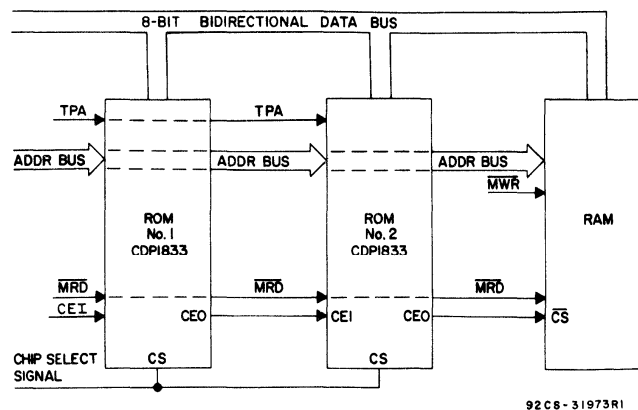


Fig. 3 - Daisy chaining CDP1833's.

"Daisy Chaining" with CEI inputs and CEO outputs is used to avoid memory conflicts between ROM and RAM in a user system. In the above configuration, if ROM #1 was masked-programmed for memory locations 0000-03FF<sub>16</sub> and ROM

#2 masked-programmed for memory locations 0400<sub>16</sub>-07FF<sub>16</sub>, for address from 0000-07FF<sub>16</sub> the RAM would be disabled and the ROM enabled. For locations above 07FF<sub>16</sub> the ROM's would be disabled and the RAM enabled.

**CDP1833, CDP1833C, CDP1833BC**

**DYNAMIC ELECTRICAL CHARACTERISTICS** at  $T_A = -40$  to  $+85^\circ\text{C}$ ,  $V_{DD} \pm 5\%$ ,  
Input  $t_r, t_f = 10\text{ ns}$ ,  $C_L = 50\text{ pF}$ ,  $R_L = 200\text{ k}\Omega$

CHARACTERISTIC	TEST CONDITIONS	LIMITS									UNITS
		CDP1833			CDP1833C			CDP1833BC			
		Min.#	Typ.●	Max.	Min.#	Typ.●	Max.	Min.#	Typ.●	Max.	
Access Time From Address Change $t_{AA}$	5	—	650	775	—	650	775	—	575	700	ns
	10	—	350	425	—	—	—	—	—	—	
Access Time From Chip Select $t_{ACS}$	5	—	500	625	—	500	625	—	475	600	
	10	—	275	310	—	—	—	—	—	—	
Chip Select Delay $t_{CS}$	5	—	250	320	—	250	320	—	250	320	
	10	—	125	180	—	—	—	—	—	—	
Address Setup Time $t_{AS}$	5	75	50	—	75	50	—	75	50	—	
	10	40	25	—	—	—	—	—	—	—	
Address Hold Time $t_{AH}$	5	100	75	—	100	75	—	75	50	—	
	10	50	30	—	—	—	—	—	—	—	
Read Delay $t_{MRD}$	5	—	400	500	—	400	500	—	400	500	
	10	—	200	275	—	—	—	—	—	—	
Chip Enable Output Delay from Address $t_{CA}$	5	—	120	170	—	120	170	—	120	170	
	10	—	70	100	—	—	—	—	—	—	
Bus Contention Delay $t_D$	5	—	220	270	—	220	270	—	220	270	
	10	—	130	150	—	—	—	—	—	—	
TPA Pulse Width $t_{PAW}$	5	200	—	—	200	—	—	175	—	—	
	10	70	—	—	—	—	—	—	—	—	
Chip Enable In to Chip Enable Out Delay $t_{CEO}$	5	—	200	250	—	200	250	—	200	250	
	10	—	100	150	—	—	—	—	—	—	

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# Time required by a limit device to allow for the indicated function.

● Time required by a typical device to allow for the indicated function. Typical values are for  $T_A = 25^\circ\text{C}$  and nominal voltages

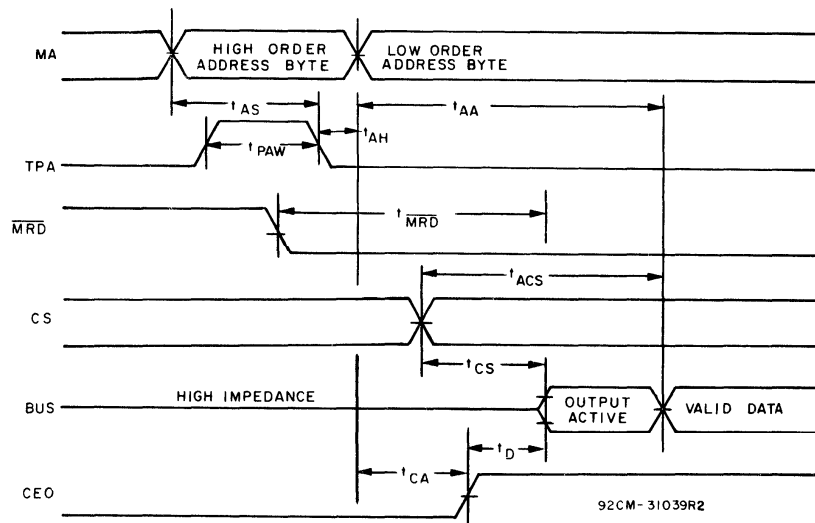


Fig. 4 - Timing waveforms.

## CDP1833, CDP1833C, CDP1833BC

**Note:**

The dynamic characteristics and timing diagrams indicate maximum performance capability of the CDP1833. When used directly with a CDP1800-series microprocessor, timing will be determined by the clock frequency and internal delays of the microprocessor.

The following general timing relationships will hold when the CDP1833 is used with a CDP1800-series microprocessor.

$$t_{AH} = 0.5 t_c$$

$$t_{PAW} = 1 t_c$$

$\overline{MRD}$  occurs one clock period ( $t_c$ ) earlier than the address bits MA0-MA7.

$$\text{where } t_c = \frac{1}{\text{CPU clock frequency}}$$