

Intel[®] 82552V Fast Ethernet PHY

Datasheet

Product Features

General

- Physical layer interface 10BASE-T/ 100BASE-TX IEEE 802.3 compliant.
- IEEE 802.3u Auto-Negotiation support for 10BASE-T/100BASE-TX
- Automatic MDI/MDI-X switch-over
- XOR tree support
- 10BASE-T auto-polarity correction
- Auto-detection of "Unplugged mode".
- 3.3 V device
- Reverse auto negotiation .
- LCI Interface Support
- Loop back support
- PXE Support

Power

- Low Power: 310 mW at fastest speed
 Reduced power in "Unplugged mode"
- Technology
 - 82552V 32 pins, QfN 5 mm x 5 mm package
 - Two Port LED support (Speed, Link and Activity)



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Contents

1.0	Intro	duction1
	1.1	Scope1
	1.2	Overview1
	1.3 1.4	References 2 Product Codes 2
2.0		connects
	2.1	Introduction
	2.2 2.3	JCLK Clock
	2.5	JRSTSYNC
~ ~		
3.0		nterface
	3.1	Pin Assignment53.1.1Signal Type Definitions5
	3.2	Pin Descriptions
4.0		age
	4.1 4.2	Package Type and Epad Size7 Package Electrical and Thermal Characteristics
	4.3	Power and Ground Requirements
	113	4.3.1 Power Delivery
	4.4	Pinouts (Top View, Pins Down)
5.0	Tnitia	alization
5.0	5.1	Power Up Sequence
	5.2	Reset Operation
	_	
6 0	Dow	nr Management and Delivery 15
6.0		Prover Consumption 15
6.0	6.1	Power Consumption
6.0		
	6.1 6.2	Power Consumption15Power Saving Feature156.2.1Low-Power Link Up (LPLU)15
6.0 7.0	6.1 6.2 Elect	Power Consumption 15 Power Saving Feature 15 6.2.1 Low-Power Link Up (LPLU) rical and Timing Specifications 17
	6.1 6.2	Power Consumption15Power Saving Feature156.2.1Low-Power Link Up (LPLU)15rical and Timing Specifications17Introduction17
	6.1 6.2 Elect 7.1	Power Consumption15Power Saving Feature156.2.1Low-Power Link Up (LPLU)1515rical and Timing Specifications17Introduction17Operating Conditions177.2.1Absolute Maximum Operating Conditions17
	6.1 6.2 Elect 7.1	Power Consumption15Power Saving Feature156.2.1Low-Power Link Up (LPLU)rical and Timing Specifications17Introduction17Operating Conditions177.2.1Absolute Maximum Operating Conditions177.2.23.3 V Rail Requirements17
	6.1 6.2 Elect 7.1	Power Consumption15Power Saving Feature156.2.1Low-Power Link Up (LPLU)rical and Timing Specifications17Introduction17Operating Conditions177.2.1Absolute Maximum Operating Conditions177.2.23.3 V Rail Requirements177.2.3DC Characteristics18
	6.1 6.2 Elect 7.1	Power Consumption15Power Saving Feature156.2.1Low-Power Link Up (LPLU)15rical and Timing Specifications17Introduction17Operating Conditions177.2.1Absolute Maximum Operating Conditions177.2.23.3 V Rail Requirements7.2.3DC Characteristics187.2.43.3 V I/O Interfaces DC Characteristics
	6.1 6.2 Elect 7.1	Power Consumption15Power Saving Feature156.2.1 Low-Power Link Up (LPLU)15rical and Timing Specifications17Introduction17Operating Conditions177.2.1 Absolute Maximum Operating Conditions177.2.2 3.3 V Rail Requirements177.2.3 DC Characteristics187.2.4 3.3 V I/O Interfaces DC Characteristics187.2.5 LED DC Characteristics19
	6.1 6.2 Elect 7.1	Power Consumption15Power Saving Feature156.2.1 Low-Power Link Up (LPLU)15rical and Timing Specifications17Introduction17Operating Conditions177.2.1 Absolute Maximum Operating Conditions177.2.2 3.3 V Rail Requirements177.2.3 DC Characteristics187.2.4 3.3 V I/O Interfaces DC Characteristics187.2.5 LED DC Characteristics197.2.6 AC Characteristics19
	6.1 6.2 Elect 7.1	Power Consumption15Power Saving Feature156.2.1 Low-Power Link Up (LPLU)15rical and Timing Specifications17Introduction17Operating Conditions177.2.1 Absolute Maximum Operating Conditions177.2.2 3.3 V Rail Requirements177.2.3 DC Characteristics187.2.4 3.3 V I/O Interfaces DC Characteristics187.2.5 LED DC Characteristics197.2.6 AC Characteristics197.2.7 Reset (JRSTSYNC) Timing Parameters22
	6.1 6.2 Elect 7.1	Power Consumption15Power Saving Feature156.2.1 Low-Power Link Up (LPLU)15rical and Timing Specifications17Introduction17Operating Conditions177.2.1 Absolute Maximum Operating Conditions177.2.2 3.3 V Rail Requirements177.2.3 DC Characteristics187.2.4 3.3 V I/O Interfaces DC Characteristics187.2.5 LED DC Characteristics197.2.6 AC Characteristics197.2.7 Reset (JRSTSYNC) Timing Parameters227.2.8 Crystal Information227.2.9 Crystal Specifications22
	6.1 6.2 Elect 7.1	Power Consumption15Power Saving Feature156.2.1Low-Power Link Up (LPLU)15rical and Timing Specifications17Introduction17Operating Conditions177.2.1Absolute Maximum Operating Conditions177.2.23.3 V Rail Requirements177.2.3DC Characteristics187.2.43.3 V I/O Interfaces DC Characteristics187.2.5LED DC Characteristics197.2.6AC Characteristics197.2.7Reset (JRSTSYNC) Timing Parameters227.2.8Crystal Information22
	6.1 6.2 Elect 7.1 7.2	Power Consumption15Power Saving Feature156.2.1 Low-Power Link Up (LPLU)15rical and Timing Specifications17Introduction17Operating Conditions177.2.1 Absolute Maximum Operating Conditions177.2.2 3.3 V Rail Requirements177.2.3 DC Characteristics187.2.4 3.3 V I/O Interfaces DC Characteristics187.2.5 LED DC Characteristics197.2.6 AC Characteristics197.2.7 Reset (JRSTSYNC) Timing Parameters227.2.8 Crystal Information227.2.9 Crystal Specifications22
7.0	6.1 6.2 Elect 7.1 7.2	Power Consumption15Power Saving Feature156.2.1 Low-Power Link Up (LPLU)15rical and Timing Specifications17Introduction17Operating Conditions177.2.1 Absolute Maximum Operating Conditions177.2.2 3.3 V Rail Requirements177.2.3 DC Characteristics187.2.4 3.3 V I/O Interfaces DC Characteristics187.2.5 LED DC Characteristics197.2.6 AC Characteristics197.2.7 Reset (JRSTSYNC) Timing Parameters227.2.8 Crystal Information227.2.9 Crystal Specifications23
7.0	6.1 6.2 Elect 7.1 7.2 7.3 Prog 8.1	Power Consumption15Power Saving Feature156.2.1 Low-Power Link Up (LPLU)15rical and Timing Specifications17Introduction17Operating Conditions177.2.1 Absolute Maximum Operating Conditions177.2.2 3.3 V Rail Requirements177.2.3 DC Characteristics187.2.4 3.3 V I/O Interfaces DC Characteristics187.2.5 LED DC Characteristics197.2.6 AC Characteristics197.2.7 Reset (JRSTSYNC) Timing Parameters227.2.8 Crystal Information227.2.9 Crystal Specifications22Discrete/Integrated Magnetics Specification23rammers' Visible State25Extended Register description44
7.0	6.1 6.2 Elect 7.1 7.2 7.3 Prog 8.1	Power Consumption15Power Saving Feature156.2.1 Low-Power Link Up (LPLU)15rical and Timing Specifications17Introduction17Operating Conditions177.2.1 Absolute Maximum Operating Conditions177.2.2 3.3 V Rail Requirements177.2.3 DC Characteristics187.2.4 3.3 V I/O Interfaces DC Characteristics187.2.5 LED DC Characteristics197.2.6 AC Characteristics197.2.7 Reset (JRSTSYNC) Timing Parameters227.2.8 Crystal Information227.2.9 Crystal Specifications22Discrete/Integrated Magnetics Specification23rammers' Visible State25
7.0	6.1 6.2 Elect 7.1 7.2 7.3 Progr 8.1 Non-	Power Consumption15Power Saving Feature156.2.1 Low-Power Link Up (LPLU)15rical and Timing Specifications17Introduction17Operating Conditions177.2.1 Absolute Maximum Operating Conditions177.2.2 3.3 V Rail Requirements177.2.3 DC Characteristics187.2.4 3.3 V I/O Interfaces DC Characteristics187.2.5 LED DC Characteristics197.2.6 AC Characteristics197.2.7 Reset (JRSTSYNC) Timing Parameters227.2.8 Crystal Information227.2.9 Crystal Specifications22Discrete/Integrated Magnetics Specification23rammers' Visible State25Extended Register description44Volatile Memory (NVM)51Introduction51EUPDATE Utility51
7.0	6.1 6.2 Elect 7.1 7.2 7.3 Progr 8.1 Non- 9.1	Power Consumption15Power Saving Feature156.2.1 Low-Power Link Up (LPLU)15rical and Timing Specifications17Introduction17Operating Conditions177.2.1 Absolute Maximum Operating Conditions177.2.2 3.3 V Rail Requirements177.2.3 DC Characteristics187.2.4 3.3 V I/O Interfaces DC Characteristics187.2.5 LED DC Characteristics197.2.6 AC Characteristics197.2.7 Reset (JRSTSYNC) Timing Parameters227.2.9 Crystal Specifications22Discrete/Integrated Magnetics Specification23rammers' Visible State25Extended Register description44Volatile Memory (NVM)51Introduction51



11.0	Reference Schematics	55
12.0	Models	59



Revision History

Date	Revision	Description		
September 2008	0.5	Initial public release.		
February 2009Added power delivery diagram. Added reset effects table. Updated Reference Docur list. Removed preliminary oscillator information. Added magnetics specifications. Corrected pinout diagram and pin description table. Updated power consumption to				
April 2009	1.0	Corrected pinout diagram and pin description table. Updated power consumption tab		
May 2000 platform chipset name, Tiger Point. Updated Signal Definition table. Update		Updated power value. Updated RBIAS value. Removed chipset reference and added platform chipset name, Tiger Point. Updated Signal Definition table. Updated mechanical drawing and assembly information. Updated Low-Power Link Up section. Corrected signal name in Figure 8.		
July 2009	1.9	Updated measured power table; removed Intel Confidential designation.		



1.0 Introduction

1.1 Scope

This document describes the external architecture for the 82552V. It's intended to be a reference for software developers of device drivers, board designers, test engineers, or anyone else who might need specific technical or programming information about the 82552V.

1.2 Overview

The Intel[®] 82552V 10/100 Mbps Platform LAN Connect is a highly-integrated device designed for 10 or 100 Mbps Ethernet systems. It is based on the IEEE 10BASE-T and 100BASE-TX standards.

The IEEE 802.3u standard for 100BASE-TX defines networking over two pairs of Category 5 unshielded twisted pair cable or Type 1 shielded twisted pair cable.

The 82552V conforms with the IEEE 802.3u Auto-Negotiation standard and the IEEE 802.3x Full Duplex Flow Control standard. The 82552V also includes a PHY interface compliant to the current platform LAN connect interface.

The 82552V only operates with the ITiger Point chipset that incorporates the MAC. An interface for a Platform Controller Hub (PCH) is also available--contact your Intel representative for more information.

The 82552V is packaged in a small footprint QFN package with 32 pins, 5 mm x 5 mm with 0.5 mm pitch, making it very useful for small form-factor platforms.

The 82552V interfaces with its MAC through the LCI-based interface.

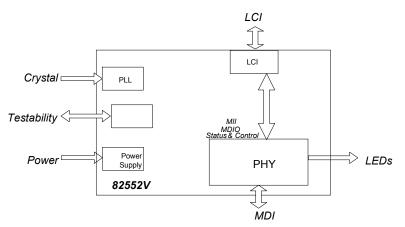


Figure 1. 82552V Block Diagram



1.3 References

- IEEE 802.3 Standard for Local and Metropolitan Area Networks, Institute of Electrical and Electronics Engineers.
- • LAN Connect Interface Specification. Intel Corporation.
- • I/O Control Hub 2, 3, and 4 EEPROM Map and Programming Information. Intel Corporation.
- • I/O Control Hub 5, 6, and 7 EEPROM Map and Programming Information. Intel Corporation

Programming information can be obtained through your local Intel representatives.

1.4 Product Codes

Table 1 lists the product ordering codes for the 82552V Ethernet controller.

Table 1.Product Ordering Code

Device	Product Code
82552V	WG82552V

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2.0 Interconnects

2.1 Introduction

The 82552V implements the LCI interconnect to the MAC:

It is an eight-pin interface that incorporates all MII management functionality. The interface includes reset functionality as well.

2.2 JCLK Clock

The 82552V drives a 50 Mhz clock or a 5 Mhz clock to the MAC depending on the selected technology: 100base-TX or 10Base-T respectively. The 82552V does not stop the LCI clock in any case. During reduced power mode, the 82552V drives a 5 Mhz clock.

2.3 JRSTSYNC

The 82552V filters out any JRSTSYNC pulses with width less than 200 ns to distinguish between a RESET and a SYNC pulse. For resetting the 82552V, the reset should be longer than 500 us.

2.4 XOR Test Interface

Signal	Туре
LED_10_100n	XOR output
LED_ACTn	XOR input
JRXD0	XOR input
JRXD1	XOR input
JRXD2	XOR input
JTXD0	XOR input
JTXD1	XOR input
JTXD2	XOR input
JCLK	XOR input
JRSTSYNC	XOR input
RSVD_IN_1	XOR input
RSVD _IN_32	XOR input



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3.0 Pin Interface

3.1 Pin Assignment

The 82552V is packaged in a 32-pin package, 5×5 mm with a 0.5 mm lead pitch. There are 32 pins on the periphery and a die pad (Exposed Pad*) for ground.

3.1.1 Signal Type Definitions

Signal Type	Definition
I	A standard input-only signal.
0	Totem pole output is a standard active driver.
T/s	Tri-state is a bi-directional, tri-state input/output pin.
S/t/s	Sustained tri-state is an active low tri-state signal owned and driven by one and only one agent at a time. The agent that drives an s/t/s pin low must drive it high for at least one clock before letting it float. A new agent cannot start driving an s/t/s signal any sooner than one clock after the previous owner tri-states it.
O/d	Open drain enables multiple devices to share as a wire-OR.
Analog	Analog input/output signal.
AI	Analog input signal.
AO	Analog output signal.
В	Input bias
Р	Power
PD	Pull down
PU	Pull up
IH	Digital input with hysteresis



3.2 Pin Descriptions

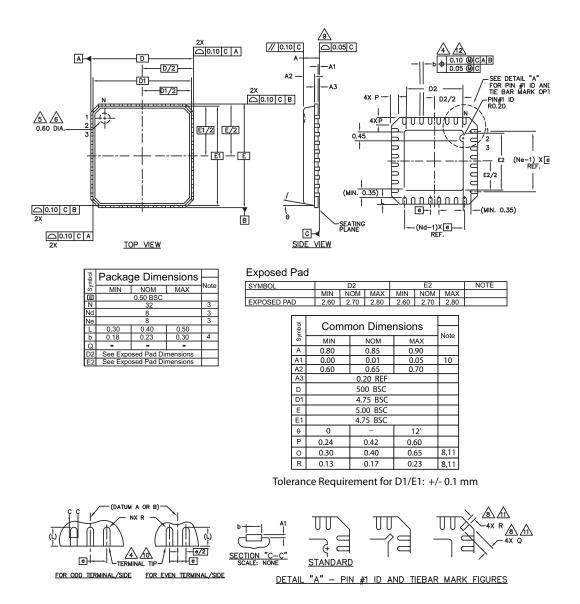
Pin Name	Pin #	Pin type	Description	
VDD2P5_OUT	1	AO	2.5V regulator output. A 1uF plus several 0.1uF cap needed to stabilize the output. It is for analog, digital I/O and the transformer center taps	
VDD3P3_IN	2	Р	3.3 V	
DVDD1P2_3	3	Р	Digital 1.2V	
RSVD_IN_4	4	I, PU (low voltage)	Select either 25 MHz or 48 MHz external clock source. Float=25 MHz, GND=48 MHz	
XTAL_OUT	5	AO	Crystal oscillator output. 27pF to GND. An external clock source with 0-1.2V swing can inject to this pin when crystal is not used	
XTAL_IN	6	AI	Crystal oscillator input, 27pF to GND.	
VDD1P2_OUT	7	Р	1.2V regulator output. Two 0.1uF caps or one 1uF cap needed to stabilize the output.	
RBIAS	8	AO	Connect 2.26 kOhm <u>+</u> 1% to GND	
MDI_PLUS0/ MDI_MINUS0	9, 10	AI, AO	Media Dependent interface 0, terminated with two 49.9 Ω resistors and connect to XFMR	
MDI_PLUS1/ MDI_MINUS1	11, 12	AI, AO	Media Dependent interface 1, terminated with two 49.9 Ω resistors and connect to XFMR	
AVDD2P5_13	13	Р	Analog 2.5 V	
RSVD_IN_14	14	I/O, PU	Reserved input pin. Tie to 3.3V through a 10 kOhm resistor.	
RSVD_IN_15	15	I/O, PU	Reserved input pin. Tie to 3.3V through a 10 kOhm resistor	
TEST_EN	16	I, PD	Test enable.	
LED_10_100#	17	I/O, PU, input is only for test	Parallel LED output for $10/100BASE$ -T, 0 = 100 BT 1 = 10 BT	
LED_ACT#	18	I/O, PU, input is only for test	Parallel LED activity indicator, active low	
JTAG_TDI	19	I/O, PU,	Jtag data in	
JTAG_TMS	20	I/O, PU,	Jtag tms	
JTAG_TDO	21	I/O, PU,	Jtag data out	
JTAG_TCK	22	I/O, PU,	Jtag clk	
DVDD2P5_23	23	Р	Digital I/O 2.5V	
JRXD2	24	I/O, PU, input is only for test	50 Mbps receive out	
JRXD1	25	I/O, PU, input is only for test	50 Mbps receive out	
JRXD0	26	I/O, PU, input is only for test	50 MHz receive out	
JCLK	27	I/O, PU, input is only for test	Clock out	
JTXD2	28	I, PU,	Transmit input	
JTXD1	29	I, PU,	Transmit input	
JTXD0	30	I, PU,	Transmit input	
JRSTSYNC	31	IH, PU,	System reset input	
RSVD _IN_32	32	IH, PU,	Reserved input pin. Tie to 3.3 V through a 10 kOhm resistor	



4.0 Package

4.1 Package Type and Epad Size

The 82552V is a 5 mm x 5 mm, 32-pin QFN package with a pad size of 2.7 mm x 2.7 mm.





4.2 Package Electrical and Thermal Characteristics

Velocity (m/s) Theta Ja (c/w) Theta Jb (c/w) Theta Jc (c/w) Psi jt (c/w) Psi jb (c/w) 0 52.5 33 11.2 0.9 31.7 1 45.9 33 11.2 1.4 31.3 2.5 41.1 33 11.2 1.9 30.9

Max temperature junction is 120 degrees C.

No heat sink is required.

4.3 **Power and Ground Requirements**

The 82552V requires one power supply.

Note: Power delivery can be customized based on a specific OEM platform configuration.

4.3.1 **Power Delivery**

The 82552V operates from a 3.3 V DC external power rail and internally generates the 2.5 V and 1.2 V supplies.



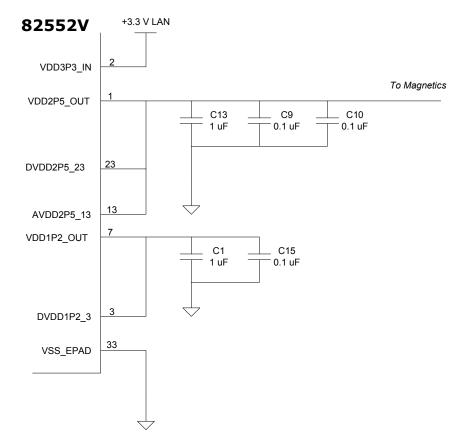
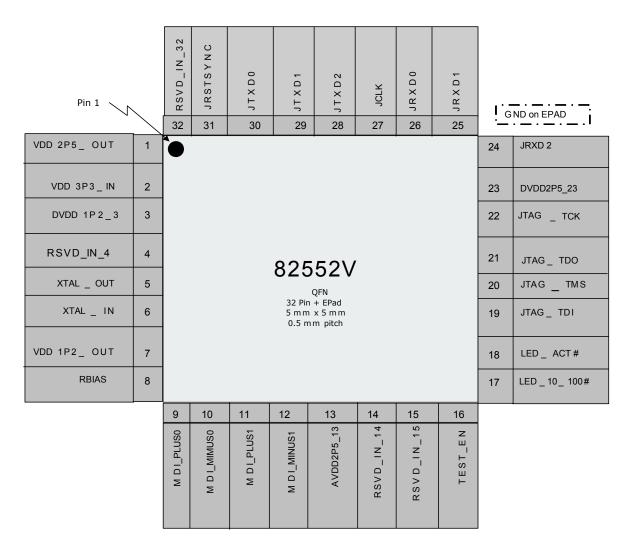


Figure 2. 82552V Power Delivery Diagram



4.4 **Pinouts (Top View, Pins Down)**







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Datasheet—82552V Fast Ethernet PHY





5.0 Initialization

5.1 Power Up Sequence

The 82552V uses a 3.3 V power rail. The rail must meet the LCI power ramp requirements. The following flowchart shows the power up sequence for the 82552V.

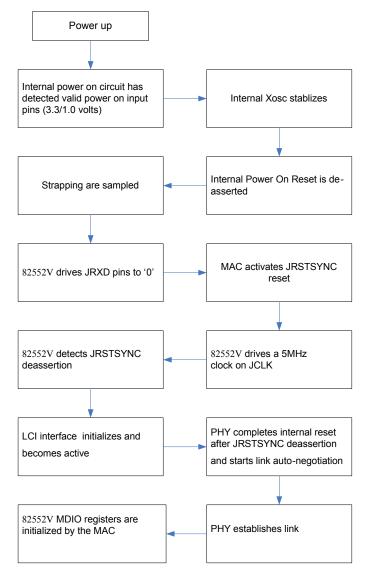


Figure 4. Power Up Sequence Flowchart



5.2 Reset Operation

Three resets are available:

• Internal Power On Reset (POR)--the 82552V has an internal mechanism for sensing the power pins. Until power is up and stable, the 82552V generates an internal active low reset. This reset acts as a master reset for the device.

Strapping values are latched after Internal POR is de-asserted.

- LCI Reset--Reset from JRSTSYNC pin causing complete reset of the 82552V, including the PHY.
- PHY Soft Reset--A PHY reset caused by writing to bit 15 in MDIO register 0.

Setting the bit resets the PHY, but does not reset non-PHY parts.

The effect/impact of these various reset options on these and other registers is listed in the following table. A ($\sqrt{}$) indicates that these areas are affected.

Effects/Sources	PHY Registers and States	Strapping Options
Internal POR	\checkmark	\checkmark
LCI Reset	\checkmark	
PHY Soft Reset	\checkmark	



Power Management and Delivery 6.0

This section describes how power management is implemented in the 82552V.

6.1 **Power Consumption**

The following table lists the measured power:

Measured Power Table 2.

Mode	Description	Intel® 82552V PHY Power + internal regulator (mW)	Intel® NM10 Express Chipset incremental power (mW)	Total Solution Power (mW)
	100 Mbit active	310	86	396
	100 Mbit idle	307	8	315
S0	10 Mbit active	413	17	430
30	10 Mbit idle	59	0	59
	Cable Disconnect	20	0	20
	LAN disable (BIOS or driver)	13	-	13
	WOL disabled	13	-	13
Sx	10 Mbit WOL	59	0	59
	100 Mbit WOL	307	8	315

- The values for power consumption with WOL enabled depend on the link partner autonegotiation or †
- The incremental chipset power is the difference between the chipset power measured at the various LAN connection speeds (active and idle) and the chipset power when the LAN has been disabled via the ++ BIOS.
- +++ To disable WOL, set "Enable PME" to Disabled.

6.2 **Power Saving Feature**

This section provides information about the low power configuration for the 82552V.

6.2.1 Low-Power Link Up (LPLU)

LPLU is a software-based (Windows*-only) feature that instructs the PHY to negotiate to the lowest possible connection speed when going from the S0 state to an Sx state. This power saving feature can be used when power is more important than performance in the Sx state. See the power consumption table for the amount of power drawn in idle when at different connection speeds.

LPLU is enabled for non-D0a states by the Low Power Link Up option in the Advanced driver properties tab.



- Disabled = LPLU is disabled.
- Enabled = LPLU is enabled in all non-D0a states.

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7.0 Electrical and Timing Specifications

7.1 Introduction

This section describes the 82552V's recommended operating conditions, power delivery, DC electrical characteristics, power sequencing and reset requirements, LCI, reference clock, and packaging information.

7.2 Operating Conditions

7.2.1 Absolute Maximum Operating Conditions

- Case Temperature Under Bias
• Storage Temperature
-0.5 V to + 4.6 V Supply Voltage with respect to V_{SS}
• Outputs Voltages0.5 V to + 3.45 V
• Input Voltages1.0 V to + VCC

Note: Case temperature should not exceed junction temperature.

7.2.2 3.3 V Rail Requirements

Title	Description	Min	Мах	Units
Rise Time	Time from 10% to 90% mark	0.1	100	mS
Monotonicity	Voltage dip allowed in ramp	N/A	0	mV
Slope	Ramp rate at any given time between 10% and 90% Min: 0.8*V(min)/Rise time (max) Max: 0.8*V(max)/Rise time (min)	24	28800	V/S
Operational Range	Voltage range for normal operating conditions	3	3.6	V
Ripple	Maximum voltage ripple (peak to peak)	N/A	70	mV
Overshoot	Maximum overshoot allowed	N/A	100	mV



Symbol	Parameter	SI	Specifications		
		Min	Тур	Max	
V1a	High-threshold for 3.3V supply	2.4	2.5	2.6	V
V2a	Low-threshold for 3.3V supply	2.1	2.2	2.3	V

Table 3. Power Detection Threshhold

7.2.3 DC Characteristics

Table 4. General DC Specifications

Symbol	Parameter	Condition	Min	Тур	Мах	Units
V _{CC}	Supply Voltage		3.0	3.3	3.6	V
Т	Temperature	Min - Case Temp; Max - Case Temp	0		85	С
Р	Power Dissipation	10 Mbps, 100 Mbps (transmitter on)		415		mW
		Reduced Power		20		mW

7.2.4 3.3 V I/O Interfaces DC Characteristics

Table 5. 3.3 V I/O Interfaces DC Characteristics

Symbol	Parameter	Condition	Min	Тур	Мах	Units
VCC3p3_IN	I/O Supply Voltage		3.0		3.6	V
Vih	Input High Voltage		0.6Vccj		Vccj+0.5	V
VIL	Input Low Voltage		-0.5		0.3Vccj	V
IIL	Input Leakage Current	0 < Vin < Vccj			±10	μA
Voн	Output High Voltage	lout = -500 μA	.9Vccj			V
Vol	Output Low Voltage	lout = 1500 μA			.1Vccj	V
Cin	Input Pin Capacitance				8	pF



7.2.5 LED DC Characteristics

Table 6. LED DC Characteristics

Symbol	Parameter	Condition	Min	Тур	Мах	Units
V _{OLLED}	Output Low Voltage	Iout = 10 mA			0.7	V
V _{OHLED}	Output High Voltage	Iout = -10 mA	2.4			V

7.2.6 AC Characteristics

7.2.6.1 LCI buffer load

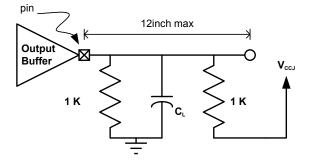


Figure 5. Load for Testing Output Timings

7.2.6.2 LCI Clock and Signals Timings

Table 7.LCI Clock and Signals Timings

	Symbol	Parameter	Condition	Min	Тур	Max	Units	Notes
Τ1	T _{CYC}	JCLK cycle time		20		200	ns	2,6
T2	T _{HIGH}	JCLK high time		8.5			Ns	8
Т3	T _{LOW}	JCLK low time		8.5			ns	8
		JCLK Slew Rate		1.0		4.0	V/ns	3
T4	tvalp	JCLK to valid delay, PHY		2.0		13.0	ns	1,4,5
T5	t _{sup}	PHY setup time to JCLK		5.0			ns	4,5
Т6	thp	PHY signals hold time to JCLK		1.0			ns	4
		Output Signals slew rate		0.25		4.0	V/ns	7
T7	t _{clk-rst}	JCLK stable time before Reset deassertion		0.5			ms	

Notes:

1. Output delays into a capacitive load of 10 pF. For a slow slew rate output driver 0pF load must be used for minimum delays and 50 pF for maximum delays.



- 2. The LCI active frequency is defined by the protocol as high 50 MHz and as low as 5MHz. Dynamic changes of the normal operating frequency are not allowed. Only a change between the normal operating state and a clock stopped state are supported. The clock may only be stopped in a low state. During clock stop, LCI iinterface signals must not be allowed to float.
- 3. Rise and fall times are specified in terms of the edge rate measured in V/ns. This slew rate must be met across the minimum peak-to-peak portion of the clock waveform.
- 4. Input and output timings are measured relative to JCLK timing at the respective component's pin (JCLK is output from PHY and input into MAC).
- 5. In a PHY that is designed for lower than 50 MHz frequency, t_{sup} and maximum t_{VALP} can be extended, by as much as half of the cycle-time difference between that frequency and 50 MHz. This will also allow some added leniency for the system designer as well. Example: max frequency for the designed PHY is 25 MHz. The cycle time difference is 20ns. t_{sup} and maximum t_{VALP} can be extended by 10ns each.
- 6. JCLK must never be stopped while in operation mode. The frequency of JCLK must be stable once initiated during reset.
- 7. Signal slew rates are measured between V_{TL} and V_{TH} .
- 8. V_{TEST} 0.5Vccj

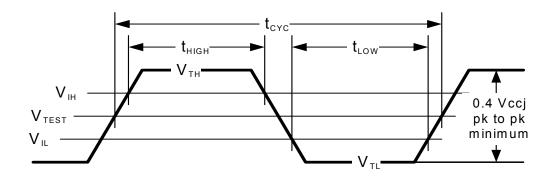


Figure 6. Clock Input Measurement Conditions





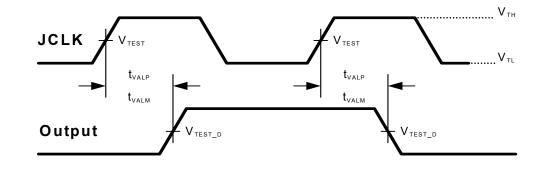


Figure 7. Output Timing Measurement Conditions

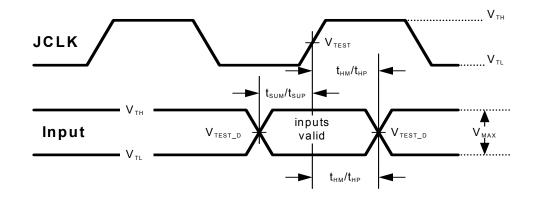
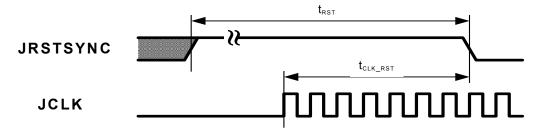


Figure 8. Input Timing Measurement Conditions







7.2.7 Reset (JRSTSYNC) Timing Parameters

Table 8. Reset (JRSTSYNC) Timing Parameters

	Symbol	Parameter	Condition	Min	Тур	Мах	Units
T17	T _{RST_WID}	Reset pulse width		500			μS
T18	T _{POP_RST}	Power Up to falling edge of Reset		1000			μs

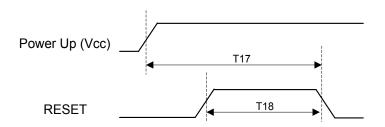


Figure 10. Reset Timing Parameters

7.2.8 Crystal Information

The schematics for the intended crystal design options are shown below:

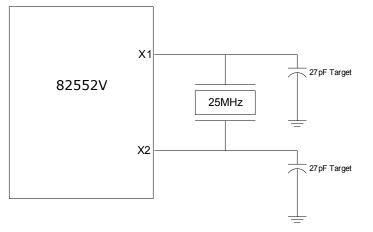


Figure 11. Crystal Connection Diagram

7.2.9 Crystal Specifications

Table 9.Crystal Specifications

Vibrational mode	Fundamental
Nominal frequency	25.000 MHz @ 25 C
Frequency Tolerance	±30ppm
Temperature Stability	±30ppm @ 0 C to 70 C
Calibration mode	Parallel
Crystal Load Capacitance	18 pF
Shunt Capacitance	6 pF maximum



Series Resistance, Rs	50 Ω maximum
Drive Level	200 uW maximum
Aging	± 5.0 ppm per year maximum
Insulation Resistance	500 M $_{\Omega}$ minimum @ DC 100 V

7.3 Discrete/Integrated Magnetics Specification

Table 10. Discrete/Integrated Magnetics Specification

Criteria	Condition	Values (Min/Max)
Voltage	At 50 to 60 Hz for 60 seconds	1500 Vrms (min)
Isolation	For 60 seconds	2250 V dc (min)
Open Circuit Inductance	With 8 mA DC bias at 25 °C	400 μH (min)
(OCL) or OCL (alternate)	With 8 mA DC bias at 0 °C to 70 °C	350 μH (min)
Insertion Loss	100 kHz through 999 kHz 1.0 MHz through 60 MHz 60.1 MHz through 80 MHz 80.1 MHz through 100 MHz 100.1 MHz through 125 MHz	1 dB (max) 0.6 dB (max) 0.8 dB (max) 1.0 dB (max) 2.4 dB (max)
Return Loss	1.0 MHz through 40 MHz 40.1 MHz through 100 MHz When reference impedance si 85 Ω , 100 Ω , and 115 Ω . Note that return loss values might vary with MDI trace lengths. The LAN magnetics might need to be measured in the platform where it is used.	18 dB (min) 12 to 20 * LOG (frequency in MHz / 80) dB (min)
Crosstalk Isolation Discrete Modules	1.0 MHz through 29.9 MHz 30 MHz through 250 MHz 250.1 MHz through 375 MHz	-50.3+(8.8*(freq in MHz / 30)) dB (max) -26-(16.8*(LOG(freq in MHz / 250)))) dB (max) -26 dB (max)
Crosstalk Isolation Integrated Modules	1.0 MHz through 10 MHz 10.1 MHz through 100 MHz 100.1 MHz through 375 MHz	-50.8+(8.8*(freq in MHz / 10)) dB (max) -26-(16.8*(LOG(freq in MHz / 100)))) dB (max) -26 dB (max)
Diff to CMR	1.0 MHz through 29.9 MHz 30 MHz through 500 MHz	-40.2+(5.3*((freq in MHz / 30)) dB (max) -22-(14*(LOG((freq in MHz / 250)))) dB (max)
CM to CMR	1.0 MHz through 270 MHz 270.1 MHz through 300 MHz 300.1 MHz through 500 MHz	-57+(38*((freq in MHz / 270)) dB (max) -17-2*((300-(freq in MHz) / 30) dB (max) -17 dB (max)

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Datasheet—82552V Fast Ethernet PHY





8.0 **Programmers' Visible State**

Table 11.PHY Register Bit Type

Туре	Description
LH	Register field with latching high function. If status is high, then the register is set to a one and remains set until a read operation is performed through the management interface or a reset occurs.
LL	Register field with latching low function. If status is low, then the register is cleared to a zero and remains cleared until a read operation is performed through the management interface or a reset occurs.
Retain	Value written to a register field does take effect without a software reset.
RES	Reserved for future use. All reserved bits are read as zero unless otherwise noted.
RO	Read only
ROC	Read only clear; After read, register field is cleared to zero.
R/W	Read/write
RWC	Read/Write clear on read. All bits are readable and writable. After reset or after the register is read, the register field is cleared to zero.
RWR	Read/Write reset. All bits are readable and writable. After reset the register field is cleared to zero.
RWS	Read/Write set. All bits are readable and writable. After reset the register field is set to a non-zero value specified in the text.
SC	Self-Clear. Writing a one to this register causes the desired function to be immediately executed, then the register field is cleared to zero when the function is complete.
Update	Value written to the register field does not take effect until a software reset is executed. The value can still be read after it is written.
wo	Write only. Reads to this type of register field return undefined data.



Table 12. Base PHY Register Summary

Offset	Name			
0	Control Register			
1	Status Register			
2	PHY identifier			
3	PHY identifier2			
4	Auto negotiation Advertisement Register			
5	Link Partner Ability Register			
6	Auto negotiation Expansion Register			
16	PHY Specific Control Register			
17	PHY Specific Status Register			
18	Interrupt Enable Register			
19	19 Interrupt Status Register			
20	SmartSpeed Control Register			
21	Receive Error Counter Register			
22	Virtual Cable Tester Control Register			
24	LED Control Register			
25	Manual LED Override Register			
28	28 Virtual Cable Tester Status Register			
29	Adresss Port of Extended Register			
30	Data Port of Extended Register			



Bits	Symbol	י	Гуре	Description
15	Decet	Mode HW Rst	R/W 0	PHY Software Reset. Writing a "1" to this bit causes the PHY to be partially reset. This bit is cleared after Write operation. The reset takes effect immediately after the bit is set.
15	Reset	SW Rst	-	1 = PHY reset
			SC	0 =Normal operation
		Mode	R/W	When loopback is activated, the transmitter data presented or MII TXD is looped back to MII RXD internally. Link is broken
14	Loopback	HW Rst	0	when loopback is enabled. 1 = Enable Loopback
		SW Rst	0	0 = Disable Loopback
		Mode	R/W	Upon hardware reset, this bit and 0.6 bit are determined by
13	Speed Selection	HW Rst	See Desc.	anen (bit0.12) and speed_i (phycore interface pin): anen {0.6, 0.13}
10	(LSB)	SW Rst		0 {1'b0, speed_i} 1 2'b01
				(00:10Mbps; 01:100Mbps; 10,11:Reserved)
		Mode	R/W	
12 Auto-negotiation	HW Rst	See Desc.	This bit determined by ANEN_i (phycore interface pin) upon hardware reset.	
	Auto negotiation			1 = Enable Auto-Negotiation Process
		SW Rst		0 = Disable Auto-Negotiation Process
	Mode	R/W	When PHY is switched from power down to normal operation, software reset and Auto-Negotiation Restart are performed	
11	Power Down	HW Rst	0	even bit Reset (0.15) or bit Restart Auto-Negotiation (0.9) is not set. 1 = Power down
		SW Rst	0	0 = Normal operation
		Mode	R/W	
10	Isolate	HW Rst	0	Not implemented. (The GMII/MII/TBI output pins are tri-stated when this bit is set to 1. The GMII/MII/TBI inputs are ignored.
		SW Rst	0	1 = Isolate 0 = Normal operation)
		Mode	R/W,SC	
9 Restart Auto- negotiation	HW Rst	0	Auto-Negotiation automatically restarts after hardware or software reset regardless of whether or not the restart bit (0.9 is set. 1 = Restart Auto-Negotiation Process	
			SW Rst	SC
8 Duple		Mode	RW,SC	Upon hardware reset , this bit depends on duplex_i (phycore interface signal) and anen bit(0.12):
	Duplex Mode	HW Rst	See Desc.	0.12 0.8 0 0
		SW Rst		1 duplex_i 1:Full Duplex

Table 13.Control PHY Register Descriptions (Address Offset = 0x00, or 0d00)



		Mode	R/W	
7 Collision Test	HW Rst	0	Setting this bit to 1 will cause the COL pin to assert whenever the TX_EN pin is asserted. 1 = Enable COL signal test 0 = Disable COL signal test	
		SW Rst	0	
		Mode	R/W	
6	6 Speed Selection (MSB)	HW Rst	See Desc.	See bit 0.13
		SW Rst		
		Mode	RO	
5:0	5:0 Reserved	HW Rst	00000	Will always be 00000.
		SW Rst	00000	



Bits	Symbol	Туре		Description
		Mode	RO	100BASE-T4.
15	100BASE-T4	HW Rst	Always 0	This protocol is not available.
		SW Rst	Always 0	0 = PHY not able to perform 100BASE-T4
		Mode	RO	
14	100BASE-X	HW Rst	Always 1	Capable of 100-Tx Full Duplex operation
	Full-Duplex	SW Rst	Always 1	
		Mode	RO	
13	100BASE-X Half-Duplex	HW Rst	Always 1	Capable of 100-Tx Half Duplex operation
		SW Rst	Always 1	
		Mode	RO	Capable of 10Base-T full duplex operation
12	10 Mbps Full-Duplex	HW Rst	Always 1	
		SW Rst	Always 1	
		Mode	RO	
11	10 Mbs Half-Duplex	HW Rst	Always 1	Capable of 10Base-T half duplex operation
		SW Rst	Always 1	
		Mode	RO	
10	100BASE-T2 Full-Duplex	HW Rst	Always 0	Not able to perform 100BASE-T2
		SW Rst	Always 0	
		Mode	RO	
9	100BASE-T2 Half-Duplex	HW Rst	Always 0	Not able to perform 100BASE-T2
		SW Rst	Always 0	
		Mode	RO	
8	Extended Status	HW Rst	Always 1	Extended status information in register15
		SW Rst	Always 1	
		Mode	RO	
7	Reserved	HW Rst	Always 0	
		SW Rst	Always 0	

Table 14. Status PHY Register (Address Offset = 0x01, or 0d01)



		Mode	RO	
6	MF Preamble Suppression	HW Rst	Always 1	PHY accepts management frames with preamble suppressed
		SW Rst	Always 1	
		Mode	RO	1: Auto negotiation process complete 0:Auto negotiation process not complete
5	Auto-Negotiation Complete	HW Rst	0	
		SW Rst	0	
	Remote Fault	Mode	RO,LH	
4		HW Rst	0	1: Remote fault condition detected
		SW Rst	0	0:Remote fault condition not detected
	Auto-Negotiation Ability	Mode	RO	1 : PHY able to perform auto negotiation
3		HW Rst	Always 1	
		SW Rst	Always 1	
	Link Status	Mode	RO,LL	This register bit indicates whether the link was lost since the last read operation of this bit.
2		HW Rst	0	Register bit 17.10 (Link Real Time) reflects real-time link sta
		SW Rst	0	1 = Link is up 0 = Link is down or lost since last Read Operation
	Jabber Detect	Mode	RO,LH	
1		HW Rst	0	 1: Jabber condition detected 0: Jabber condition not detected
		SW Rst	0	
0	Extended Capbility	Mode	RO	1: Extended register capabilities
		HW Rst	Always 1	
		SW Rst	Always 1	

Table 15.PHY Identifier (Address Offset = 0x02, or 0d02)

ſ	Bits	Symbol		Туре	Description
ſ		Organizationally	Mode	RO	
	15:0	Unique Identifier (OUI) Bit 3:18	HW Rst	Always	Organizationally Unique Identifier bits 3:18
			SW Rst	Always	

Table 16.PHY iIdentifier2 (Address Offset = 0x03, or 0d03)

Bits	Symbol	Туре		Description
	OUI bit 19:24 Model Number Revision Number	Mode	RO	Organizationally Unique Identifier bits 19:24
15: 0		HW Rst	Always	Bit 9:0 is set by PHY interface pins mn[5:0] and rn[3:0].
		SW Rst	Always	

Description



Bits

Symbol

Mode R/W HW Rst 0 15 Reserved Reserved SW Rst Update Mode RO HW Rst Always 0 14 Ack Must be 0 SW Rst Always 0 Mode R/W 1 = Set Remote Fault bit HW Rst 0 13 Remote Fault 0 = Do not set Remote Fault bit SW Rst Update Mode RO HW Rst Always 0 12 Reserved Always 0. SW Rst Always 0 The value of this bit will be updated immediately after writing R/W Mode this register. But the value written to this bit does not takes effect until any one of the following occurs: HW Rst 1 • Software reset is asserted (register 0.15) • Restart Auto-Negotiation is asserted (register 0.9) • Power down (register 0.11) transitions from power down to 11 Asymmetric Pause normal operation • Link goes down SW Rst 1 = Asymmetric Pause Update 0 = No asymmetric Pause (this bit has added the pad control and can be set from the F001 top, its default value is one) The value of this bit will be updated immediately after writing Mode R/W this register. But the value written to this bit does not takes effect until any one of the following occurs: HW Rst 1 Software reset is asserted (register 0.15) • Restart Auto-Negotiation is asserted (register 0.9) • Power down (register 0.11) transitions from power down to 10 PAUSE normal operation • Link goes down SW Rst Update 1 = MAC PAUSE implemented 0 = MAC PAUSE not implemented (this bit has added the pad control and can be set from the F001 top, its default value is one) Mode RO HW Rst Always 0 9 100BASE-T4 Not able to perform 100BASE-T4 SW Rst Always 0

Table 17.Auto-Negotiation Advertisement PHY Register (Address Offset = 0x04, or
0d04)

Туре



		Mode	RW	The value of this bit will be updated immediately after writing
	100BASE-TX	HW Rst	1	 this register. But the value written to this bit does not takes effect until any one of the following occurs: Software reset is asserted (register 0.15) Restart Auto-Negotiation is asserted (register 0.9)
8	Full Duplex	SW Rst	Update	 Power down (register 0.11) transitions from power down to normal operation Link goes down 1 = Advertise 0 = Not advertised
		Mode	R/W	The value of this bit will be updated immediately after writing
-	100BASE-TX	HW Rst	1	 this register. But the value written to this bit does not takes effect until any one of the following occurs: Software reset is asserted (register 0.15) Restart Auto-Negotiation is asserted (register 0.9)
	7 Half Duplex	SW Rst	Update	 Power down (register 0.11) transitions from power down to normal operation Link goes down 1 = Advertise 0 = Not advertised
		Mode	R/W	The value of this bit will be updated immediately after writing
10BASE-TX	HW Rst	1	 this register. But the value written to this bit does not takes effect until any one of the following occurs: Software reset is asserted (register 0.15) Restart Auto-Negotiation is asserted (register 0.9) 	
6	6 Full Duplex	SW Rst	Update	 Power down (register 0.11) transitions from power down to normal operation Link goes down 1 = Advertise 0 = Not advertised
		Mode	RW	The value of this bit will be updated immediately after writing
10040	10BASE-TX	HW Rst	1	 this register. But the value written to this bit does not takes effect until any one of the following occurs: Software reset is asserted (register 0.15) Restart Auto-Negotiation is asserted (register 0.9)
5	Half Duplex	SW Rst	Update	 Power down (register 0.11) transitions from power down to normal operation Link goes down 1 = Advertise 0 = Not advertised
		Mode	RO	
4:0	Selector field	HW Rst	Always 00001	Selector Field mode 00001 = 802.3
		SW Rst	Always 00001	

Table 18.Link partner ability PHY register, base page (Address Offset = 0x05, or 0d05)

Bits	Symbol	Туре		Description
		Mode	RO	
15	Reserved	HW Rst	0	Reserved
		SW Rst	0	
	Ack	Mode	RO	Acknowledge
14		HW Rst	0	Received Code Word Bit 14 1 = Link partner received link code word
		SW Rst	0	0 = Link partner does not have Next Page ability



		Mode	RO	
13	Remote Fault	HW Rst	0	Remote Fault Received Code Word Bit 13 1 = Link partner detected remote fault
		SW Rst	0	0 = Link partner has not detected remote fault
\vdash		Mode	RO	
12	12 Reserved	HW Rst	0	Technology Ability Field Received Code Word Bit 12
		SW Rst	0	
		Mode	RO	Technology Ability Field
11	Asymmetric Pause	HW Rst	0	Received Code Word Bit 11 1 = Link partner requests asymmetric pause 0 = Link partner does not request asymmetric pause
		SW Rst	0	0 – Enk partner does not request asymmetric pause
		Mode	RO	
10	PAUSE	HW Rst	0	Technology Ability Field Received Code Word Bit 10 1 = Link partner is capable of pause operation
		SW Rst	0	0 = Link partner is not capable of pause operation
		Mode	RO	
9	9 100BASE-T4	HW Rst	0	Technology Ability Field Received Code Word Bit 9 1 = Link partner is 100BASE-T4 capable
		SW Rst		0 = Link partner is not 100BASE-T4 capable
		Mode	RO	
8	100BASE-TX Full Duplex	HW Rst	0	Technology Ability Field Received Code Word Bit 8 1 = Link partner is 100BASE-TX full-duplex capable 0 = Link partner is not 100BASE-TX full-duplex capable
		SW Rst	0	
		Mode	RO	
7	100BASE-TX Half Duplex	HW Rst	0	Technology Ability Field Received Code Word Bit 7 1 = Link partner is 100BASE-TX half-duplex capable 0 = Link partner is not 100BASE-TX half-duplex capable
		SW Rst	0	
		Mode	RO	
6	10BASE-TX Full Duplex	HW Rst	0	Technology Ability Field Received Code Word Bit 6 1 = Link partner is 10BASE-T full-duplex capable
		SW Rst	0	0 = Link partner is not 10BASE-T full-duplex capable
		Mode	RO	
5	10BASE-TX Half Duplex	HW Rst	0	Technology Ability Field Received Code Word Bit 5 1 = Link partner is 10BASE-T half-duplex capable
5				0 = Link partner is not 10BASE-T half-duplex capable



		Mode	RO	
4:0	Selector field	HW Rst	00000	Selector Field Received Code Word Bit 4:0
		SW Rst	00000	

Note: The values contained in reg5 are only guaranteed to be valid once auto-negotiation has successfully completed, as indicated by bit 1.5.

Table 19. Auto-Negotiation expansion PHY register (Address Offset = 0x06, or 0d06)

Bits	Symbol	Туре		Description
		Mode	RO	
15:5	Reserved	HW Rst	Always 0x000	Reserved. Must be 0.
		SW Rst	Always 0x000	
		Mode	RO,LH	
4	Parallel Detection fault	HW Rst	0	1: a fault has been detect 0: no fault has been detected
		SW Rst	0	
		Mode	RO	
3	Reserved	HW Rst	0	
		SW Rst	0	
		Mode	R/W	
2	Reserved	HW Rst	1	
		SW Rst	1	
		Mode	RO,LH	
1	Page received	HW Rst	0	1: A new page has been received 0: No new page has been received
		SW Rst	0	
		Mode	RO	
0	Link Partner Auto negotiation able	HW Rst	0	1: Link partner is auto negotiation able 0: Link partner is not auto negotiation able
		SW Rst	0	

Table 20.Function Control PHY register (Address Offset = 0x10, or 0d16)

Bits	Symbol	Ţ	уре	Description
15:12	Reserved	h/s w	0	Always 0
		Mode	R/W	
11	Assert CRS on Transmit	HW Rst	0	11
		SW Rst	Retain	



10	Reserved	h/s w	0	Always 0
		Mode	R/W	
9:8	Energy Detect	HW Rst	0	0x = Off 10 = Sense only on Receive (Energy Detect) 11 = Sense and periodically transmit NLP
		SW Rst	Retain	
		Mode	R/W	Changes to these bits are disruptive to the normal operation; therefore any changes to these registers must be followed by
6:5	MDI Crossover Mode	HW Rst	11	a software reset to take effect. 00 = Manual MDI configuration 01 = Manual MDIX configuration
		SW Rst	Update	10 = Reserved11 = Enable automatic crossover for all modes
4:3	Reserved	h/s w	0	Always 0
		Mode	R/W	
2	SQE Test	HW Rst	0	SQE Test is automatically disabled in full-duplex mode regardless of the state of register 16.2
		SW Rst	Retain	1 = SQE test enabled 0 = SQE test disabled
		Mode	R/W	If polarity is disabled, then the polarity is forced to be normal
1 Polarity Reversal HW Rst 0 10BASE-T. 1 = Polarity Reversal Disabled	10BASE-T. 1 = Polarity Reversal Disabled			
		SW Rst	Retain	0 = Polarity Reversal Enabled
		Mode	R/W	
0	Disable Jabber	HW Rst	0	Jabber has effect only in 10BASE-T half-duplex mode. 1 = Disable jabber function
		SW Rst	Retain	0 = Enable jabber function

Table 21.PHY specific status PHY register (Address Offset = 0x11, or 0d17)

Bits	Symbol	T	уре	Description
		Mode	RO	These status bits are valid only after resolved bit $17.11 = 1$. The resolved bit is set when Auto-Negotiation is completed or
		HW Rst	00	Auto-Negotiation is disabled.
15:14	Speed	SW Rst	Retain	11 = Reserved 10 = Reserved 01 = 100 Mbps 00 = 10 Mbps
	Duplex	Mode	RO	This status bit is valid only after resolved bit $17.11 = 1$. The
13		HW Rst	0	resolved bit is set when Auto-Negotiation is completed or Auto- Negotiation is disabled.
		SW Rst	Retain	1 = Full-duplex 0 = Half-duplex
		Mode	RO	
12	Page Received (real-time)	HW Rst	0	1 = Page received 0 = Page not received
		SW Rst	Retain	



11 Speed and Duplex Resolved HW Rst 0 1 = Resolved 11 Resolved SW Rst 0 When Auto-Negotiation is disabled, this bit will be set for speed mode. 10 Link (real-time) Mode RO 1 = Link up 0 = Link down 9: 7 reserved Mode RO 9: 7 reserved Mode RO 6 MDI Crossover Status Mode RO 6 MDI Crossover Status HW Rst 0 5 Smartspeed downgrade Mode RO 5 Smartspeed downgrade Mode RO 4 Energy Detect Status Mode RO 4 Energy Detect Status Mode RO 3 Pause Enabled SW Rst 0 3 Pause Enabled SW Rst 0			Mode	RO	
11 Speed and Duplex Resolved HW Rst 0 0 = Not resolved When Auto-Negotiation is disabled, this bit will be set for speed mode. 10 Link (real-time) Mode RO 1 = Link up 0 = Link down 10 Link (real-time) HW Rst 0 1 = Link up 0 = Link down 9: 7 reserved Mode RO 9: 7 reserved Mode RO 6 MDI Crossover Status Mode RO 6 MDI Crossover Status HW Rst 0 5 Smartspeed downgrade Mode RO 4 Energy Detect Transmit HW Rst 0 3 Pause Enabled SW Rst 0 4 Energy Detect Fransmit Mode RO HW Rst 0 7 Receive Pause Enabled SW Rst 0 - Active 7 Receive Pause Enabled SW Rst 0 - Active 1 Polarity (real HW Rst 0 - This is a reflection of the MAC pause resolution. This bit resolved bit is set when Auto-Negotiation is completed o Negotiation is disabled. 1 Transmit Pause Enabled SW Rst 0 - Active 1 Transmit Pause Enabled SW Rst 0 - Active 1 Mode RO <td></td> <td></td> <td></td> <td></td> <td>-</td>					-
11 Resolved Mode RO 10 Link (real-time) Mode RO 1 = Link up 0 = Link down 10 Link (real-time) HW Rst 0 1 = Link up 0 = Link down 9: 7 reserved Mode RO 9: 7 reserved Mode RO 6 MDI Crossover Status Mode RO This status bit is valid only after resolved bit 17.11 = 1. resolved bit is set when Auto-Negotiation is completed o Negotiation is disabled. This bit is 0 or 1 depending on N written to 16.615 are updated. This bit is 0 or 1 depending on N written to 16.615 are updated. This bit is 0 or 1 depending on N written to 16.615 are updated. This bit is 0 or 1 depending on N written to 16.615 are updated. This bit is 0 or 1 depending on N written to 16.615 are updated. This bit is 0 or 1 depending on N written to 16.615 are updated. This bit is 0 or 1 depending on N written to 16.615 are updated. This bit is 0 or 1 depending on N written to 16.615 are updated. This bit is 0 or 1 depending on N written to 16.615 are updated. This bit is 0 or 1 depending on N written to 16.615 are updated. This bit is 0 or 1 depending on N written to 16.615 are updated. This bit is 0 or 1 depending on N written to 16.615 are updated. This bit is 0 or 1 depending on N written to 16.615 are updated. This bit is 0 or 1 depending on N written to 16.615 are updated. This bit is 0 or 1 depending on N written to 16.615 are updated. This bit is 0 or 1 depending on N written to 16.615 are updated. This bit is 0 or 1 depending on N written to 16.615 are updated. This bit is 0 or 1 depending on N written to 16.6		Cread and Dunlay			
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3 Transmit Transmit This status bit is valid only after resolved bit 17.11 = 1. 3 Pause SW Rst Retain This status bit is valid only after resolved bit 17.11 = 1. 3 Pause SW Rst Retain This status bit is valid only after resolved bit 17.11 = 1. 3 Pause SW Rst Retain This status bit is valid only after resolved bit 17.11 = 1. 2 Mode RO This is a reflection of the MAC pause resolution. This bit information purposes and is not used by the device. 2 Pause SW Rst Retain 2 Pause SW Rst Retain 2 Pause SW Rst Retain 4 This status bit is valid only after resolved bit 17.11 = 1. resolved bit is set when Auto-Negotiation is completed o 2 Pause SW Rst Retain This status bit is valid only after resolved bit 17.11 = 1. 2 Pause SW Rst Retain This status bit is valid only after resolved bit 17.11 = 1. 1 Polarity (real Mode RO 1 = Receive pause enabled 1 Polarity (real Mode RO 1 = Reversed 1					This is a reflection of the MAC pause resolution. This bit is for
3 Pause Enabled SW Rst Retain resolved bit is set when Auto-Negotiation is completed of Negotiation is disabled. 3 Pause Enabled SW Rst Retain resolved bit is set when Auto-Negotiation is completed of Negotiation is disabled. 2 Pause Enabled Mode HW Rst Retain This is a reflection of the MAC pause resolution. This bit information purposes and is not used by the device. 2 Pause Enabled SW Rst Retain This status bit is valid only after resolved bit 17.11 = 1. resolved bit is set when Auto-Negotiation is completed o Negotiation is disabled. 1 Polarity (real Mode HW Rst RO HW Rst 1 = Reversed		Transmit	1111 1000	0	
Enabled SW Rst Retain Negotiation is disabled. 1 Enabled SW Rst Retain Negotiation is disabled. 1 Polarity (real Mode RO This is a reflection of the MAC pause resolution. This bit information purposes and is not used by the device. 1 Polarity (real Mode RO This status bit is valid only after resolved bit 17.11 = 1. resolved bit is set when Auto-Negotiation is completed o Negotiation is disabled. 1 Polarity (real Mode RO 1 = Receive pause enabled	2				This status bit is valid only after resolved bit $1/.11 = 1$. The resolved bit is set when Auto-Negotiation is completed or Auto-
1 Transmit pause enabled 0 Transmit pause disabled 0 Transmit pause disabled 1 Mode RO 1 Polarity (real Mode 1 Mode RO 1 HW Rst V 1 HW Rst V 1 HW Rst V 1 Receive Negotiation 1 Receive pause enabled 0 1 Receive Node 1 Receive Node 1 Receive pause disabled 1 Receive pause disabled 1 Receive pause disabled 1 Receive pause di	5		SW Rst	Retain	
Mode RO This is a reflection of the MAC pause resolution. This bit information purposes and is not used by the device. 2 Pause Enabled SW Rst Retain This status bit is valid only after resolved bit 17.11 = 1. resolved bit is set when Auto-Negotiation is completed o Negotiation is disabled. 1 Polarity (real Mode RO 1 = Reversed		LIUDIEU			1 = Transmit pause enabled
2 Pause Enabled SW Rst Retain Negotiation is concluded on the purposes and is not used by the device. 2 Pause Enabled SW Rst Retain This status bit is valid only after resolved bit 17.11 = 1. resolved bit is set when Auto-Negotiation is completed o Negotiation is disabled. 1 Polarity (real Mode RO 1 = Reversed 1 time) HW Rst 0 0					0 = Transmit pause disabled
2 Receive Pause Enabled SW Rst Retain This status bit is valid only after resolved bit 17.11 = 1. resolved bit is set when Auto-Negotiation is completed o Negotiation is disabled. 1 = Receive pause enabled 0 = Receive pause disabled 1 Polarity (real HW Rst Mode HW Rst RO 0 1 = Reversed					This is a reflection of the MAC pause resolution. This bit is for
2 Pause Enabled SW Rst Retain resolved bit is set when Auto-Negotiation is completed o Negotiation is disabled. 1 Polarity (real Mode RO 1 = Reversed 1 HW Rst 0 0 Negotiation		Deschus	IIW KSL	0	
Enabled SW Rst Retain Negotiation is disabled. 1 = Receive pause enabled 0 = Receive pause disabled 1 Polarity (real Mode RO 1 = Reversed 1 HW Rst 0 0 Neuron					
1 Polarity (real Mode RO 1 = Receive pause enabled 1 Polarity (real Mode RO 1 = Reversed	2		SW Rst	Retain	
Polarity (real Mode RO 1 = Reversed 1 HW Rst 0 0 Normal		Ellableu			5
1 HW Rst 0 A Normal					0 = Receive pause disabled
I HW RST U O Normal		Polarity (real			1 = Reversed
Mode RO			-		
			<u>├</u>		1
Jabber (real HW Rst 0 1 = Jabber	0	Jabber (real	HW Rst	0	1 = Jabber
0 time) HW RSt 0 I Subscr	U	time)		5	0 = No jabber
			0.11.5		4
SW Rst Retain			SW Rst	Retain	



Bits	Symbol	т	уре	Description
	Auto-Negotiation	Mode	RW	
15	Error Interrupt Enable	HW Rst	0	1 = Interrupt enable 0 = Interrupt disable
		SW Rst	Retain	
		Mode	RW	
14	Speed Changed Interrupt Enable	HW Rst	0	1 = Interrupt enable 0 = Interrupt disable
		SW Rst	Retain	
		Mode	RŴ	
13	Duplex Changed Interrupt Enable	HW Rst	0	1 = Interrupt enable 0 = Interrupt disable
		SW Rst	Retain	
		Mode	RW	-
12	Page Received Interrupt Enable	HW Rst	0	1 = Interrupt enable 0 = Interrupt disable
		SW Rst	Retain	
		Mode	RW	
11	Auto-Negotiation Completed Interrupt Enable	HW Rst	0	1 = Interrupt enable 0 = Interrupt disable
		SW Rst	Retain	
		Mode	RW	-
10	Link Status Changed	HW Rst	0	1 = Interrupt enable 0 = Interrupt disable
	Interrupt Enable	SW Rst	Retain	
		Mode	RW	
9	Symbol Error Interrupt Enable	HW Rst	0	1 = Interrupt enable 0 = Interrupt disable
		SW Rst	Retain	-
		Mode	RW	
8	False Carrier	HW Rst	0	1 = Interrupt enable 0 = Interrupt disable
	Interrupt Enable	SW Rst	Retain	
	FIFO Over/	Mode	RW	
7	Underflow	HW Rst	0	1 = Interrupt enable 0 = Interrupt disable
	Interrupt Enable	SW Rst	Retain	
		Mode	RW	
	MDI Croccovor			
6	MDI Crossover Changed	HW Rst	0	1 = Interrupt enable 0 = Interrupt disable

Table 22.Interrupt enable PHY register (Address Offset = 0x12, or 0d18)



	Smartspeed-	Mode	RW	
5	downgrade	HW Rst	0	1 = Interrupt enable 0 = Interrupt disable
	Interrupt Enable	SW Rst	Retain	
		Mode	RW	
4	Energy Detect Interrupt Enable	HW Rst	0	1 = Interrupt enable 0 = Interrupt disable
		SW Rst	Retain	
3:2	Reserved	h/s w	0	Always 00.
	Polarity	Mode	RW	
1		HW Rst	0	1 = Interrupt enable 0 = Interrupt disable
		SW Rst	Retain	
		Mode	RW	
0	Jabber Interrupt Enable	HW Rst	0	1 = Interrupt enable 0 = Interrupt disable
		SW Rst	Retain	

Table 23.Interrupt status PHY register (Address Offset = 0x13, or 0d19)

Bits	Symbol	Т	уре	Description
		Mode	RO, LH	An error will occur if there are parallel detect fault, no common
15	Auto-Negotiation Error	HW Rst	0	HCD, or link failure after negotiation completes. 1 = Auto-Negotiation Error
		SW Rst	Retain	0 = No Auto-Negotiation Error
		Mode	RO, LH	
14	14 Speed Changed	HW Rst	0	1 = Speed changed 0 = Speed not changed
		SW Rst	Retain	
		Mode	RO, LH	
13	Duplex Changed	HW Rst	0	1 = Duplex changed 0 = Duplex not changed
		SW Rst	Retain	
		Mode	RO	
12	Page Received	HW Rst	0	1 = Page received 0 = Page not received
		SW Rst	Retain	
		Mode	RO	1 = Auto-Negotiation completed
11	Auto-Negotiation Completed	HW Rst	0	0 = Auto-Negotiation not completed
		SW Rst	Retain	1



		Mode	RO, LH	
10	Link Status Changed	HW Rst	0	1 = Link status changed 0 = Link status not changed
		SW Rst	Retain	
		Mode	RO, LH	
9	Symbol Error	HW Rst	0	1 = Symbol error 0 = No symbol error
		SW Rst	Retain	
		Mode	RO, LH	
8	False Carrier	HW Rst	0	1 = False carrier 0 = No false carrier
		SW Rst	Retain	
		Mode	RO, LH	
7	7 Reserved	HW Rst	0	
		SW Rst	Retain	
		Mode	RO, LH	
6	MDI Crossover Changed	HW Rst	0	1 = Crossover changed 0 = Crossover not changed
		SW Rst	Retain	
	Smartspeed-	Mode	RO, LH	
5	downgrade	HW Rst	0	1 = Smartspeed-downgrade detected. 0 = No Smartspeed-downgrade.
	Interrupt	SW Rst	Retain	
		Mode	RO, LH	1 = Energy Detect state changed
4	Energy Detect Changed	HW Rst	0	0 = No Energy Detect state change detected
		SW Rst	Retain	Not implement, always 0.
3:2	reserved	h/s w	0	Always 00
	Dala ii	Mode	RO, LH	1 = Polarity Changed
1	1 Polarity Changed	HW Rst	0	0 = Polarity not changed
	-	SW Rst	Retain	
		Mode	RO, LH	1 = Jabber
0	Jabber	HW Rst	0	0 = No jabber
		SW Rst	Retain	

Table 24.SmartSpeed Control PHY Register (Address Offset = 0x14, or 0d20)

			Mode	RO	
15	:11	reserved	HW Rst	0	Reserved. Must be 00000000.
			SW Rst	0	



		Mode	R/W		
9	aneg_now_qual	HW Rst	1′b0	Set this bit to 1 to cause the PHY to restart	
	2	SW Rst	Retain	— autonegotiation.	
		Mode	R/W		
9	Rev_aneg_qual	HW Rst	1′b0	Make PHY to auto-negotiate in reversed mode.	
		SW Rst	Update	-	
		Mode	R/W		
8	Reserved	HW Rst	1′b0	Reserved	
		SW Rst	Update	_	
		Mode	R/W	The default value is zero; if this bit is set to	
7	Cfg_pad_en	HW Rst	0	one, then the auto negotiation Arbitration FSM will bypass the LINK_STATUS_CHECK state when the 10BASE-T/100BASE-TX	
		SW Rst	Update	ready signal is asserted.	
		Mode	R/W		
6	Mr_ltdis	HW Rst	0	 The default value is zero; if this bit is set t one, then the NLP Receive Link Integrity Test FSM will stays at the NLP_TEST_PASS state. 	
		SW Rst	Update	state.	
		Mode	R/W	The default value is one; if this bit is set to	
5	SmartSpeed_en	HW Rst	1	one and cable inhibits completion of the training phase, then After a few failed attempts, PHY automatically downgrades the highest	
		SW Rst	Update	ability to the next lower speed: from 100 to 10.	
		Mode	R/W		
4:2	SmartSpeed_retry_limit	HW Rst	011	The default value is three; if these bits are set to three, then the PHY will attempt five times before downgrading; The number of attempts can be changed through setting	
		SW Rst	Update	these bits.	
		Mode	R/W	The default value is zero; if this bit is set to	
1	Bypass_smartSpeed_timer	HW Rst	0	one, the SmartSpeed FSM will bypass the	
		SW Rst	Update	timer used for stability.	
		Mode	RO		
0	reserved	HW Rst	0	Reserved. Must be 0.	
		SW Rst	0		



Table 25.Receive error counter PHY register (Address Offset = 0x15, or 0d21)

		Mode	RO	
15:0	15:0 Receive Error Count HW Rst SW Rst	HW Rst	0×0000	Counter will peg at 0xFFFF and will not roll over. (when rx_dv is valid, count rx_er numbers)
		Retain	(in this version, only for 100Base-TX)	

Table 26.Virtual cable tester control PHY register (Address Offset = 0x16, or 0d22)

		Mode	RO	
15:10	15:10 Reserved	HW Rst	Always 0	Reserved.
		SW Rst	Always 0	
		Mode	RW	Virtual Cable Tester™ Control registers. Use the Virtual Cable Tester Control Registers to select which MDI pair is shown in
9:8	9:8 MDI Pair Select	HW Rst	00	the Virtual Cable Tester Status register. 00 = MDI[0] pair 01 = MDI[1] pair
		SW Rst	Retain	10 = Reserved 11 = Reserved
7:1	Reserved	h/s w	0	Always 0
		Mode	RW	When set, hardware automatically disables this bit when VCT is done.
0	0 Enable Test	HW Rst	0	1 = Enable VCT Test 0 = Disable VCT Test
		SW Rst	Retain	

Table 27.LED control PHY register (Address Offset = 0x18, or 0d24)

Bits	Symbol	Туре		Description
		Mode	R/W	
15	Disable LED	HW Rst	0	0 = Enable 1 = Disable
		SW Rst	Retain	
		Mode	R/W	001 = 10ms
14:12	Led on time	HW Rst	100	010 = 21 ms 011 = 42ms
112		SW Rst	Retain	100 = 84 ms 101 = 168ms 110 to 111 = 42ms



г		Mode	RO	
11	Force Interrupt	HW Rst	0	Always 0.
		SW Rst	0	
		Mode	R/W	000 = 21 ms
10:8	Led off time	HW Rst	001	001 = 42 ms 010 = 84 ms 011 =168 ms 100 =330 ms
		SW Rst	Retain	101 to 111 = 168ms
		Mode	RO	
7:5	Reserved	HW Rst	000	Reserved
		SW Rst	Always 0	
		Mode	R/W	
4:3	LED_LINK control	HW Rst	0	00 = Direct LED mode 11 = Master/Slave LED mode
		SW Rst	Retain	01, 10 = Combined LED modes
		Mode	R/W	0 = Duplex
2	LED_DUPLEX control	HW Rst	0	1 = Duplex/Collision
		SW Rst	Retain	
		Mode	R/W	
1	LED_RX control	HW Rst	0	1 = Receive activity/Link 0 = Receive activity
		SW Rst	Retain	
0	LED_TX Control	Mode HW Rst SW Rst	R/W 0 Retain	1 = Activity/Link 0 = Transmit activity

Table 28.Manual LED override PHY register (Address Offset = 0x19, or 0d25)

Bits	Symbol	Туре		Description
		Mode	RO	
15:12	Reserved	HW Rst	Always 0	Reserved.
		SW Rst	Always 0	
		Mode	R/W	LED "Off" means LED pin output equals high.
11:10	LED_	HW Rst	00	LED "On" means LED pin output equals low. 00 = Normal
11.10	DUPLEX	SW Rst	Retain	01 = Blink 10 = LED Off 11 = LED On



		Mode	R/W	LED "Off" means LED pin output equals high.
9:8	LED_LINK10	HW Rst	00	LED "On" means LED pin output equals low. 00 = Normal
	_	SW Rst	Retain	01 = Blink 10 = LED Off 11 = LED On
		Mode	R/W	LED "Off" means LED pin output equals high.
7:6	LED_LINK100	HW Rst	00	LED "On" means LED pin output equals low. 00 = Normal 01 = Blink 10 = LED Off
		SW Rst	Retain	11 = LED On
		Mode	R/W	
5:4	5:4 Reserved	HW Rst	00	Reserved
		SW Rst	Retain	
		Mode	R/W	
3:2	LED_RX	HW Rst	00	LED "Off" means LED pin output equals high. LED "On" means LED pin output equals low. 00 = Normal 01 = Blink
		SW Rst	Retain	10 = LED Off 11 = LED On
		Mode	R/W	LED "Off" means LED pin output equals high.
1:0	LED_TX	HW Rst	00	LED "On" means LED pin output equals low. 00 = Normal 01 = Blink 10 = LED Off
		SW Rst	Retain	11 = LED On

Table 29.Virtual cable tester status PHY register (Address Offset = 0x1c, or 0d28)

Bits	Symbol	т	уре	Description
		Mode	RO	
15:10	Reserved	HW Rst	Always 0	Reserved.
		SW Rst	Always 0	
		Mode	RO	The content of the Virtual Cable Tester Status Registers applies to the cable
		HW Rst	00	pair selected in the Virtual Cable Tester [™] Control Registers.
9:8	9:8 Status	SW Rst	00	 11 = Test Fail 00 = Valid test, normal cable (no short or open in cable) 10 = Valid test, open in cable (Impedance > 333 ohms) 01 = Valid test, short in cable (Impedance < 33 ohms)
		Mode	R/W	
7:0	Delta_Time	HW Rst	0	Delta time to indicate distance.
		SW Rst	0	



Bits	Symbol	Туре				
		Mode	RO			
15:6	15:6 Reserved	HW Rst	0	The address index of the register will be write or Read.		
		SW Rst	0			
		Mode	R/W			
5:0	5:0 Address Offset	HW Rst	0	The address index of the register will be Write or Read.		
		SW Rst	0			

Table 30. Address Port of Extended PHY Register (Address Offset = 0x1d, or 0d29)

Table 31.Data Port of Extended PHY Register (Address Offset = 0x1e, or 0d20)

		Mode	R/W	
15:0	Data	HW Rst	0	The data port of extended register. address offset must be set before accessing this register.
		SW Rst	0	

8.1 Extended Register description

Table 32. System Mode Control 0 (Address Offset = 0x00 (Hex), or 0(Decimal))

		Mode	R/W	
15:6	Reserved	HW Rst	10'h009	
		SW Rst		
		Mode	R/W	
5:4	TXDAC Class AB enable	HW Rst	0	
		SW Rst	Retain	[5]: 1 enable 100BASE-TX TXDAC Class AB Mode
		HW Rst	2′b01	[4]: 1 enable 10BASE-T TXDAC Class AB Mode
		SW Rst	Retain	



			Mode	R/W
3	:0	reserved	HW Rst	4′hE
			SW Rst	Retain

Table 33.System mode control 3 (Address Offset = 0x03 (Hex), or 3(Decimal))

	Reserved	Mode	R/W	
15		HW Rst	0	
		SW Rst	0	
		Mode	R/W	1 = the frame with link_status(register17.10) asserted
14	First_LUFrame_TX	HW Rst	0	in the middle of the frame will not be transmitted at all;
		SW Rst	Retain	0 = frames will be transmitted when link is up.
	Phy_pll_on	Mode	R/W	PLL control bit, makes AND connection with input pin
13		HW Rst	1	phy_pll_on to control PLL, 1 = PLL is always on, except iddq mode; 0 = PLL is control by hibernate module.
		SW Rst	Retain	
		Mode	R/W	
12:11	reesrved	HW Rst	2′b11	
		SW Rst	Retain	
		Mode	R/W	
10	LED test control	HW Rst	0	1: when power on reset, the LED will not light. 0: when power on reset, the LED will light for 2.5s.
		SW Rst	Retain	
		Mode	R/W	
9:0	reserved	HW Rst	10'h3FF	
		SW Rst	Retain	



		Mode	R/W	Power hibernate control bit;
15	Ps_hib_en	HW Rst	1	1: hibernate enable 0: hibernate disable
		SW Rst	retain	
		Mode	R/W	
14	Wake_mode	HW Rst	0	1:PHY wake up by energy detect or wake up pin 0:PHY wake up only by energy detect
		SW Rst	retain	
		Mode	R/W	
13	reserved	HW Rst	1	
		SW Rst	retain	
	Hib_pulse_sw	Mode	R/W	1: when hibernate, PHY sends NLP pulse and detects
12		HW Rst	1	signal from cable. 0: when hibernate, PHY doesn't send NLP pulse and
		SW Rst	retain	only detects signal from cable.
		Mode	R/W	1:when hibernate, shut off 25m clock of auto-
11	Gate_25m_en_sw	HW Rst	1	negotiation 0:25m clock to auto-negotiation is not controlled by
		SW Rst	retain	hibernate
		Mode	R/W	
10:0	reserved	HW Rst	11'h400	
		SW Rst	retain	

Table 34.Hibernation Mode Control Register (Address Offset = 0x0b (Hex), or 11
(Decimal))

Table 35.100BASE-TX Test Mode Register (Address Offset = 0x10 (Hex), or 16 (Decimal))

15	TM100_ENA	Mode	R/W	
		HW Rst	0	Enable 100BASE-TX loopback test mode.
		SW Rst	Retain	
	Reversed	Mode	R/W	
14:8		HW Rst	7′h00	Always 0.
		SW Rst	0	



		Mode	R/W	
7	Jitter_test	HW Rst	0	100BASE-TX jitter test
		SW Rst	Retain	
		Mode	R/W	
6	Os_test	HW Rst	0	100BASE-TX over-shoot test
		SW Rst	Retain	
		Mode	R/W	
5	Dcd_test	HW Rst	0	100BASE-TX DCD test
		SW Rst	Retain	
		Mode	R/W	
4	PMD_LPBK_2	HW Rst	0	PMA loopback, test MLT-3 Encoder and MLT-3 Decoder
		SW Rst	0	
		Mode	R/W	
3	PMD_LPBK_1	HW Rst	0	PMD loopback, test Scrambler and Descrambler
		SW Rst	0	
		Mode	R/W	
2	PMA_LPBK_2	HW Rst	0	PMA loopback, test Carrier Detect and Link Monitor
		SW Rst	0	
		Mode	R/W	
1	PMA_LPBK_1	HW Rst	0	PMA loopback, test FEF Generator and FEF Detector
		SW Rst	0	
		Mode	R/W	
0	PCS_LPBK	HW Rst	0	PCS loopback, test pcs_tx and pcs_rx
		SW Rst	0	



Table 36.10BASE-T Test Mode Register (Address Offset = 0x12 (Hex), or 18 (Decimal))

		Mode	R/W	
15:14	reserved	HW Rst	10′h120	
		SW Rst	Retain	
		Mode	R/W	
5	Test_mode[2]	HW Rst	0	bit2 of 3-bit test_mode[2:0]. See bit 1:0 of this register.
		SW Rst	0	
	reserved	HW Rst	2′b00	
4:3		SW Rst	0	
		SW Rst	retain	
	Loopback mode select	Mode	R/W	
2		HW Rst	0	1: lpbk2—deep in Loopback mode 0: lpbk1—shallow in Loopback mode (connect to dig10.test_mode_i[0])
		SW Rst	0	(
	Test_mode[1:0]	Mode	R/W	Combined with bit5:
1:0		HW Rst	0	[001]: packet with all ones, 10MHz sine wave [010]: pseudo random, [011]: normal link pulse only,
		SW Rst	0	[100]: 5MHz sin wave. Others: normal mode.

Table 37.Power Saving Control (Address Offset = 0x29 (Hex), or 41 (Decimal))

	Top_ps_en	Mode	RO	
15		HW Rst	1	1: top level power saving enable 0: top level power saving disable
		SW Rst	retained	
		Mode	R/W	
14:12	Reserved	HW Rst	3′h3	
		SW Rst	retained	



		Mode	R/W	
11:9	Dac_amp_100	HW Rst	3′h3	Control amplitude of transmit signal in 100BT mode
		SW Rst	retained	
		Mode	R/W	
8:6	Dac_amp_10	HW Rst	3′h3	Control amplitude of transmit signal in 100BT mode
		SW Rst	retained	
		Mode	R/W	
5:1	reserved	HW Rst	0	
		SW Rst	0	
		Mode	R/W	
0	Reserved	HW Rst	1	
		SW Rst	retained	

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Datasheet—82552V Fast Ethernet PHY





9.0 Non-Volatile Memory (NVM)

9.1 Introduction

This section is intended for designs using a 10/100 Mb/s LAN controller that is integrated into an Intel[®] Platform Control Hub (PCH) device in conjunction with an the 82552V Physical Layer Transceiver (PHY).

There are several LAN clients that might access the NVM such as hardware, LAN driver, and BIOS. Refer to the *I/O Control Hub 5, 6, and 7 EEPROM Map and Programming Information.* and the *Intel*[®]10/100 Mbps Ethernet Controller Family Software Technical Reference Manual, both from Intel, for more details.

Unless otherwise specified, all numbers in this section use the following numbering convention:

- Numbers that do not have a suffix are decimal (base 10).
- Numbers with a prefix of "0x" are hexadecimal (base 16).
- Numbers with a suffix of "b" are binary (base 2).

9.2 **EEUPDATE Utility**

Intel has created an EEUPDATE utility that can be used to update NVM LAN images. The tool uses two basic data files outlined in the following section (image file and MACaddress file). The EEUPDATE utility is flexible and can be used to update the entire NVM LAN region image or just the Ethernet controller MAC address. In addition, it also updates the checksum field after the region is modified. Note that other Flash programming utilities (such as FITC) might not have this capability. For more information on how to use EEUPDATE, refer to the eeupdate.txt file that is included with the EEUPDATE utility.

To obtain a copy of this program, contact your Intel representative.

9.2.1 Command Line Parameters

The DOS command format is as follows:

```
EEUPDATE Parameter 1 Parameter 2
```

where:

Parameter 1 = /D or /A

/D is used to update the entire region image./A is used to update just the Ethernet Individual Address.Parameter 2 = filename

In Example 1, Parameter_2 is file1.eep, which contains the complete NVM image in a specific format used to update the complete region. All comments in the .eep file must be preceded by a semicolon (;).

Datasheet—82552V Fast Ethernet PHY



Example 1. EEUPDATE /D file1.eep

In Example 1, Parameter 2 is file2.dat, which contains a list of IA addresses. The EEUPDATE utility finds the first unused address from this file and uses it to update the NVM. An address is marked used if it is followed by a date stamp. When the utility uses a specific address, a log file called eelog.dat is updated with that address. This updated file should be used as the .dat file for the next update.

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10.0 Checklists

Contact your Intel Representative for access to the 82552V Design and Board Layout Checklists.



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82552V Fast Ethernet PHY—Datasheet



11.0 Reference Schematics



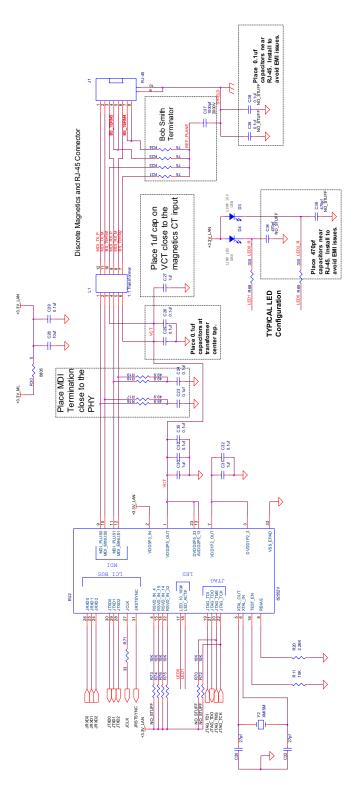


Figure 12. 82552V Reference Schematic--Discrete Magnetics



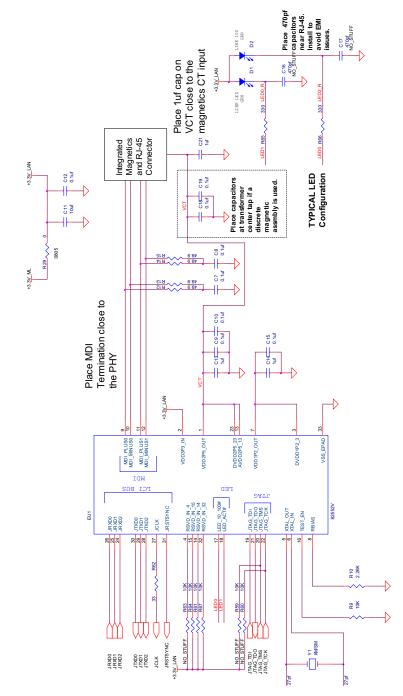


Figure 13. 82552V Schematic--Integrated Magnetics



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12.0 Models

Contact your Intel Representative for access to the 82552V XOR model.



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