- Compatible With IEEE Std 1194.1-1991 (BTL)

- TTL A Port, Backplane Transceiver Logic (BTL) $\overline{\text{B}}$ Port

- Open-Collector $\overline{\text{B}}$-Port Outputs Sink 100 mA

- High-Impedance State During Power Up and Power Down

- BIAS V_{CC} Pin Minimizes Signal Distortion During Live Insertion or Withdrawal

- $\overline{\text{B}}$-Port Biasing Network Preconditions the Connector and PC Trace to the BTL High-Level Voltage

SN54FB2040 . . . WD PACKAGE
(TOP VIEW)

NC	1	56	NC
OEB	2	55	$\overline{\text{OEB}}$
OEA	3	54	TCK
BIAS V_{CC}	4	53	V_{CC}
V_{CC}	5	52	TMS
AO1	6	51	GND
AI1	7	50	$\overline{\text{B1}}$
AO2	8	49	GND
GND	9	48	$\overline{\text{B2}}$
AI2	10	47	GND
AI3	11	46	$\overline{\text{B3}}$
AO3	12	45	GND
GND	13	44	$\overline{\text{B4}}$
AO4	14	43	GND
GND	15	42	$\overline{\text{B5}}$
AI4	16	41	GND
AI5	17	40	$\overline{\text{B6}}$
AO5	18	39	GND
GND	19	38	$\overline{\text{B7}}$
AO6	20	37	GND
GND	21	36	$\overline{\text{B8}}$
AI6	22	35	GND
GND	23	34	AI8
AO7	24	33	V_{CC}
BG V_{CC}	25	32	TDI
AI7	26	31	TDO
BG GND	27	30	AO8
NC	28	29	NC
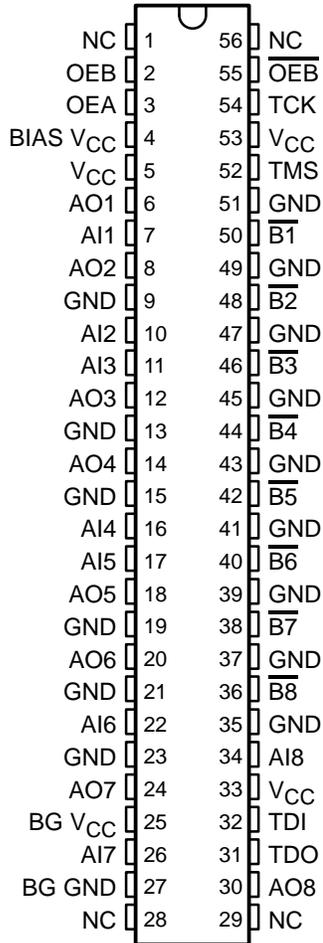
SN74FB2040 . . . RC PACKAGE
(TOP VIEW)

Top pins (52–40): AO2, AI1, AO1, V_{CC}, BIAS V_{CC}, OEA, OEB, $\overline{\text{OEB}}$, TCK, V_{CC}, TMS, GND, $\overline{\text{B1}}$

Left side (1–13): GND, AI2, AI3, AO3, GND, AO4, GND, AI4, AI5, AO5, GND, AO6, GND

Right side (39–27): GND, $\overline{\text{B2}}$, GND, $\overline{\text{B3}}$, GND, $\overline{\text{B4}}$, GND, $\overline{\text{B5}}$, GND, $\overline{\text{B6}}$, GND, $\overline{\text{B7}}$, GND

Bottom pins (14–26): AI6, GND, AO7, BG V_{CC}, AI7, BG GND, AO8, TDO, TDI, V_{CC}, AI8, GND, $\overline{\text{B8}}$
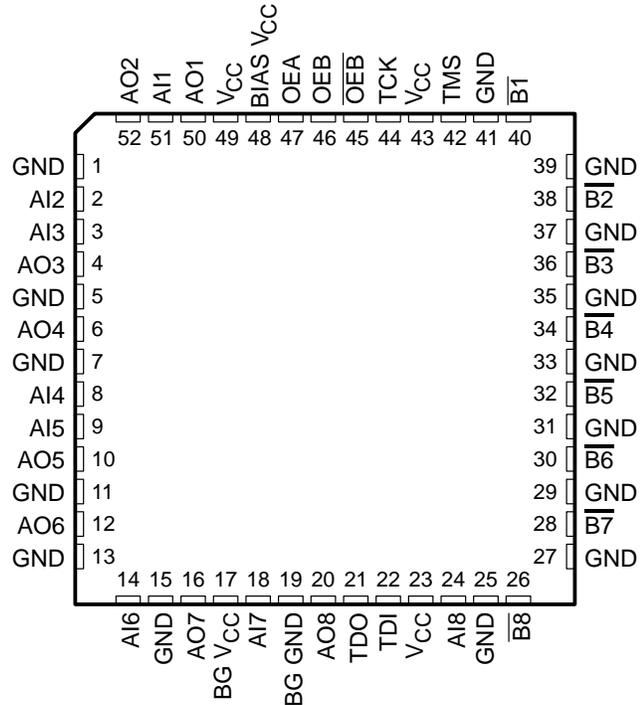
NC – No internal connection

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

TEXAS INSTRUMENTS

description

The 'FB2040 devices are 8-bit transceivers designed to translate signals between TTL and backplane transceiver logic (BTL) environments.

The $\overline{B}$ port operates at BTL-signal levels. The open-collector $\overline{B}$ ports are specified to sink 100 mA. Two output enables (OEB and $\overline{OEB}$) are provided for the $\overline{B}$ outputs. When OEB is high and $\overline{OEB}$ is low, the $\overline{B}$ port is active and reflects the inverse of the data present at the A-input pins. When OEB is low, $\overline{OEB}$ is high, or V_{CC} is less than 2.1 V, the $\overline{B}$ port is turned off.

The A port operates at TTL-signal levels and has separate input and output pins. The A outputs reflect the inverse of the data at the $\overline{B}$ port when the A-port output enable (OEA) is high. When OEA is low or when V_{CC} is less than 2.1 V, the A outputs are in the high-impedance state.

Pins are allocated for the four-wire IEEE Std 1149.1 (JTAG) test bus, although currently there are no plans to release a JTAG-featured version. TMS and TCK are not connected, and TDI is shorted to TDO.

BIAS V_{CC} establishes a voltage between 1.62 V and 2.1 V on the BTL outputs when V_{CC} is not connected.

ORDERING INFORMATION

T_A	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
0°C to 70°C	QFP – RC	Tube	SN74FB2040RC	FB2040
−55°C to 125°C	CFP – WD	Tube	SNJ54FB2040WD	SNJ54FB2040WD

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

FUNCTION TABLE

INPUTS			FUNCTION
OEB	$\overline{OEB}$	OEA	
L	X	L	Isolation
X	H	L	
L	X	H	$\overline{B}$ data to AO bus
X	H	H	
H	L	L	$\overline{AI}$ data to B bus
H	L	H	$\overline{AI}$ data to B bus, $\overline{B}$ data to AO bus

functional block diagram

To Seven Other Channels
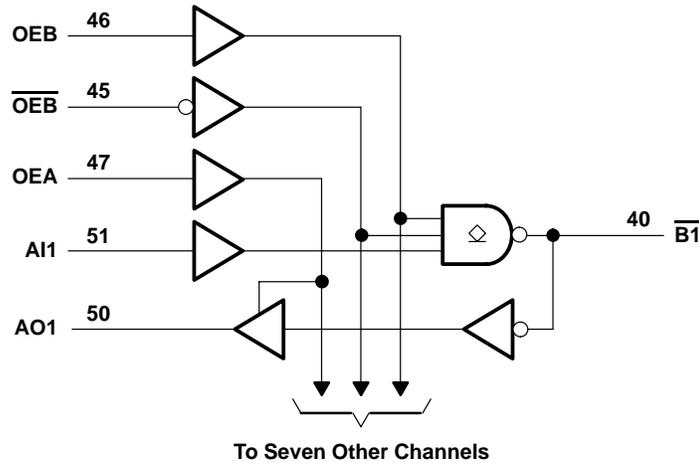
Pin numbers shown are for the RC package.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} . . . . –0.5 V to 7 V

Input voltage range, V_I: Except $\overline{B}$ port . . . . –1.2 V to 7 V

$\overline{B}$ port . . . . –1.2 V to 3.5 V

Voltage range applied to any $\overline{B}$ output in the disabled or power-off state, V_O . . . . –0.5 V to 3.5 V

Voltage range applied to any output in the high state, V_O: A port . . . . –0.5 V to V_{CC}

Input clamp current, I_{IK}: Except $\overline{B}$ port . . . . –40 mA

$\overline{B}$ port . . . . –18 mA

Current applied to any single output in the low state, I_O: A port . . . . 48 mA

$\overline{B}$ port . . . . 200 mA

Package thermal impedance, θ_{JA} (see Note 1) . . . . 44°C/W

Storage temperature range, T_{stg} . . . . –65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions (see Note 2)

			SN54FB2040			SN74FB2040			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}, BIAS V_{CC}, BG V_{CC}	Supply voltage		4.75	5	5.25	4.5	5	5.5	V
V_{IH}	High-level input voltage	$\overline{B}$ port	1.62*		2.3*	1.62		2.3	V
		Except $\overline{B}$ port	2			2			
V_{IL}	Low-level input voltage	$\overline{B}$ port	0.75*		1.47*	0.75		1.47	V
		Except $\overline{B}$ port			0.8			0.8	
I_{IK}	Input clamp current				−18			−18	mA
I_{OH}	High-level output current	AO port			−3			−3	mA
I_{OL}	Low-level output current	AO port			24			24	mA
		$\overline{B}$ port			100			100	
T_A	Operating free-air temperature		−55		125	0		70	°C

* On products compliant to MIL-PRF-38535, this parameter is not production tested.

NOTE 2: To ensure proper device operation, all unused inputs must be terminated as follows: A and control inputs to V_{CC}(5 V) or GND, and B inputs to GND only. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

TEXAS
INSTRUMENTS

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54FB2040 MIN	TYP†	MAX	SN74FB2040 MIN	TYP†	MAX	UNIT
V_{IK}	B port	$V_{CC} = 4.75$ V,	$I_I = -18$ mA			−1.2				V
		$V_{CC} = 4.5$ V,	$I_I = -18$ mA						−1.2	
	Except B port	$V_{CC} = 4.75$ V,	$I_I = -40$ mA			−1.2				
		$V_{CC} = 4.5$ V,	$I_I = -40$ mA						−0.5	
V_{OH}	AO port	$V_{CC} = 4.75$ V	$I_{OH} = -1$ mA		3.2					V
			$I_{OH} = -3$ mA	2.5	3.3					
		$V_{CC} = 4.5$ V,	$I_{OH} = -3$ mA				2.5	3.3		
V_{OL}	AO port	$V_{CC} = 4.75$ V	$I_{OL} = 20$ mA		0.09					V
			$I_{OL} = 24$ mA		0.35	0.5				
		$V_{CC} = 4.5$ V,	$I_{OL} = 24$ mA					0.35	0.5	
	$\overline{B}$ port	$V_{CC} = 4.75$ V,	$I_{OL} = 80$ mA	0.7		1.1				
		$V_{CC} = 4.5$ V,	$I_{OL} = 80$ mA				0.75		1.1	
		$V_{CC} = 4.75$ V,	$I_{OL} = 100$ mA			1.2				
		$V_{CC} = 4.5$ V,	$I_{OL} = 100$ mA						1.15	
I_I	Except B port	$V_{CC} = 5.25$ V,	$V_I = 5.25$ V			50				µA
		$V_{CC} = 5.5$ V,	$V_I = 5.5$ V						50	
I_{IH}‡	Except B port	$V_{CC} = 5.25$ V,	$V_I = 2.7$ V			50				µA
		$V_{CC} = 5.5$ V,	$V_I = 2.7$ V						50	
I_{IL}‡	Except B port	$V_{CC} = 5.25$ V,	$V_I = 0.5$ V			−50				µA
		$V_{CC} = 5.5$ V,	$V_I = 0.5$ V						−50	
	$\overline{B}$ port	$V_{CC} = 5.25$ V,	$V_I = 0.75$ V			−100				
		$V_{CC} = 5.5$ V,	$V_I = 0.75$ V						−100	
I_{OH}	B port	$V_{CC} = 0$ to 5.25 V,	$V_O = 2.1$ V			100				µA
		$V_{CC} = 0$ to 5.5 V,	$V_O = 2.1$ V						100	
I_{OZH}	AO port	$V_{CC} = 5.25$ V,	$V_O = 2.7$ V			50				µA
		$V_{CC} = 5.5$ V,	$V_O = 2.7$ V						50	
I_{OZL}	AO port	$V_{CC} = 5.25$ V,	$V_O = 0.5$ V			−50				µA
		$V_{CC} = 5.5$ V,	$V_O = 0.5$ V						−50	
I_{OZPU}	A port	$V_{CC} = 0$ to 2.1 V,	$V_O = 0.5$ V to 2.7 V			50			50	µA
I_{OZPD}	A port	$V_{CC} = 2.1$ V to 0,	$V_O = 0.5$ V to 2.7 V			−50			−50	µA
I_{OS}§	AO port	$V_{CC} = 5.25$ V,	$V_O = 0$	−30		−170				mA
		$V_{CC} = 5.5$ V,	$V_O = 0$				−30		−180	

† All typical values are at $V_{CC} = 5$ V, $T_A = 25°$C.
‡ For I/O ports, the parameters I_{IH} and I_{IL} include the off-state output current.
§ Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted) (continued)

PARAMETER		TEST CONDITIONS		SN54FB2040			SN74FB2040			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
I_{CC}	AI port to $\overline{B}$ port	V_{CC} = 5.25 V,	I_O = 0		25	40				mA
	$\overline{B}$ port to AO port				60	70				
	AI port to $\overline{B}$ port	V_{CC} = 5.5 V,	I_O = 0					40		
	$\overline{B}$ port to AO port							70		
C_i	AI port	$V_I = V_{CC}$ or GND				9.9*		3.5		pF
	Control inputs					9.9*		3		
C_o	AO port	$V_O = V_{CC}$ or GND				14.7*		6		pF
C_{io}	$\overline{B}$ port per IEEE Std 1194.1-1991	V_{CC} = 0 to 4.75 V				8**				pF
		V_{CC} = 0 to 4.5 V							5	
		V_{CC} = 4.75 V to 5.25 V				9**				
		V_{CC} = 4.5 V to 5.5 V							5	

* On products compliant to MIL-PRF-38535, this parameter is not production tested.

** On products compliant to MIL-PRF-38535, this parameter is not production tested and does not meet IEEE Std 1194.1-1991.

† All typical values are at V_{CC} = 5 V, T_A = 25°C.

## live-insertion specifications over recommended operating free-air temperature range

PARAMETER		TEST CONDITIONS			SN54FB2040		SN74FB2040		UNIT
					MIN	MAX	MIN	MAX	
I_{CC} (BIAS V_{CC})		V_{CC} = 0 to 4.75 V,	V_B = 0 to 2 V,	V_I (BIAS V_{CC}) = 4.75 V to 5.25 V		450			μA
		V_{CC} = 0 to 4.5 V,	V_B = 0 to 2 V,	V_I (BIAS V_{CC}) = 4.5 V to 5.5 V				450	
		V_{CC} = 4.75 to 5.25 V,	V_B = 0 to 2 V,	V_I (BIAS V_{CC}) = 4.75 V to 5.25 V		10			
		V_{CC} = 4.5 to 5.5 V,	V_B = 0 to 2 V,	V_I (BIAS V_{CC}) = 4.5 V to 5.5 V				10	
V_O	$\overline{B}$ port	V_{CC} = 0,	V_I (BIAS V_{CC}) = 5 V		1.62	2.1	1.62	2.1	V
I_O	$\overline{B}$ port	V_{CC} = 0,	V_B = 1 V	V_I (BIAS V_{CC}) = 4.75 V to 5.25 V	−30				μA
				V_I (BIAS V_{CC}) = 4.5 V to 5.5 V			−1		
		V_{CC} = 0 to 5.25 V,	OEB = 0 to 0.8 V			100			
		V_{CC} = 0 to 5.5 V,	OEB = 0 to 0.8 V					100	
		V_{CC} = 0 to 2.2 V,	OEB = 0 to 5 V			100		100	

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 1)

PARAMETER		FROM (INPUT)	TO (OUTPUT)	SN54FB2040					SN74FB2040					UNIT
				V_{CC} = 5 V, T_A = 25°C			MIN	MAX	V_{CC} = 5 V, T_A = 25°C			MIN	MAX	
				MIN	TYP	MAX			MIN	TYP	MAX			
t_{PLH}		AI	$\overline{B}$	2.5	4.5	6	0.5	8.5	3.2	4.5	6	2.4	6.5	ns
t_{PHL}				1.8	4.2	5.8	0.4	8.5	2.8	4.2	5.6	2.7	5.8	
t_{PLH}		$\overline{B}$	AO	1.5	3.8	5.7	0.4	8	2.3	3.8	5.7	1.9	6.2	ns
t_{PHL}				2.3	4.2	5.9	0.8	18	2.3	4.2	5.9	2	8.2	
t_{PLH}		OEB	$\overline{B}$	3.3	5.1	6.7	0.5	9.9	3.7	5.1	6.7	3	7	ns
t_{PHL}				3.1	4.6	6.2	0.4	9.5	3.1	4.6	5.9	3	6.1	
t_{PLH}		$\overline{OEB}$	$\overline{B}$	3.2	5.2	6.8	1.3	9.5	3.6	5.2	6.8	3.3	7	ns
t_{PHL}				2.9	4.4	6	0.2	9.8	2.9	4.4	5.9	2.6	6.1	
t_{PZH}		OEA	AO	1.7	4	5.5	1.2	8	2.5	4	5.5	2.1	5.8	ns
t_{PZL}				1.5	3.6	5.1	0.8	7.5	2.1	3.6	4.8	2	5	
t_{PHZ}		OEA	AO	1.8	4.1	5.9	1	8.2	2.3	4.1	5.9	1.9	6.5	ns
t_{PLZ}				1	3.1	4.7	0.4	7.2	1.6	3.1	4.5	1.4	4.7	
$t_{sk(p)}$	Skew for any single channel $\lvert t_{PHL} - t_{PLH}\rvert$, AI to $\overline{B}$ or $\overline{B}$ to AO				0.5					0.5				ns
$t_{sk(o)}$	Skew between drivers in the same package, AI to $\overline{B}$ or $\overline{B}$ to AO				0.4*					0.4				ns
t_r	Rise time, 1.3 V to 1.8 V, $\overline{B}$ port			0.2	2.8	3.8	0.2	4.5	2	2.8	3.8	1.7		ns
t_f	Fall time, 1.8 V to 1.3 V, $\overline{B}$ port			1	1.9	3	0.9	4.0	1	1.9	3	1	4.2	ns
$\overline{B}$-port input pulse rejection												1	3.4	ns

* On products compliant to MIL-PRF-38535, this parameter is not production tested.

PARAMETER MEASUREMENT INFORMATION

7 V
S1
Open

500 Ω

From Output Under Test

C_L = 50 pF
(see Note A)

500 Ω
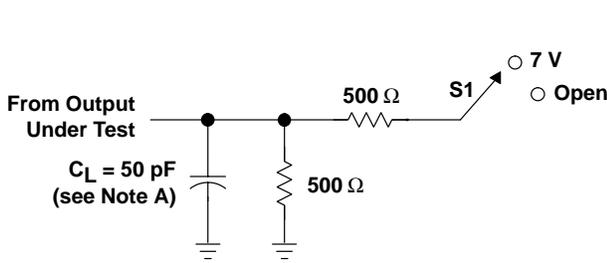
LOAD CIRCUIT FOR A OUTPUTS

2.1 V

16.5 Ω

From Output Under Test

Test Point

C_L = 30 pF
(see Note A)
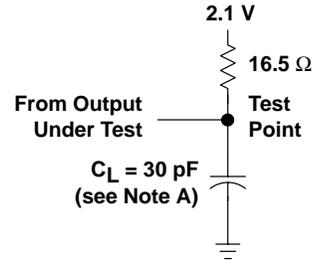
LOAD CIRCUIT FOR B OUTPUTS

Input — 3 V — 1.5 V — 1.5 V — 0 V

t_{PHL} t_{PLH}

Output — V_{OH} — 1.55 V — 1.55 V — V_{OL}

VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES (A TO B)
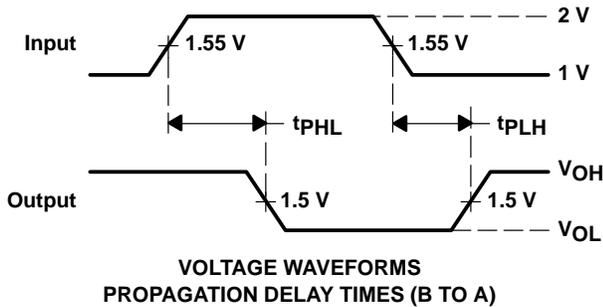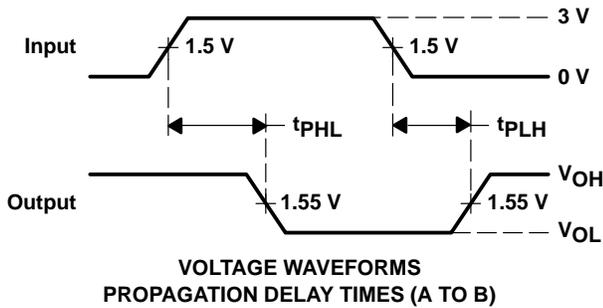
TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	7 V
t_{PHZ}/t_{PZH}	Open

Input — 2 V — 1.55 V — 1.55 V — 1 V

t_{PHL} t_{PLH}

Output — V_{OH} — 1.5 V — 1.5 V — V_{OL}

VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES (B TO A)

Output Control — 3 V — 1.5 V — 1.5 V — 0 V

t_{PZL} t_{PLZ}

Output Waveform 1
S1 at 7 V
(see Note B) — 3.5 V — 1.5 V — V_{OL} + 0.3 V — V_{OL}

t_{PZH} t_{PHZ}

Output Waveform 2
S1 at Open
(see Note B) — V_{OH} — 1.5 V — V_{OH} – 0.3 V — ≈0 V

VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES (A PORT)
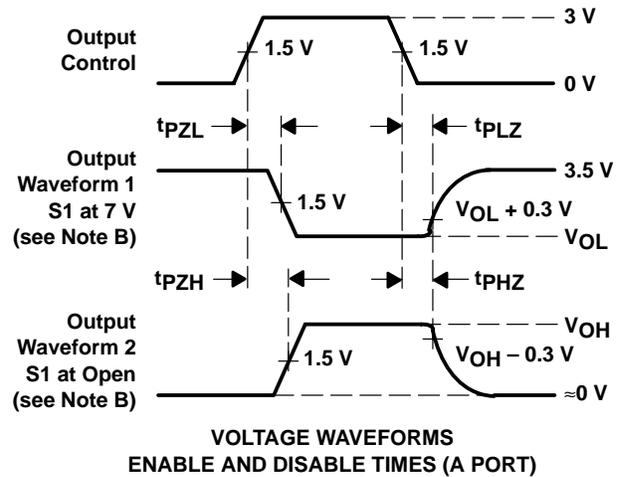
NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.
Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: TTL inputs: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns; BTL inputs: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuits and Voltage Waveforms

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