# ADS8284 18-BIT, 1-MSPS, Pseudo-Bipolar Differential SAR ADC with On-Chip ADC Driver (OPA) and 4-Channel Differential Multiplexer

## 1 Features

- 1.0-MHz Sample Rate, Zero Latency at Full Speed
- 18-Bit Resolution
- Supports Pseudo-Bipolar Differential Input Range: -4 V to +4 V with 2-V Common-Mode
- Built-In Four Channel, Differential Ended Multiplexer; with Channel Count Selection and Auto/Manual Mode
- On-Board Differential ADC Driver (OPA)
- Buffered Reference Output to Level Shift Bipolar ±4-V Input with External Resistance Divider
- Reference/2 Output to Set Common-Mode for External Signal Conditioner
- 18-/16-/8-Bit Parallel Interface
- SNR: 98.4dB Typ at 2-kHz I/P
- THD: –119dB Typ at 2-kHz I/P
- Power Dissipation: 331.25 mW at 1 MSPS Including ADC Driver
- Internal Reference
- Internal Reference Buffer
- 64-Pin QFN Package

## 2 Applications

- Medical Imaging/CT Scanners
- Automated Test Equipment
- High-Speed Data Acquisition Systems
- High-Speed Closed-Loop Systems

## 3 Description

The ADS8284 is a high-performance analog system-on-chip (SoC) device with an 18-bit, 1-MSPS A/D converter, 4-V internal reference, an on-chip ADC driver (OPA), and a 4-channel differential multiplexer. The channel count of the multiplexer and auto/manual scan modes of the device are user selectable.

The ADC driver is designed to leverage the very high noise performance of the differential ADC at optimum power usage levels.

The ADS8284 outputs a buffered reference signal for level shifting of a ±4-V bipolar signal with an external resistance divider. A $V_{ref}/2$ output signal is available to set the common-mode of a signal conditioning circuit. The device also includes an 18-/16-/8-bit parallel interface.

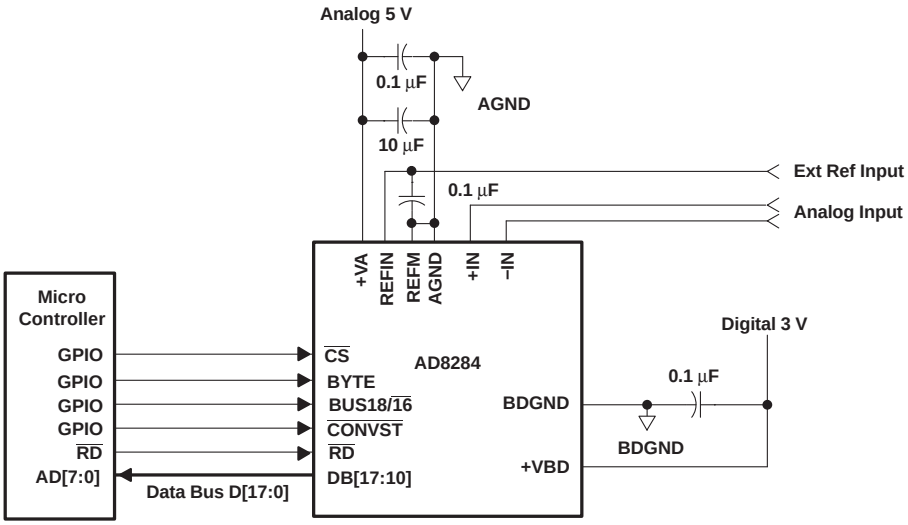
The ADS8284 is available in a 9 mm x 9 mm, 64-pin QFN package and is characterized from -40°C to 85°C.

**Device Information** (1)

| DEVICE NAME | PACKAGE | BODY SIZE |
|---|---|---|
| ADS8284 | QFN (64) | 9mm x 9mm |

(1) For all available packages, see the orderable addendum at the end of the data sheet.

**Simplified Schematic**



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## 4 Revision History

**Changes from Original (March 2009) to Revision A** **Page**

- Changed the data sheet to the new TI standard ... 1
- Added the Device Information table ... 1
- Added the Handling Ratings table ... 6
- Added Reference/2 Voltage Range to the Electrical Characteristics table ... 8
- Added the Power Supply Recommendations section ... 36

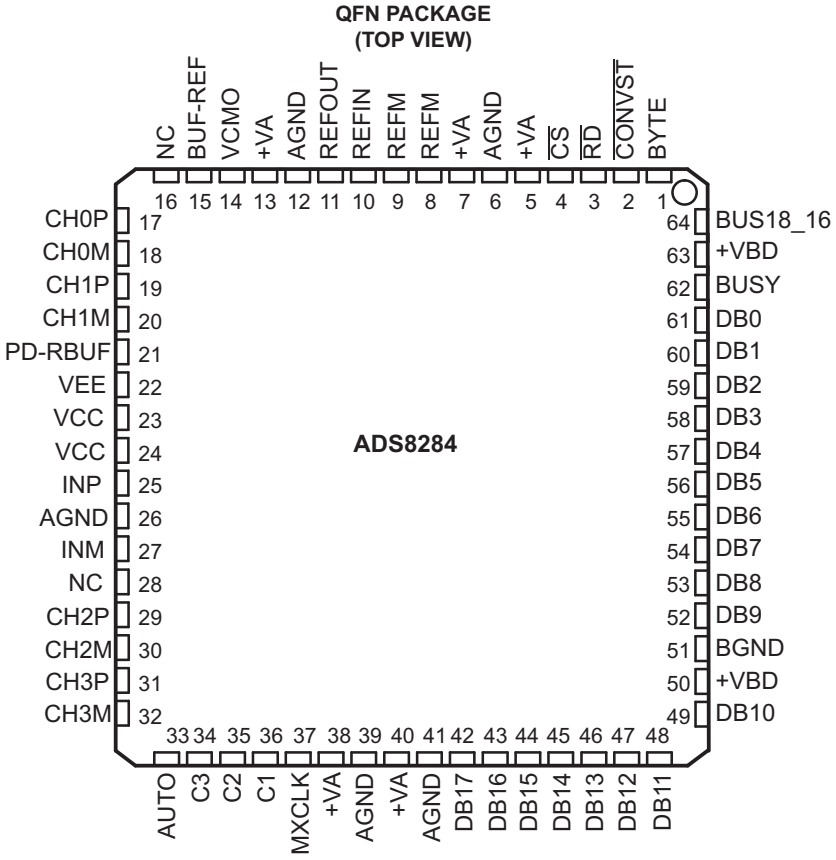
**Device Comparison Table**

| TYPE/SPEED | 500 kHz | ~600 kHz | 750 kHz | 1 MHz | 1.25 MHz | 2 MHz | 3 MHz | 4MHz |
|---|---|---|---|---|---|---|---|---|
| 18-Bit Pseudo-Diff | ADS8383 | ADS8381 | | ADS8481 | | | | |
| | | ADS8380 (s) | | | | | | |
| 18-Bit Pseudo-Bipolar, Fully Diff | | ADS8382 (s) | | ADS8284 | ADS8484 | | | |
| | | | | ADS8482 | | | | |
| 16-Bit Pseudo-Diff | ADS8327 | ADS8370 (s) | ADS8371 | ADS8471 | ADS8401 | ADS8411 | | |
| | ADS8328 | | | | ADS8405 | ADS8410 (s) | | |
| | ADS8319 | | | | | | | |
| 16-Bit Pseudo-Bipolar, Fully Diff | ADS8318 | ADS8372 (s) | | ADS8472 | ADS8402 | ADS8412 | | ADS8422 |
| | | | | ADS8254 | ADS8406 | ADS8413 (s) | | |
| 14-Bit Pseudo-Diff | | | | | ADS7890 (s) | | ADS7891 | |
| 12-Bit Pseudo-Diff | | | | ADS7886 | | ADS7883 | | ADS7881 |

**Device Linearity**

| MODEL | MAXIMUM INTEGRAL LINEARITY (LSB) | MAXIMUM DIFFERENTIAL LINEARITY (LSB) | NO MISSING CODES AT RESOLUTION (BIT) |
|---|---|---|---|
| ADS8284IB | ±2.5 | +1.5/–1 | 18 |
| ADS8284I | ±4.5 | +1.5/–1 | 18 |

## 5 Pin Configuration and Function



## Pin Functions

| PIN | | I/O | DESCRIPTION |
|---|---|---|---|
| NO | NAME | | |
| **MULTIPLEXER INPUT PINS** | | | |
| 17 | CH0P | I | Non-inverting analog input for differential multiplexer channel number 0. Device performance is optimized for 50-Ω source impedance at this input. |
| 18 | CH0M | I | Inverting analog input for differential multiplexer channel number 0. Device performance is optimized for 50-Ω source impedance at this input. |
| 19 | CH1P | I | Non-inverting analog input for differential multiplexer channel number 1. Device performance is optimized for 50-Ω source impedance at this input. |
| 20 | CH1M | I | Inverting analog input for differential multiplexer channel number 1. Device performance is optimized for 50-Ω source impedance at this input. |
| 29 | CH2P | I | Non-inverting analog input for differential multiplexer channel number 2. Device performance is optimized for 50-Ω source impedance at this input. |
| 30 | CH2M | I | Inverting analog input for differential multiplexer channel number 2. Device performance is optimized for 50-Ω source impedance at this input. |
| 31 | CH3P | I | Non-inverting analog input for differential multiplexer channel number 3. Device performance is optimized for 50 ohm source impedance at this input. |
| 32 | CH3M | I | Inverting analog input for differential multiplexer channel number 3. Device performance is optimized for 50-Ω source impedance at this input. |
| **ADC INPUT PINS** | | | |
| 25 | INP | I | ADC Non inverting input., connect 1-nF capacitor across INP and INM |
| 27 | INM | I | ADC Inverting input, connect 1-nF capacitor across INP and INM |
| **REFERENCE INPUT/ OUTPUT PINS** | | | |
| 8, 9 | REFM | I | Reference ground. |
| 10 | REFIN | I | Reference Input. Add 0.1-µF decoupling capacitor between REFIN and REFM. |
| 11 | REFOUT | O | Reference Output. Add 1-µF capacitor between the REFOUT pin and REFM pin when internal reference is used. |
| 14 | VCMO | O | This pin outputs REFIN/2 and can be used to set common-mode voltage of differential analog inputs. |
| 15 | BUF-REF | O | Buffered reference output. Useful to level shift bipolar signals using external resistors. |
| **POWER CONTROL PINS** | | | |
| 21 | PD-RBUF | I | High on this pin powers down the reference buffer (BUF-REF). |
| **MULTIPLEXER CONTROL PINS** | | | |
| 33 | AUTO | I | High level on this pin selects auto mode for multiplexer scanning. Low level selects manual mode of multiplexer scanning |
| 34 | C3 | I | In auto mode (AUTO = 1) multiplexer channel selection is reset to CH0 on rising edge of MXCLK while C3 = 1. The pin is do not care in manual mode. |
| 35 | C2 | I | Acts as multiplexer address bit when AUTO = 0 (manual mode). In auto mode (AUTO = 1) C2 and C1 select the last multiplexer channel (channel count) in the auto scan sequence. |
| 36 | C1 | I | Acts as multiplexer address LSB when AUTO = 0 (manual mode). In auto mode (AUTO = 1) C2 and C1 select the last multiplexer channel (channel count) in the auto scan sequence. |
| 37 | MXCLK | I | Multiplexer channel is selected on rising edge of MXCLK irrespective of whether it is auto or manual mode. Device BUSY output can be connected to MXCLK so that device selects next channel at the end of every sample. |
| **ADC DATA BUS** | | | |
| 42-49, 52-61 | Data Bus | | 8-BIT BUS: BYTE = 0, BUS18/$\overline{16}$ = 0 \| 8-BIT BUS: BYTE = 1, BUS18/$\overline{16}$ = 0 \| 8-BIT BUS: BYTE = 1, BUS18/$\overline{16}$ = 1 \| 16-BIT BUS: BYTE = 0, BUS18/$\overline{16}$ = 0 \| 16-BIT BUS: BYTE = 0, BUS18/$\overline{16}$ = 1 \| 18-BIT BUS: BYTE = 0, BUS18/$\overline{16}$ = 0 |
| 42 | DB17 | O | D17 (MSB) | D9 | All ones | D17 (MSB) | All ones | D17 (MSB) |
| 43 | DB16 | O | D16 | D8 | All ones | D16 | All ones | D16 |
| 44 | DB15 | O | D15 | D7 | All ones | D15 | All ones | D15 |
| 45 | DB14 | O | D14 | D6 | All ones | D14 | All ones | D14 |
| 46 | DB13 | O | D13 | D5 | All ones | D13 | All ones | D13 |
| 47 | DB12 | O | D12 | D4 | All ones | D12 | All ones | D12 |
| 48 | DB11 | O | D11 | D3 | D1 | D11 | All ones | D11 |
| 49 | DB10 | O | D10 | D2 | D0 (LSB) | D10 | All ones | D10 |
| 52 | DB9 | O | D9 | All ones | All ones | D9 | All ones | D9 |
| 53 | DB8 | O | D8 | All ones | All ones | D8 | All ones | D8 |
| 54 | DB7 | O | D7 | All ones | All ones | D7 | All ones | D7 |
| 55 | DB6 | O | D6 | All ones | All ones | D6 | All ones | D6 |
| 56 | DB5 | O | D5 | All ones | All ones | D5 | All ones | D5 |

## Pin Functions (continued)

| PIN | | I/O | DESCRIPTION | | | | | |
|---|---|---|---|---|---|---|---|---|
| NO | NAME | | | | | | | |
| 57 | DB4 | O | D4 | All ones | All ones | D4 | All ones | D4 |
| 58 | DB3 | O | D3 | All ones | All ones | D3 | D1 | D3 |
| 59 | DB2 | O | D2 | All ones | All ones | D2 | D0 (LSB) | D2 |
| 60 | DB1 | O | D1 | All ones | All ones | D1 | All ones | D1 |
| 61 | DB0 | O | D0 (LSB) | All ones | All ones | D0 (LSB) | All ones | D0 (LSB) |
| **ADC CONTROL PINS** | | | | | | | | |
| 62 | BUSY | O | Status output. This pin is held high when device is converting. | | | | | |
| 64 | BUS18_16 | I | Bus size select input. Used for selecting 18-bit or 16-bit wide bus transfer. Refer to ADC DATA BUS description above. | | | | | |
| 1 | BYTE | I | Byte Select Input. Used for 8-bit bus reading. Refer to ADC DATA BUS description above. | | | | | |
| 2 | $\overline{\text{CONVST}}$ | I | Convert start. This input is active low and can act independent of the $\overline{\text{CS}}$ input. | | | | | |
| 3 | $\overline{\text{RD}}$ | I | Synchronization pulse for the parallel output. | | | | | |
| 4 | $\overline{\text{CS}}$ | I | Chip select. | | | | | |
| **DEVICE POWER SUPPLIES** | | | | | | | | |
| 22 | VEE | | Negative supply for OPA (OP1, OP2) | | | | | |
| 23, 24 | VCC | | Positive supply for OPA (OP1, OP2, BUF-REF) | | | | | |
| 5, 7, 13, 38, 40 | +VA | | Analog power supply. | | | | | |
| 6, 12, 26, 39, 41 | AGND | | Analog ground. | | | | | |
| 50, 63 | +VBD | | Digital power supply for ADC bus. | | | | | |
| 51 | BGND | | Digital ground for ADC bus interface digital supply. | | | | | |
| **NOT CONNECTED PINS** | | | | | | | | |
| 16, 28 | NC | | No connection. | | | | | |

# 6 Specifications

## 6.1 Absolute Maximum Ratings(1)

over operating free-air temperature range (unless otherwise noted)

| | MIN | MAX | UNIT |
|---|---|---|---|
| CH(i) to AGND (both P and M inputs) | VEE–0.3 | VCC + 0.3 | V |
| VCC to VEE | -0.3 | 18 | V |
| +VA to AGND | –0.3 | 7 | V |
| +VBD to BDGND | –0.3 | 7 | V |
| ADC control digital input voltage to GND | –0.3 | (+VBD + 0.3) | V |
| ADC control digital output to GND | –0.3 | (+VBD + 0.3) | V |
| Multiplexer control digital input voltage to GND | –0.3 | (+VA + 0.3) | V |
| Power control digital input voltage to GND | –0.3 | (+VCC + 0.3) | V |
| Operating temperature range | –40 | 85 | °C |
| Junction temperature ($T_J$max) | | 150 | °C |

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

## 6.2 Handling Ratings

| | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| $T_{stg}$ | Storage temperature range | | –65 | 150 | °C |
| $V_{(ESD)}$ | Electrostatic discharge | Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1) | –2 | 2 | kV |
| | | Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2) | –500 | 500 | V |

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

## 6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

| | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|
| Analog Input at Multiplexer Inputs | CHxP, CHxM | 0 | | $V_{REF}$ | V |
| Digital Supply Voltage | +VBD | 2.7 | 3.3 | 5.25 | V |
| Analog Supply Voltage | +VA | 4.75 | 5 | 5.25 | V |
| Positive Supply Voltage for OPA | VCC | 4.75 | 5 | 7.5 | V |
| Negative Supply Voltage for OPA | VEE | –7.5 | –5 | –3 | V |

## 6.4 Thermal Information

| THERMAL METRIC(1) | | RCG 64 PINS | UNIT |
|---|---|---|---|
| $R_{\theta JA}$ | Junction-to-ambient thermal resistance | 24.0 | °C/W |
| $R_{\theta JC(top)}$ | Junction-to-case(top) thermal resistance | 7.8 | |
| $R_{\theta JB}$ | Junction-to-board thermal resistance | 3.2 | |
| $\psi_{JT}$ | Junction-to-top characterization parameter | 0.1 | |
| $\psi_{JB}$ | Junction-to-board characterization parameter | 3.2 | |
| $R_{\theta JC(bottom)}$ | Junction-to-case(bottom) thermal resistance | n/a | |

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

## 6.5 Electrical Characteristics

$T_A$ = –40°C to 85°C, VCC = 5 V, VEE = –5 V, +VA = 5 V, +VBD = 5 V or 3.3 V, $V_{ref}$ = 4 V, $f_{SAMPLE}$ = 1 MSPS (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **ANALOG INPUT** | | | | | | |
| Full-scale input voltage at multiplexer input(1) | | CH(i)P–CH(i)M | $–V_{ref}$ | | $V_{ref}$ | V |
| Absolute input range at multiplexer input | | CH (i) | –0.2 | | $V_{ref}$ + 0.2 | V |
| Input common-mode voltage | | [CH(i)P + CH(i)M] /2 | $(V_{ref})/2$ – 0.2 | $(V_{ref})/2$ | $(V_{ref})/2$ + 0.2 | V |
| **SYSTEM PERFORMANCE** | | | | | | |
| Resolution | | | | 18 | | Bits |
| No missing codes | ADS8284IB | | 18 | | | Bits |
| | ADS8284I | | 18 | | | |
| Integral linearity (2) | ADS8284IB | | –2.5 | ±1.25 | 2.5 | LSB (3) |
| | ADS8284I | | –4.5 | ±1.5 | 4.5 | |
| Differential linearity | ADS8284IB | At 18-bit level | –1 | ±0.6 | 1.5 | LSB(3) |
| | ADS8284I | | –1 | ±0.6 | 1.5 | |
| Offset error | ADS8284IB | | –0.5 | ±0.05 | 0.5 | mV |
| | ADS8284I | | –0.5 | ±0.05 | 0.5 | |
| Gain error(4) | ADS8284IB | External reference | –0.1 | ±0.025 | 0.1 | %FS |
| | ADS8284I | | –0.1 | ±0.025 | 0.1 | |
| DC power supply rejection ratio | | At $3FFF0_H$ output code. For +VA or VCC, VEE variation of 0.5 V individually | | 80 | | dB |
| **SAMPLING DYNAMICS** | | | | | | |
| Conversion time | | +VBD = 5 V | | 625 | 650 | ns |
| | | +VDB = 3 V | | 625 | 650 | ns |
| Acquisition time | | +VBD = 5 V | 320 | 350 | | ns |
| | | +VDB = 3 V | 320 | 350 | | |
| Maximum throughput rate | | | | | 1.0 | MHz |
| Aperture delay | | | | 4 | | ns |
| Aperture jitter | | | | 5 | | ps |
| Settling time to 0.5 LSB | | For ADC only | | 150 | | ns |
| | | For OPA (OP1, OP2) + mux | | 700 | | |
| Over voltage recovery | | For ADC only | | 150 | | ns |
| **DYNAMIC CHARACTERISTICS** | | | | | | |
| Total harmonic distortion (THD)(5) | ADS8284I | $V_{IN}$ = 4 $V_{pp}$ at 2 kHz | | –119 | | dB |
| | ADS8284IB | | | –119 | | |
| | ADS8284I | $V_{IN}$ = 4 $V_{pp}$ at 10 kHz | | –105 | | dB |
| | ADS8284IB | | | –105 | | |
| | ADS8284I | $V_{IN}$ = 4 $V_{pp}$ at 100 kHz, LoPWR = 0 | | –100 | | dB |
| | ADS8284IB | | | –100 | | |
| Signal-to-noise ratio (SNR) | ADS8284I | $V_{IN}$ = 4 $V_{pp}$ at 2 kHz | | 98.4 | | dB |
| | ADS8284IB | | 97.5 | 98.4 | | |
| | ADS8284I | $V_{IN}$ = 4 $V_{pp}$ at 10 kHz | | 98 | | dB |
| | ADS8284IB | | | 98 | | |
| | ADS8284I | $V_{IN}$ = 4 $V_{pp}$ at 100 kHz, LoPWR = 0 | | 95 | | dB |
| | ADS8284IB | | | 97 | | |

(1) Ideal input span, does not include gain or offset error.
(2) This is endpoint INL, not best fit.
(3) LSB means least significant bit.
(4) Calculated on the first nine harmonics of the input frequency.
(5) Measured relative to acutal measured reference.

## Electrical Characteristics (continued)

$T_A$ = –40°C to 85°C, VCC = 5 V, VEE = –5 V, +VA = 5 V, +VBD = 5 V or 3.3 V, $V_{ref}$ = 4 V, $f_{SAMPLE}$ = 1 MSPS (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| Signal-to-noise + distortion (SINAD) | ADS8284I | $V_{IN}$ = 4 $V_{pp}$ at 2 kHz | | 98.3 | | dB |
| | ADS8284IB | | | 98.3 | | |
| | ADS8284I | $V_{IN}$ = 4 $V_{pp}$ at 10 kHz | | 97.2 | | dB |
| | ADS8284IB | | | 97.2 | | |
| | ADS8284I | $V_{IN}$ = 4 $V_{pp}$ at 100 kHz, LoPWR = 0 | | 93.8 | | dB |
| | ADS8284IB | | | 95.23 | | |
| Spurious free dynamic range (SFDR) | ADS8284I | $V_{IN}$ = 4 $V_{pp}$ at 2 kHz | | 121 | | dB |
| | ADS8284IB | | | 121 | | |
| | ADS8284I | $V_{IN}$ = 4 $V_{pp}$ at 10 kHz | | 106 | | dB |
| | ADS8284IB | | | 106 | | |
| | ADS8284I | $V_{IN}$ = 4 $V_{pp}$ at 100 kHz, LoPWR = 0 | | 101 | | dB |
| | ADS8284IB | | | 101 | | |
| –3dB small signal bandwidth | | | | 8 | | MHz |
| **VOLTAGE REFERENCE INPUT (REFIN)** | | | | | | |
| Reference voltage at REFIN, $V_{ref}$ | | | 3.0 | 4.096 | +VA – 0.8 | V |
| Reference input current(6) | | | | 1 | 1 | µA |
| **INTERNAL REFERENCE OUTPUT (REFOUT)** | | | | | | |
| Internal reference start-up time | | From 95% (+VA), with 1-µF storage capacitor | | | 120 | ms |
| Reference voltage range, $V_{ref}$ | | | 4.081 | 4.096 | 4.111 | V |
| Source current | | Static load | | | 10 | µA |
| Line regulation | | +VA = 4.75 V to 5.25 V | | 60 | | µV |
| Drift | | $I_O$ = 0 | | ±6 | | PPM/°C |
| **BUFFERED REFERENCE OUTPUT (BUF-REF)** | | | | | | |
| Output current | | REFIN = 4 V, at 85°C | | 70 | | mA |
| **REFERENCE/2 OUTPUT (VCMO)** | | | | | | |
| Reference/2 Voltage Range | | At No Load on VCMO | 1.938 | 2.048 | 2.158 | V |
| Output current | | REFIN = 4 V, at +85°C | | 50 | | µA |
| **ANALOG MULTIPLEXER** | | | | | | |
| Number of channels | | | | | 4 | |
| Channel to channel crosstalk | | 100 kHz i/p | | –95 | | dB |
| Channel selection | | Auto sequencer with selection of channel count or manual selection through control lines | | | | |
| **DIGITAL INPUT-OUTPUT** | | | | | | |
| **ADC CONTROL PINS** | | | | | | |
| Logic Family-CMOS | | | | | | |
| Logic level | $V_{IH}$ | $I_{IH}$ = 5 µA | $+V_{BD}$–1 | | $+V_{BD}$ + 0.3 | V |
| | $V_{IL}$ | $I_{IL}$ = 5 µA | 0.3 | | 0.8 | V |
| | $V_{OH}$ | $I_{OH}$ = 2 TTL loads | $+V_{BD}$–0.6 | | $+V_{BD}$ | V |
| | $V_{OL}$ | $I_{OL}$ = 2 TTL loads | 0 | | 0.4 | V |
| **MULTIPLEXER CONTROL PINS** | | | | | | |
| Logic Family - CMOS | | | | | | |
| Logic level | $I_{IH}$ | $I_{IH}$ = 5 µA | 2.3 | | +VA +0.3 | V |
| | $I_{IL}$ | $I_{IL}$ = 5 µA | –0.3 | | 0.8 | V |
| **POWER CONTROL PINS** | | | | | | |
| Logic Family - CMOS | | | | | | |
| Logic level | $V_{IH}$ | $I_{IH}$ = 5 µA | 2.3 | | +VA +0.3 | V |
| | $V_{IL}$ | $I_{IL}$ = 5 µA | –0.3 | | 0.8 | V |

(6) Can vary ±20%

## Electrical Characteristics (continued)

$T_A$ = –40°C to 85°C, VCC = 5 V, VEE = –5 V, +VA = 5 V, +VBD = 5 V or 3.3 V, $V_{ref}$ = 4 V, $f_{SAMPLE}$ = 1 MSPS (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **POWER SUPPLY REQUIREMENTS** | | | | | | |
| Power supply voltage | +VBD | | 2.7 | 3.3 | 5.25 | V |
| | +VA | | 4.75 | 5 | 5.25 | V |
| | VCC | | 4.75 | 5 | 7.5 | V |
| | VEE | | –7.5 | –5 | –3 | V |
| ADC driver positive supply (VCC) current (for OP1 and OP2 together) | | VCC = +5, VEE = -5V, CH0 - CH3 p and m inputs shorted to each other and connected to 2V | | 11.65 | | mA |
| ADC driver negative supply ( VEE) current (for OP1 and OP1 together) | | VCC= +5V, CH0 - CH3 p and m inputs shorted to each other and connected to 2V | | 9.6 | | mA |
| +VA supply current, 1-MHz sample rate | | | | 45 | 50 | mA |
| Reference buffer (BUF-REF) supply current (VCC to GND) | | VCC= +5, PD-RBUF = 0, Quiescent current | | 8 | | mA |
| | | VCC = 5, PD-RBUF = 1 (7) | | 10 | | µA |
| **TEMPERATURE RANGE** | | | | | | |
| Operating free-air | | | –40 | | 85 | °C |

(7) PD-RBUF = 1 powers down the reference buffer (BUF-REF), note that it does not 3-state the BUF-REF output.

## 6.6 Timing Requirements, 5 V

All specifications typical at –40°C to 85°C, +VA = +VBD = 5 V (1) (2) (3)

| PARAMETER | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| $t_{(CONV)}$ | Conversion time | | | 650 | ns |
| $t_{(ACQ)}$ | Acquisition time | 320 | | | ns |
| $t_{(HOLD)}$ | Sample capacitor hold time | | | 25 | ns |
| $t_{pd1}$ | $\overline{CONVST}$ low to BUSY high | | | 40 | ns |
| $t_{pd2}$ | Propagation delay time, end of conversion to BUSY low | | | 15 | ns |
| $t_{pd3}$ | Propagation delay time, start of convert state to rising edge of BUSY | | | 15 | ns |
| $t_{w1}$ | Pulse duration, $\overline{CONVST}$ low | 40 | | | ns |
| $t_{su1}$ | Setup time, $\overline{CS}$ low to $\overline{CONVST}$ low | 20 | | | ns |
| $t_{w2}$ | Pulse duration, $\overline{CONVST}$ high | 20 | | | ns |
| | $\overline{CONVST}$ falling edge jitter | | | 10 | ps |
| $t_{w3}$ | Pulse duration, BUSY signal low | $t_{(ACQ)}$min | | | ns |
| $t_{w4}$ | Pulse duration, BUSY signal high | | | 650 | ns |
| $t_{h1}$ | Hold time, first data bus transition ($\overline{RD}$ low, or $\overline{CS}$ low for read cycle, or BYTE or BUS18/$\overline{16}$ input changes) after $\overline{CONVST}$ low | 40 | | | ns |
| $t_{d1}$ | Delay time, $\overline{CS}$ low to $\overline{RD}$ low | 0 | | | ns |
| $t_{su2}$ | Setup time, $\overline{RD}$ high to $\overline{CS}$ high | 0 | | | ns |
| $t_{w5}$ | Pulse duration, $\overline{RD}$ low | 50 | | | ns |
| $t_{en}$ | Enable time, $\overline{RD}$ low (or $\overline{CS}$ low for read cycle) to data valid | | | 20 | ns |
| $t_{d2}$ | Delay time, data hold from $\overline{RD}$ high | 5 | | | ns |
| $t_{d3}$ | Delay time, BUS18/$\overline{16}$ or BYTE rising edge or falling edge to data valid | 10 | | 20 | ns |
| $t_{w6}$ | Pulse duration, $\overline{RD}$ high | 20 | | | ns |
| $t_{w7}$ | Pulse duration, $\overline{CS}$ high | 20 | | | ns |
| $t_{h2}$ | Hold time, last $\overline{RD}$ (or $\overline{CS}$ for read cycle ) rising edge to $\overline{CONVST}$ falling edge | 50 | | | ns |
| $t_{pd4}$ | Propagation delay time, BUSY falling edge to next $\overline{RD}$ (or $\overline{CS}$ for read cycle) falling edge | 0 | | | ns |
| $t_{d4}$ | Delay time, BYTE edge to BUS18/$\overline{16}$ edge skew | 0 | | | ns |
| $t_{su3}$ | Setup time, BYTE or BUS18/$\overline{16}$ transition to $\overline{RD}$ falling edge | 10 | | | ns |
| $t_{h3}$ | Hold time, BYTE or BUS18/$\overline{16}$ transition to $\overline{RD}$ falling edge | 10 | | | ns |
| $t_{dis}$ | Disable time, $\overline{RD}$ high ($\overline{CS}$ high for read cycle) to 3-stated data bus | | | 20 | ns |
| $t_{d5}$ | Delay time, BUSY low to MSB data valid delay | | | 0 | ns |
| $t_{d6}$ | Delay time, $\overline{CS}$ rising edge to BUSY falling edge | 50 | | | ns |
| $t_{d7}$ | Delay time, BUSY falling edge to $\overline{CS}$ rising edge | 50 | | | ns |
| $t_{su5}$ | BYTE transition setup time, from BYTE transition to next BYTE transition, or BUS18/$\overline{16}$ transition setup time, from BUS18/$\overline{16}$ to next BUS18/$\overline{16}$. | 50 | | | ns |
| $t_{su(ABORT)}$ | Setup time from the falling edge of $\overline{CONVST}$ (used to start the valid conversion) to the next falling edge of $\overline{CONVST}$ (when CS = 0 and $\overline{CONVST}$ are used to abort) or to the next falling edge of $\overline{CS}$ (when $\overline{CS}$ is used to abort). | 60 | | 550 | ns |

(1) All input signals are specified with $t_r = t_f = 5$ ns (10% to 90% of +VBD) and timed from a voltage level of $(V_{IL} + V_{IH})/2$.
(2) See timing diagrams.
(3) All timing are measured with 20 pF equivalent loads on all data bits and BUSY pins.

## 6.7 Timing Requirements, 3 V

All specifications typical at –40°C to 85°C, +VA = 5 V +VBD = 3 V (1) (2) (3)

| PARAMETER | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| $t_{(CONV)}$ | Conversion time | | | 650 | ns |
| $t_{(ACQ)}$ | Acquisition time | 320 | | | ns |
| $t_{(HOLD)}$ | Sample capacitor hold time | | | 25 | ns |
| $t_{pd1}$ | $\overline{CONVST}$ low to BUSY high | | | 40 | ns |
| $t_{pd2}$ | Propagation delay time, end of conversion to BUSY low | | | 25 | ns |
| $t_{pd3}$ | Propagation delay time, start of convert state to rising edge of BUSY | | | 25 | ns |
| $t_{w1}$ | Pulse duration, $\overline{CONVST}$ low | 40 | | | ns |
| $t_{su1}$ | Setup time, $\overline{CS}$ low to $\overline{CONVST}$ low | 20 | | | ns |
| $t_{w2}$ | Pulse duration, CONVST high | 20 | | | ns |
| | $\overline{CONVST}$ falling edge jitter | | | 10 | ps |
| $t_{w3}$ | Pulse duration, BUSY signal low | $t_{(ACQ)}$min | | | ns |
| $t_{w4}$ | Pulse duration, BUSY signal high | | | 650 | ns |
| $t_{h1}$ | Hold time, first data bus transition ($\overline{RD}$ low, or $\overline{CS}$ low for read cycle, or BYTE or BUS18/$\overline{16}$ input changes) after $\overline{CONVST}$ low | 40 | | | ns |
| $t_{d1}$ | Delay time, $\overline{CS}$ low to $\overline{RD}$ low | 0 | | | ns |
| $t_{su2}$ | Setup time, $\overline{RD}$ high to $\overline{CS}$ high | 0 | | | ns |
| $t_{w5}$ | Pulse duration, $\overline{RD}$ low | 50 | | | ns |
| $t_{en}$ | Enable time, $\overline{RD}$ low (or $\overline{CS}$ low for read cycle) to data valid | | | 30 | ns |
| $t_{d2}$ | Delay time, data hold from $\overline{RD}$ high | 5 | | | ns |
| $t_{d3}$ | Delay time, BUS18/$\overline{16}$ or BYTE rising edge or falling edge to data valid | 10 | | 30 | ns |
| $t_{w6}$ | Pulse duration, $\overline{RD}$ high | 20 | | | ns |
| $t_{w7}$ | Pulse duration, $\overline{CS}$ high | 20 | | | ns |
| $t_{h2}$ | Hold time, last $\overline{RD}$ (or $\overline{CS}$ for read cycle ) rising edge to $\overline{CONVST}$ falling edge | 50 | | | ns |
| $t_{pd4}$ | Propagation delay time, BUSY falling edge to next $\overline{RD}$ (or $\overline{CS}$ for read cycle) falling edge | 0 | | | ns |
| $t_{d4}$ | Delay time, BYTE edge to BUS18/$\overline{16}$ edge skew | 0 | | | ns |
| $t_{su3}$ | Setup time, BYTE or BUS18/$\overline{16}$ transition to $\overline{RD}$ falling edge | 10 | | | ns |
| $t_{h3}$ | Hold time, BYTE or BUS18/$\overline{16}$ transition to $\overline{RD}$ falling edge | 10 | | | ns |
| $t_{dis}$ | Disable time, $\overline{RD}$ high ($\overline{CS}$ high for read cycle) to 3-stated data bus | | | 30 | ns |
| $t_{d5}$ | Delay time, BUSY low to MSB data valid delay | | | 0 | ns |
| $t_{d6}$ | Delay time, $\overline{CS}$ rising edge to BUSY falling edge | 50 | | | ns |
| $t_{d7}$ | Delay time, BUSY falling edge to $\overline{CS}$ rising edge | 50 | | | ns |
| $t_{su5}$ | BYTE transition setup time, from BYTE transition to next BYTE transition, or BUS18/$\overline{16}$ transition setup time, from BUS18/$\overline{16}$ to next BUS18/$\overline{16}$. | 50 | | | ns |
| $t_{su(ABORT)}$ | Setup time from the falling edge of $\overline{CONVST}$ (used to start the valid conversion) to the next falling edge of $\overline{CONVST}$ (when CS = 0 and $\overline{CONVST}$ are used to abort) or to the next falling edge of $\overline{CS}$ (when $\overline{CS}$ is used to abort). | 70 | | 550 | ns |

(1) All input signals are specified with $t_r = t_f = 5$ ns (10% to 90% of +VBD) and timed from a voltage level of $(V_{IL} + V_{IH})/2$.
(2) See timing diagrams.
(3) All timing are measured with 20-pF equivalent loads on all data bits and BUSY pins.

## 6.8 Multiplexer Timing Requirements

VCC = 4.75 V to 7.5 V, VEE = -3 V to -7.5 V

| | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| $t_{su6}$ | Setup time C1, C2 or C3 to MXCLK rising edge | | | 600 | ns |
| $t_{d8}$ | Multiplexer and driver settle time ( from MXCLK rising edge to $\overline{CONVST}$ falling edge) | 600 | | | ns |

## 6.9 Timing Diagrams

The ADS8284 is analog system-on-chip (SoC) device. The device includes a multiplexer, a differential input/differential output ADC driver and differential input high-performance ADC, an additional internal reference, a buffered reference output, and a REF/2 output.

Figure 1 shows the basic operation of the device (including all elements). Subsequent sections describe the detailed timings of the individual blocks of the device (primarily the multiplexer and ADC).

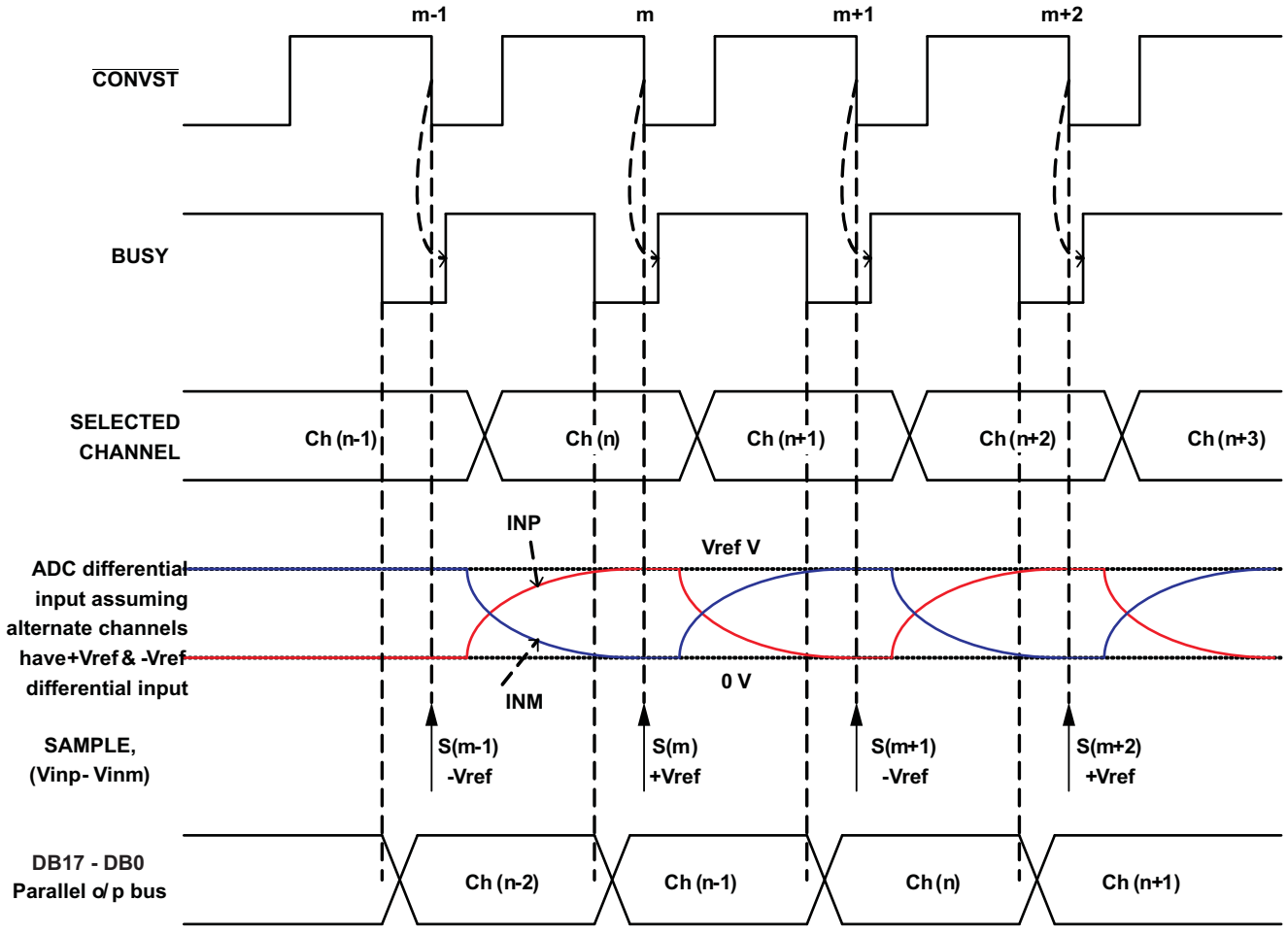


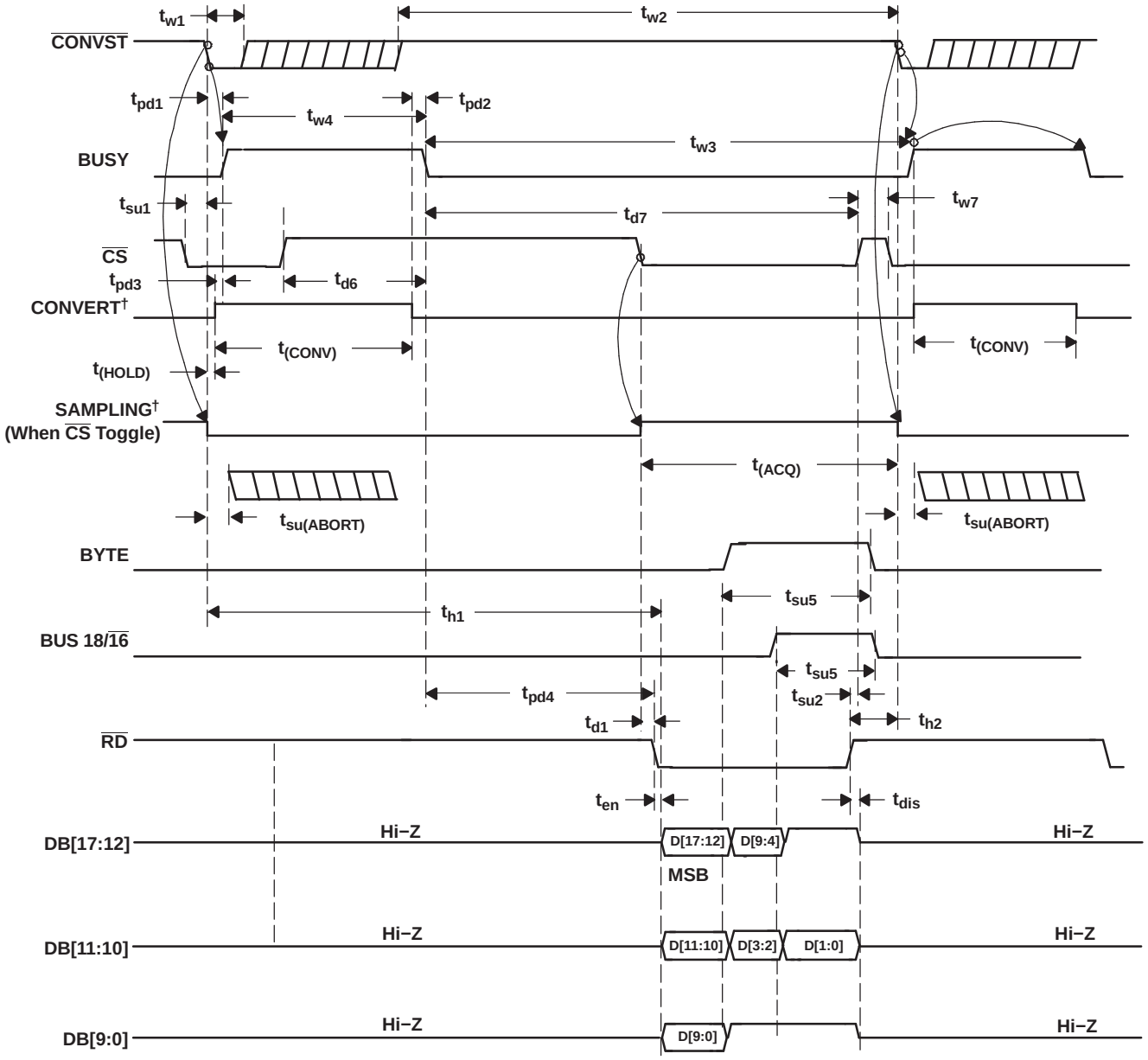

**Figure 1. Device Operation**

As shown in the diagram, the device can be controlled with only one ($\overline{\text{CONVST}}$) digital input. On the falling edge of $\overline{\text{CONVST}}$, the BUSY output of the device goes high. A high level on BUSY indicates the device has sampled the signal and it is converting the sample into its digital equivalent. After the conversion is complete, the BUSY output falls to a logic low level and the device output data corresponding to the recently converted sample is available for reading.

It is recommended (not mandatory) to short the BUSY output of the device to the MXCLK input. The device selects a new channel at every rising edge of MXCLK. The multiplexer is differential. The multiplexer and ADC driver are designed to settle to the 18-bit level before sampling; even at the maximum conversion speed.

**ADC control and timing:** The timing diagrams in this section describe ADC operation; multiplexer operation is described in a later section.

## Timing Diagrams (continued)




†Signal internal to device

**Figure 2. Timing for Conversion and Acquisition Cycles with $\overline{CS}$ and $\overline{RD}$ Toggling**

## Timing Diagrams (continued)

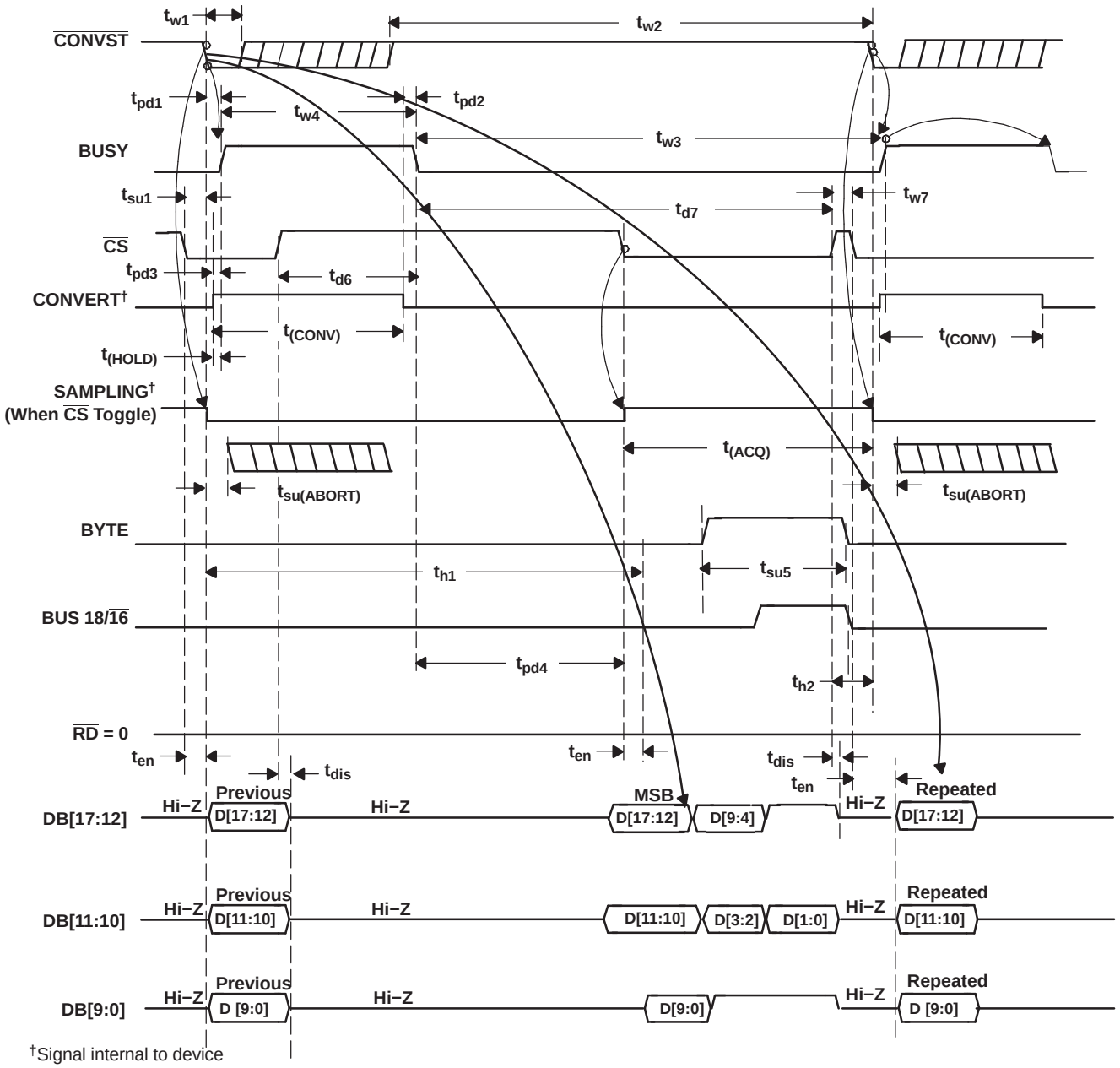
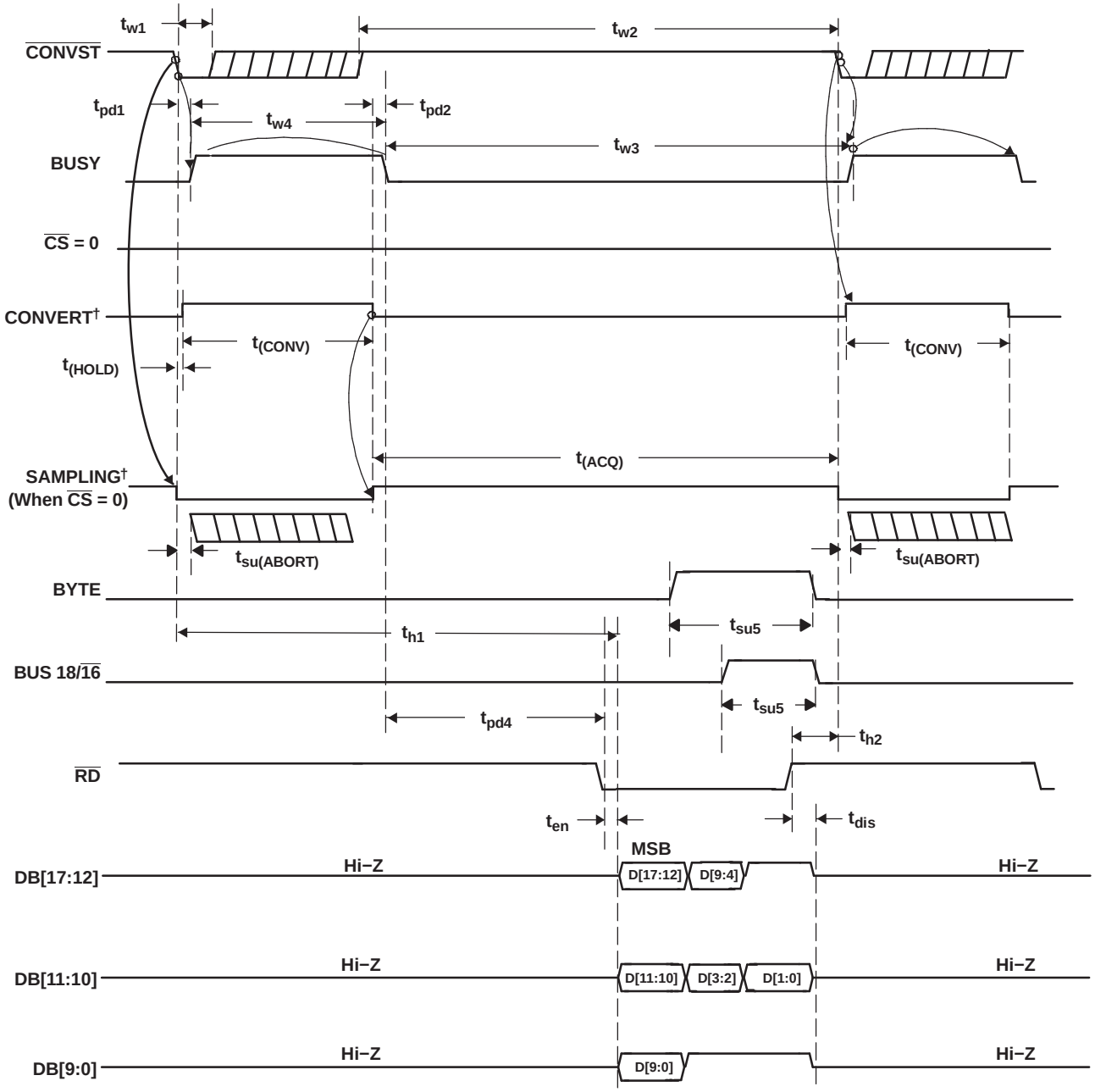



**Figure 3. Timing for Conversion and Acquisition Cycles with $\overline{CS}$ Toggling, $\overline{RD}$ Tied to BDGND**

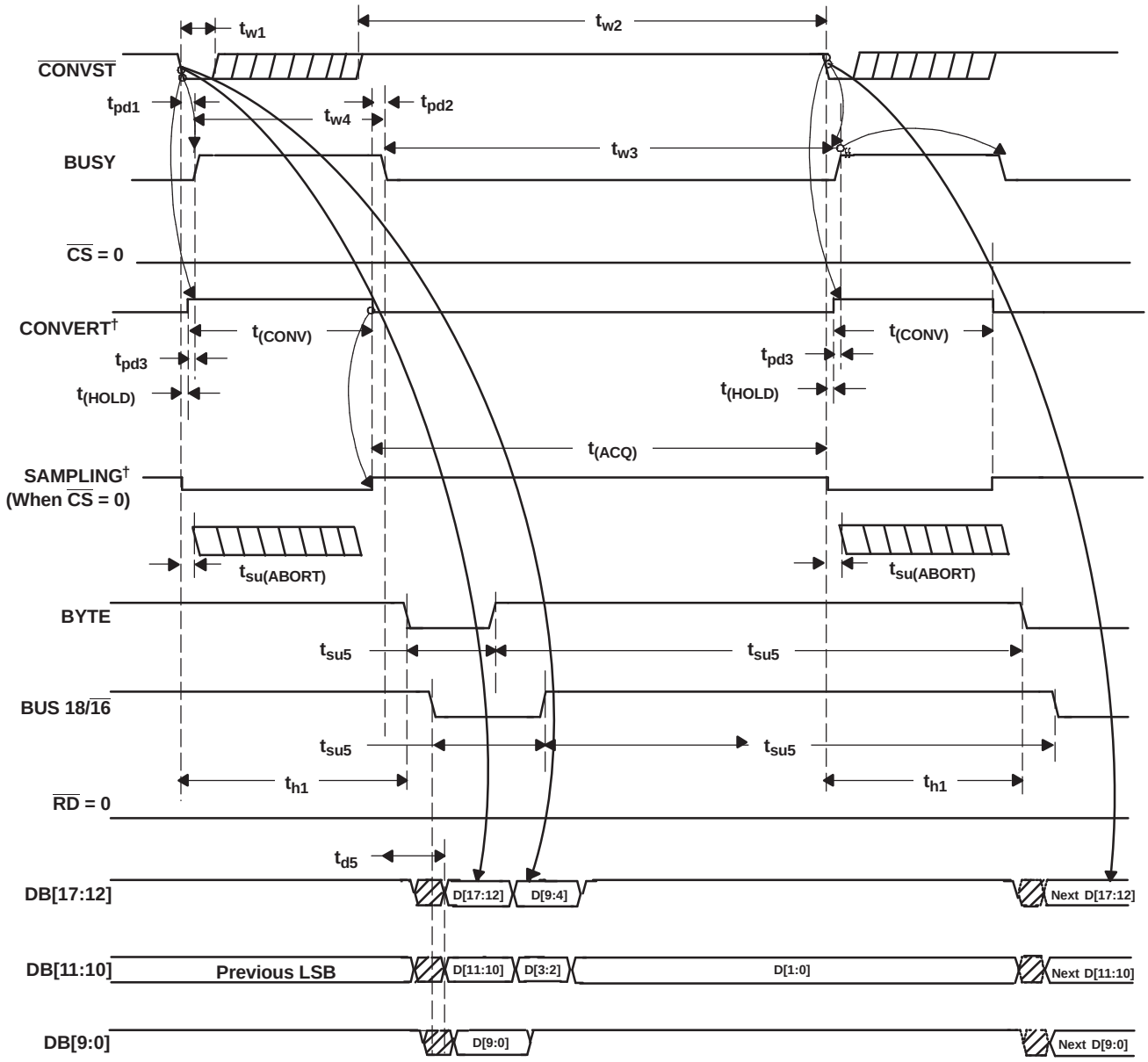
## Timing Diagrams (continued)




†Signal internal to device

**Figure 4. Timing for Conversion and Acquisition Cycles With $\overline{CS}$ Tied to BDGND, $\overline{RD}$ Toggling**

## Timing Diagrams (continued)




†Signal internal to device

**Figure 5. Timing for Conversion and Acquisition Cycles With $\overline{CS}$ and $\overline{RD}$ Tied to BDGND - Auto Read**

## Timing Diagrams (continued)

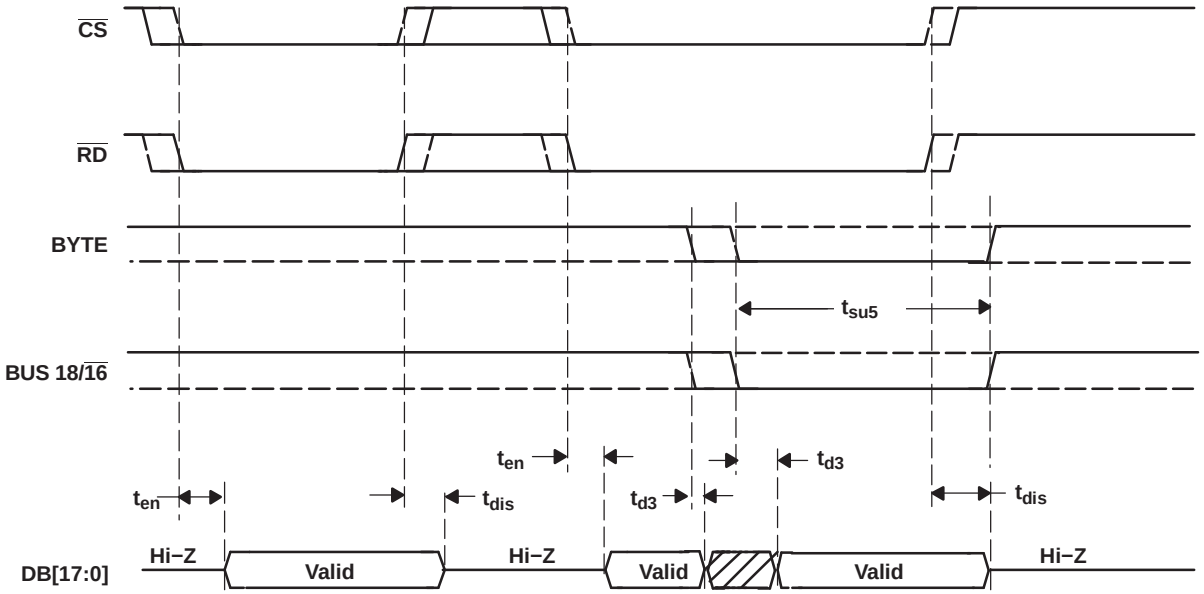



**Figure 6. Detailed Timing for Read Cycles**

**Multiplexer:** The multiplexer has two modes of sequencing namely auto sequencing and manual sequencing. Multiplexer mode selection and operation is controlled with the AUTO, C1, C2, C3, and MXCLK pin.

**Auto sequencing:** A logic one level on the AUTO pin selects auto sequencing mode. It is possible to select the number of channels to be scanned (always starting from channel zero) in auto sequencing mode. Pins C1 and C2 select the channel count (last channel in the auto sequence).

On every rising edge of MXCLK while C3 is at the logic zero level, the next higher channel (in ascending order) is selected. Channel selection rolls over to channel zero on the rising edge of MXCLK after channel selection reaches the *channel count* (last channel in the auto sequence selected by pins C1and C2).

Any time during the sequence the channel sequence can be reset to channel zero. A rising edge on MXCLK while C3 is at the logic one level resets channel selection to channel zero.

**Table 1. Channel Selection in Auto Mode**

| CHANNEL COUNT PINS | | | CLOCK PIN | LAST CHANNEL IN SEQUENCE | CHANNEL SEQUENCE |
|---|---|---|---|---|---|
| C3 | C2 | C1 | MXCLK | | |
| 0 | 0 | 0 | ↑ | 0 | 0,0,0,0.. |
| 0 | 0 | 1 | ↑ | 1 | 0,1,0,1,.. |
| 0 | 1 | 0 | ↑ | 2 | 0,1,2,0,1,2,0… |
| 0 | 1 | 1 | ↑ | 3 | 0,1,2,3,0,1,2,3,0… |
| 1 | X | X | ↑ | X | n → 0 (channel reset to zero) |

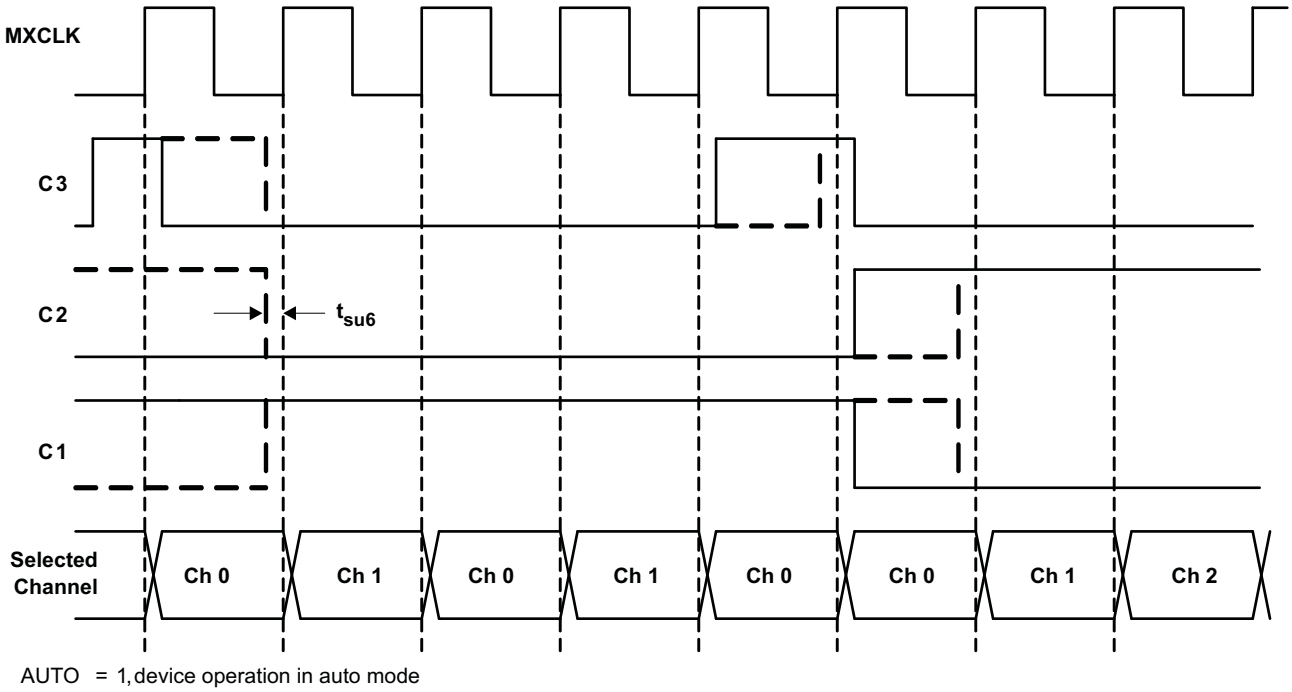



**Figure 7. Multiplexer Auto Mode Timing Diagram**

**Manual sequencing:** A logic zero level on the AUTO pin selects manual sequencing mode. Pins C1and C2 set the channel address. On the rising edge of MXCLK, the addressed channel is connected to the ADC driver input.

**Table 2. Channel Selection in Manual Mode**

| MODE | CHANNEL ADDRESS PINS | | | CLOCK PIN | CHANNEL |
|---|---|---|---|---|---|
| AUTO | C3 | C2 | C1 | MXCLK | |
| 0 | X | 0 | 0 | ↑ | 0 |
| 0 | X | 0 | 1 | ↑ | 1 |
| 0 | X | 1 | 0 | ↑ | 2 |
| 0 | X | 1 | 1 | ↑ | 3 |

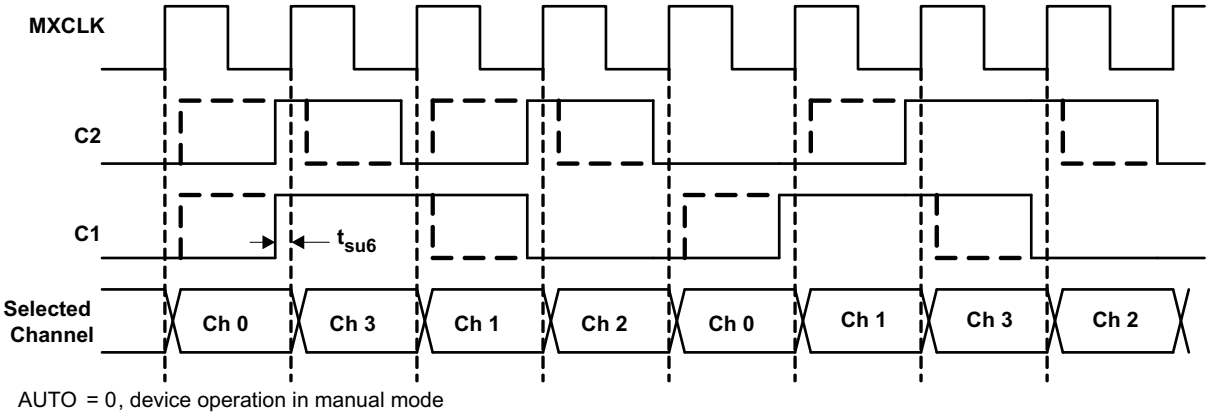



**Figure 8. Multiplexer Manual Mode Timing Diagram**

## 6.10 Typical Characteristics

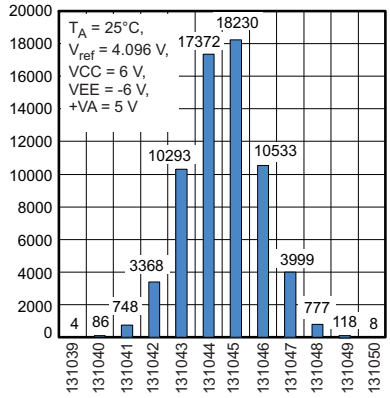



**Figure 9. DC Histogram (CH0 without mux switching)**

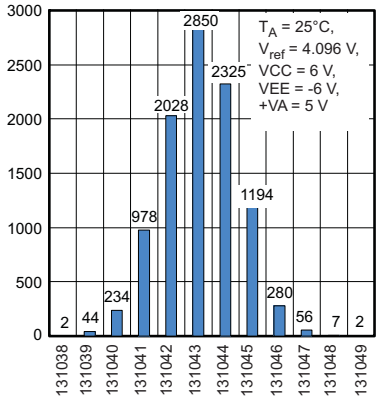



**Figure 10. DC Histogram (CH0 with mux switching, CH 0-1-0)**

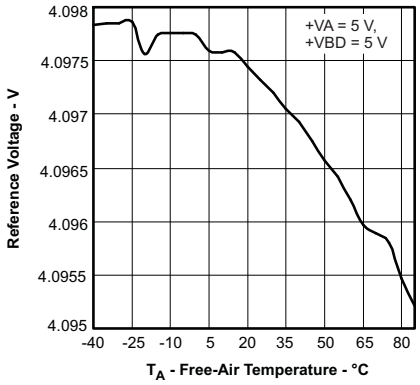



**Figure 11. Internal Reference Voltage vs Free-air Temperature**

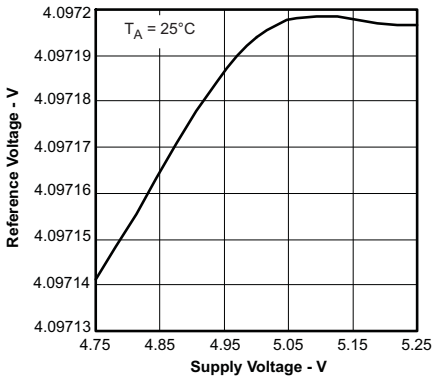



**Figure 12. Internal Reference Voltage vs SI Voltage**

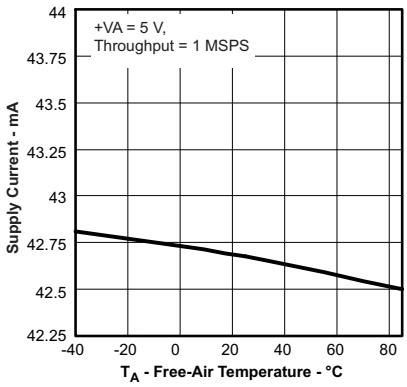



**Figure 13. Analog Voltage (+VA) Supply Current (IA) vs Free-air Temperature**

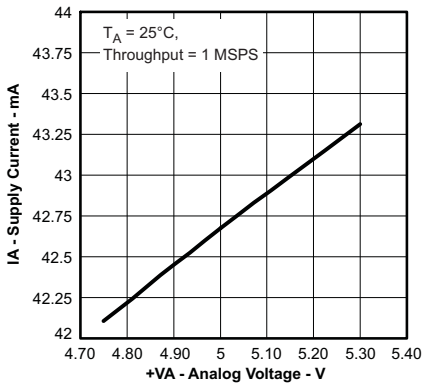



**Figure 14. Supply Current (IA) vs Analog Voltage (+VA)**

## Typical Characteristics (continued)

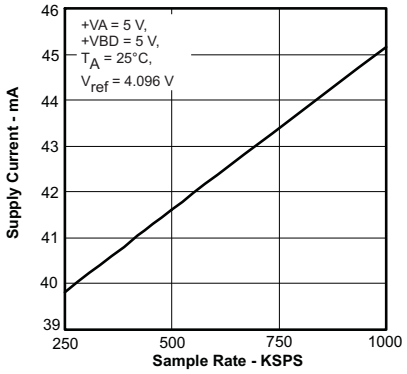



**Figure 15. Analog Supply Current vs Sample Rate**

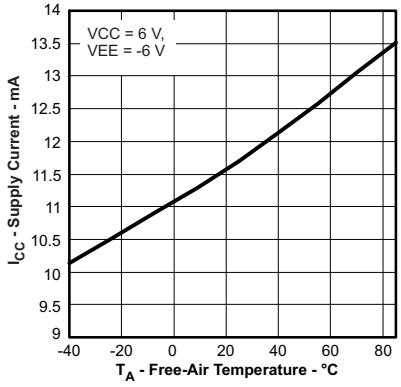



**Figure 16. OPA Positive Supply Current ($I_{CC}$) vs Free-air Temperature**

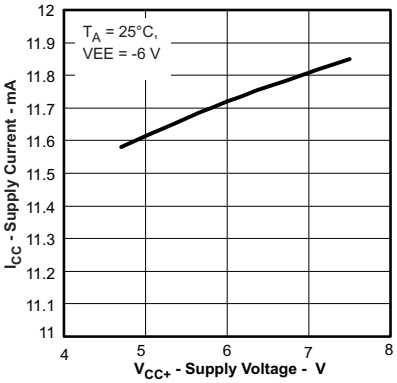



**Figure 17. OPA Positive Supply Current ($I_{CC}$) vs OPA Positive Supply Voltage (+VCC)**

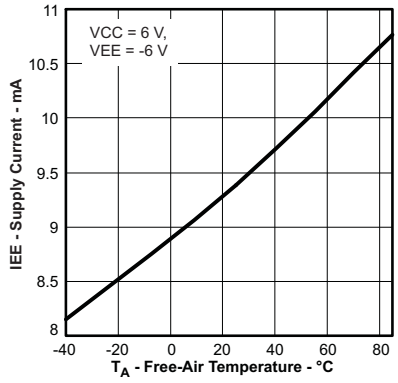



**Figure 18. OPA -VE Supply Current (IEE) vs Free-air Temperature**

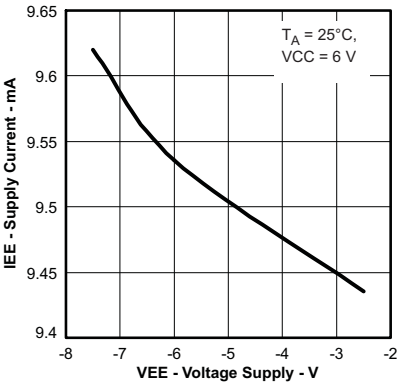



**Figure 19. OPA Negative Supply Current (IEE) vs OPA Negative Supply Voltage (-VEE)**

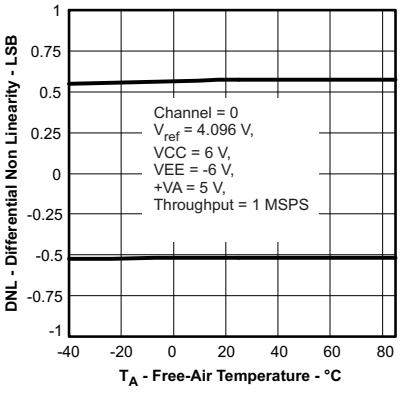



**Figure 20. Differential Nonlinearity vs Free-air Temperature**

## Typical Characteristics (continued)

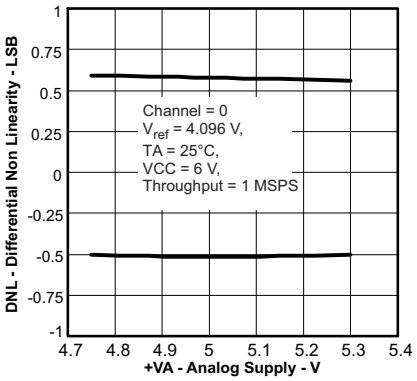



**Figure 21. Differential Nonlinearity vs Analog Supply Voltage (+VA)**

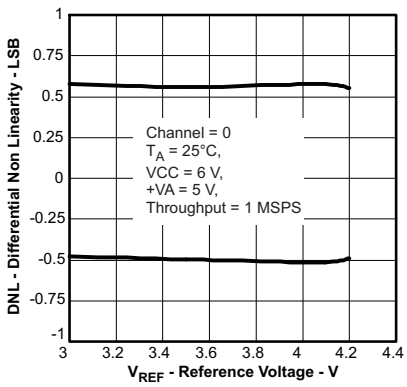



**Figure 22. Differential Nonlinearity vs Reference Voltage**

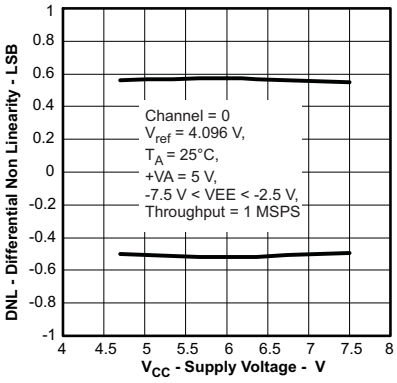



**Figure 23. Differential Nonlinearity vs OPA Supply Voltage (VCC)**

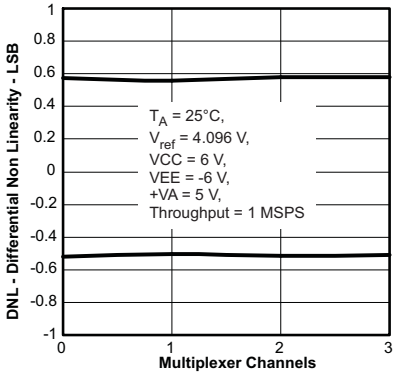



**Figure 24. Differential Nonlinearity vs Multiplexer Channels**

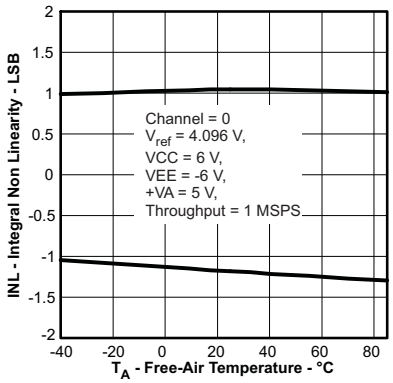



**Figure 25. Integral Nonlinearity vs Free-air Temperature**

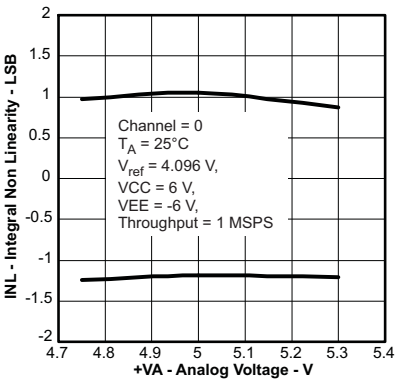



**Figure 26. Integral Nonlinearity vs Analog Supply Voltage (+VA)**

## Typical Characteristics (continued)

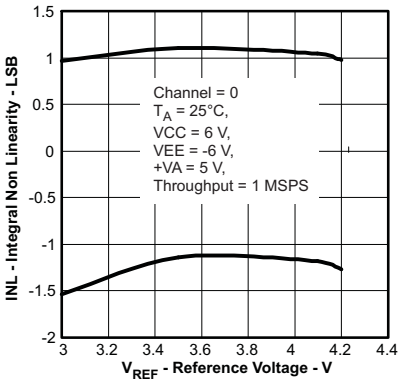



**Figure 27. Integral Nonlinearity vs Reference Voltage**

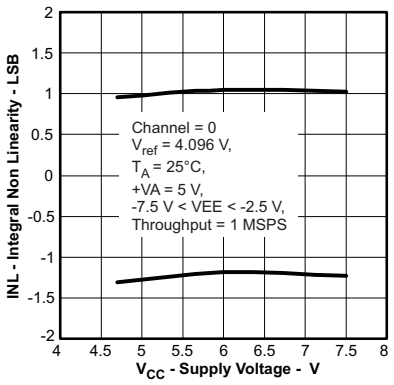



**Figure 28. Integral Nonlinearity vs OPA Supply Voltage (+VCC)**

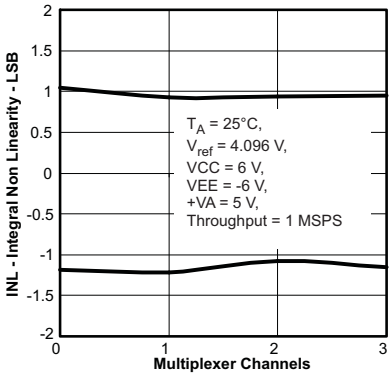



**Figure 29. Integral Nonlinearity vs Multiplexer Channels**

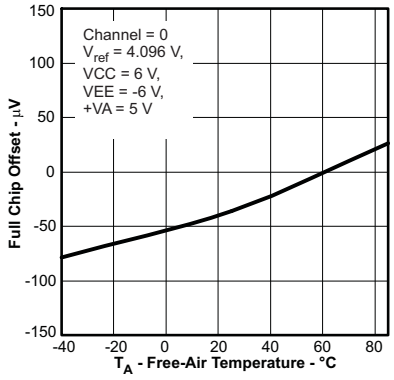



**Figure 30. Full Chip Offset Error vs Free-air Temperature**

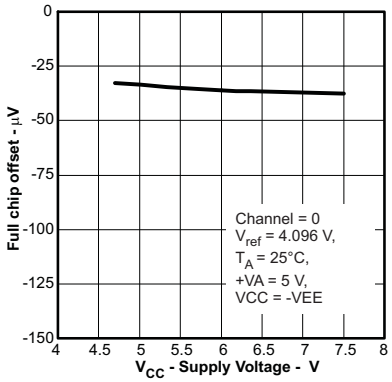



**Figure 31. Full Chip Offset Error vs OPA Supply Voltage (VCC)**

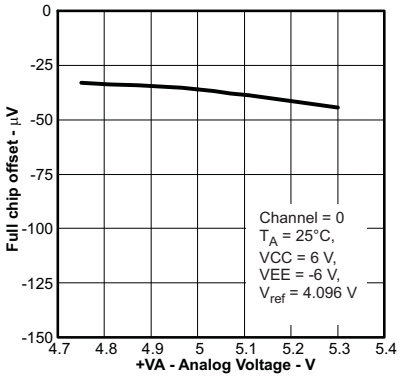



**Figure 32. Full Chip Offset Error vs Analog Supply Voltage (+VA)**

## Typical Characteristics (continued)

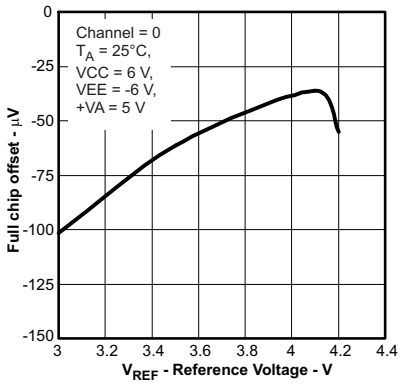



**Figure 33. Full Chip Offset Error vs Reference Voltage**

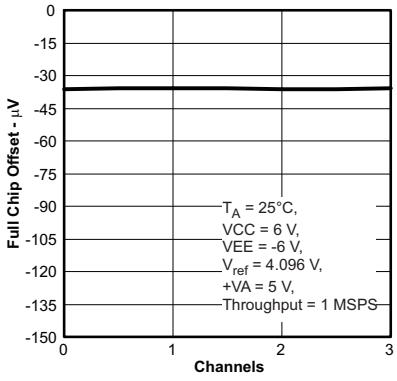



**Figure 34. Full Chip Offset Error vs Channel**

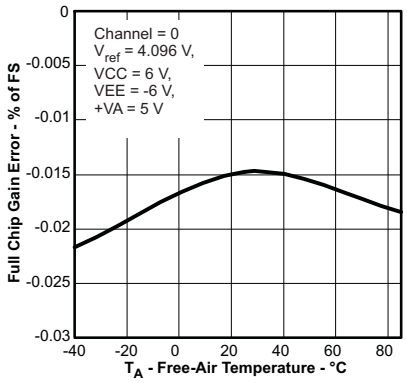



**Figure 35. Full Chip Gain Error vs Free-air Temperature**

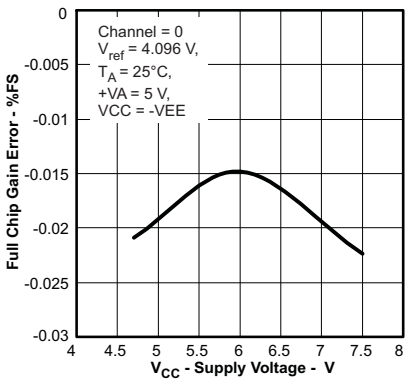



**Figure 36. Full Chip Gain Error vs OPA Supply Voltage (VCC)**

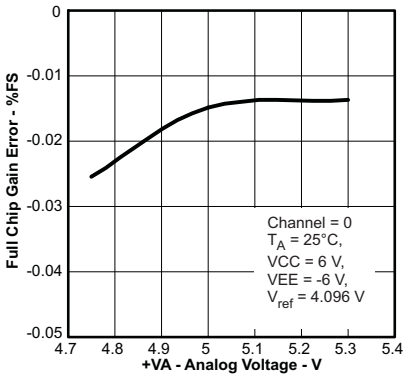



**Figure 37. Full Chip Gain Error vs Analog Supply Voltage (+VA)**

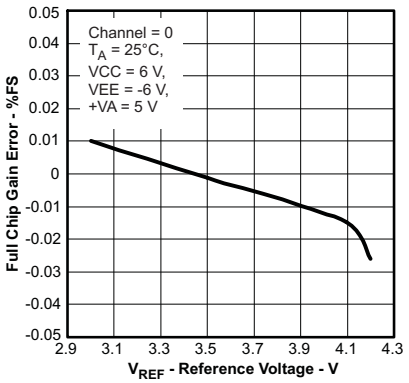



**Figure 38. Full Chip Gain Error vs Reference Voltage**

## Typical Characteristics (continued)

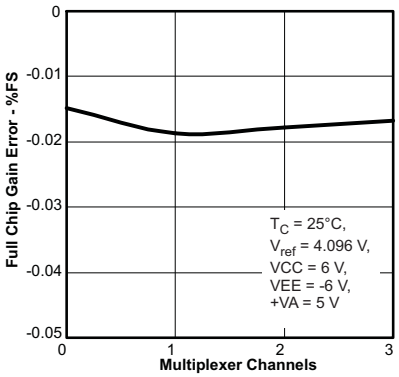



**Figure 39. Full Chip Gain Error vs Multiplexer Channels**

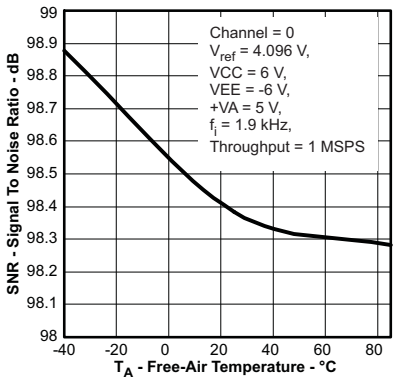



**Figure 40. Signal-To-Noise Ratio vs Free-air Temperature**

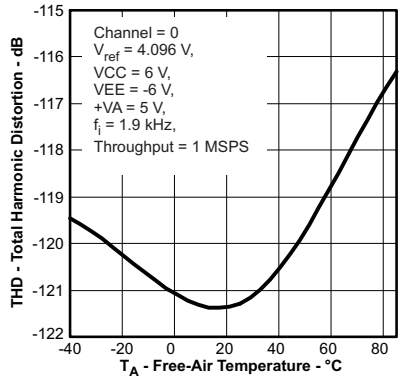



**Figure 41. Total Harmonic Distortion vs Free-air Temperature**

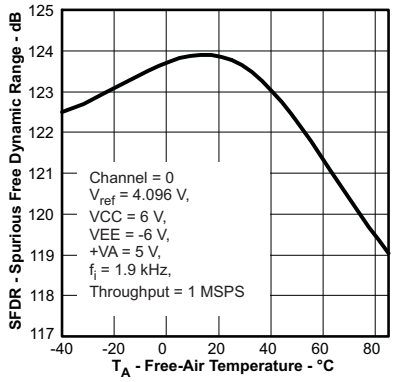



**Figure 42. Spurious Free Dynamic Range vs Free-air Temperature**

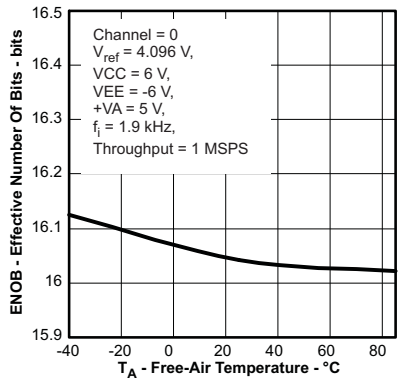



**Figure 43. Effective Number Of Bits vs Free-air Temperature**

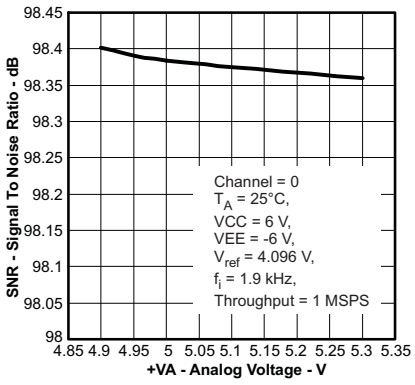



**Figure 44. Signal-To-Noise Ratio vs Analog Supply Voltage (+VA)**

## Typical Characteristics (continued)

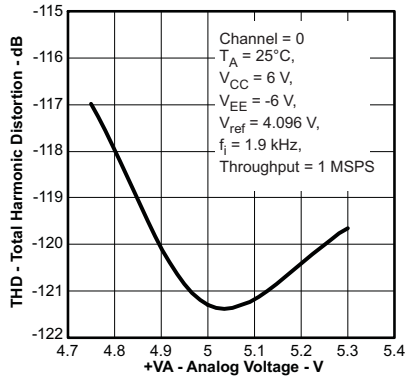



**Figure 45. Total Harmonic Distortion vs Analog Supply Voltage (+VA)**

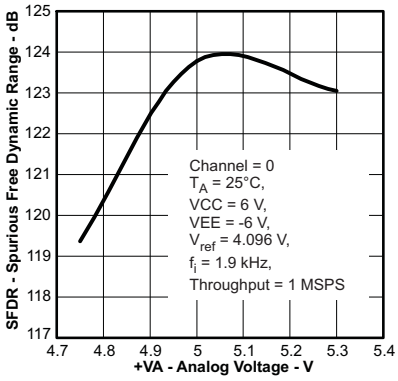



**Figure 46. Spurious Free Dynamic Range vs Analog Supply Voltage (+VA)**

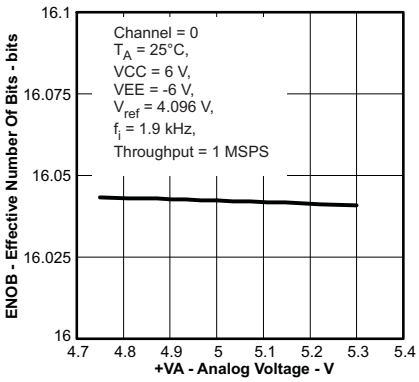



**Figure 47. Effective Number Of Bits vs Analog Supply Voltage (+VA)**

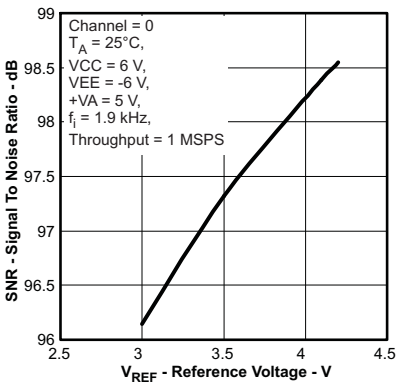



**Figure 48. Signal-To-Noise Ratio vs Reference Voltage**

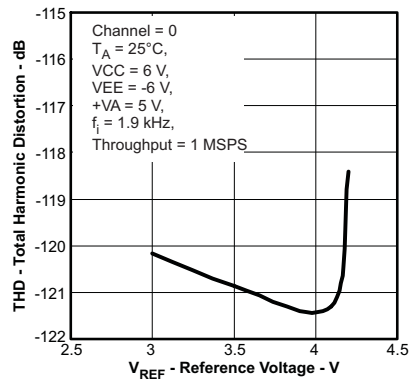



**Figure 49. Total Harmonic Distortion vs Reference Voltage**

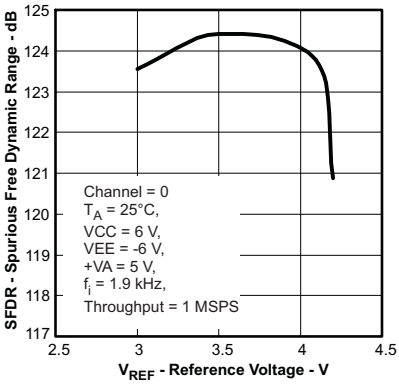



**Figure 50. Spurious Free Dynamic Range vs Reference Voltage**

## Typical Characteristics (continued)

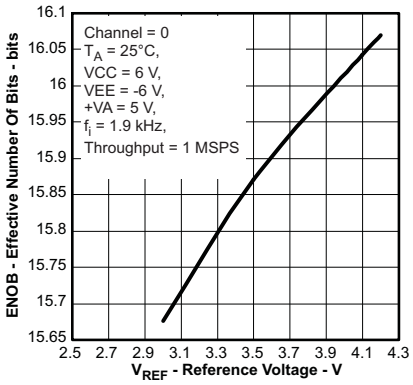



**Figure 51. Effective Number Of Bits vs Reference Voltage**

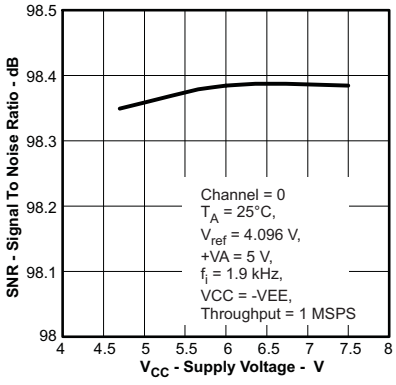



**Figure 52. Signal-To-Noise Ratio vs OPA Supply Voltage (VCC)**

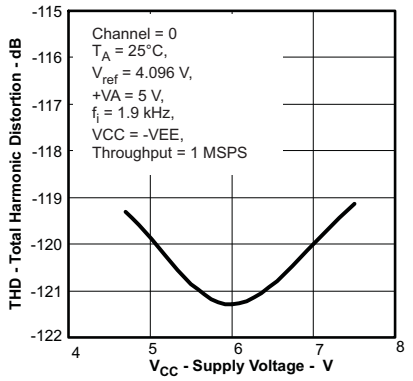



**Figure 53. Total Harmonic Distortion vs OPA Supply Voltage (VCC)**

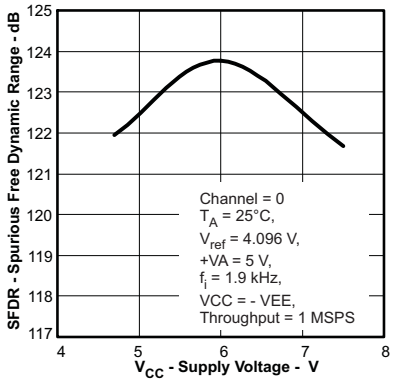



**Figure 54. Spurious Free Dynamic Range vs OPA Supply Voltage (VCC)**

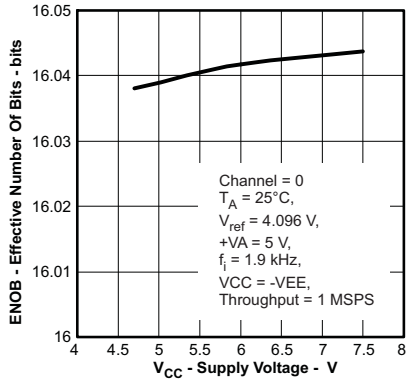



**Figure 55. Effective Number Of Bits vs OPA Supply Voltage (VCC)**

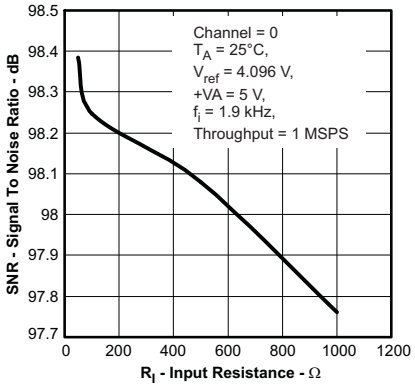



**Figure 56. Signal-To-Noise Ratio vs Source Resistance (RIN)**

## Typical Characteristics (continued)

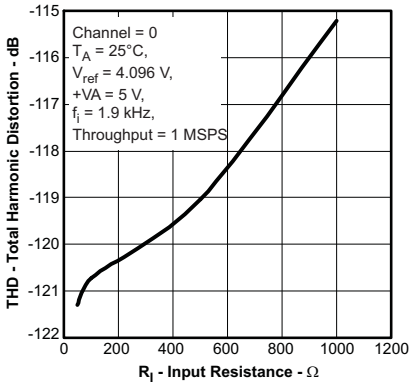



**Figure 57. Total Harmonic Distortion vs Source Resistance (RIN)**

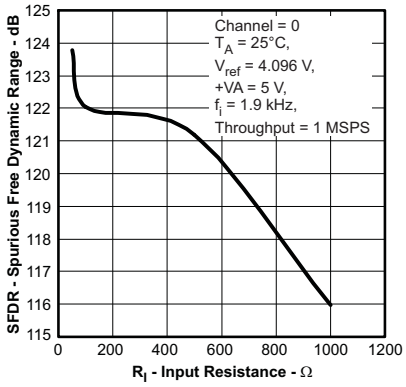



**Figure 58. Spurious Free Dynamic Range vs Source Resistance (RIN)**

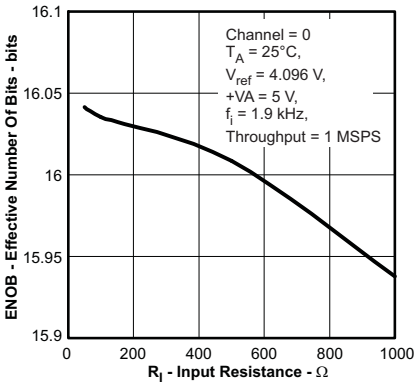



**Figure 59. Effective Number OF Bits vs Source Resistance (RIN)**

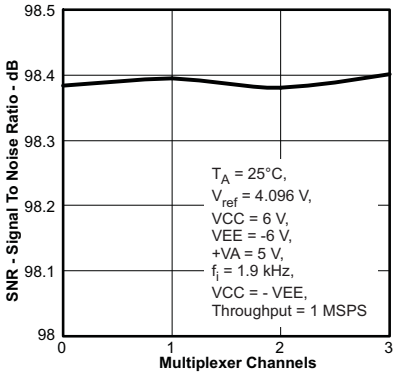



**Figure 60. Signal-To-Noise Ratio vs Multiplexer Channels**

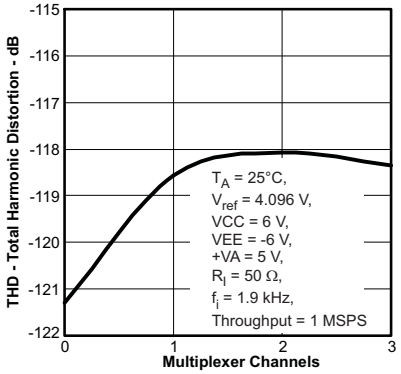



**Figure 61. Total Harmonic Distortion vs Multiplexer Channels**

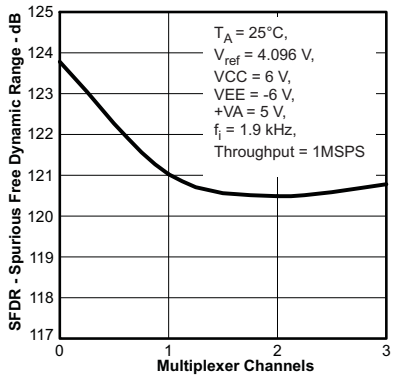



**Figure 62. Spurious Free Dynamic Range vs Multiplexer Channels**

## Typical Characteristics (continued)

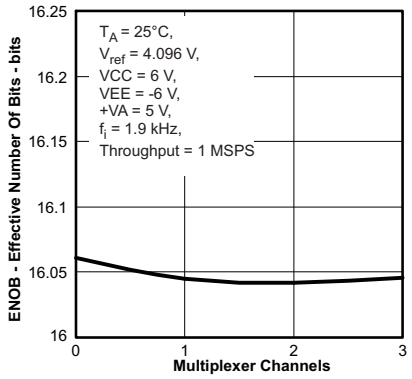



**Figure 63. Effective Number Of Bits vs Multiplexer Channels**

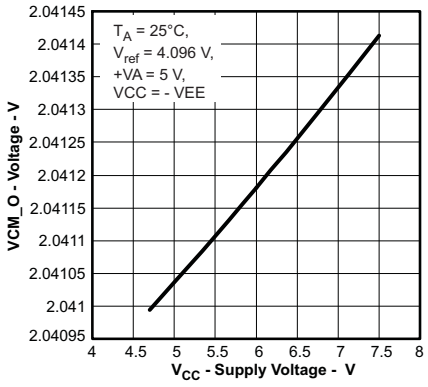



**Figure 64. VCM_O Voltage vs OPA Supply Voltage (VCC)**

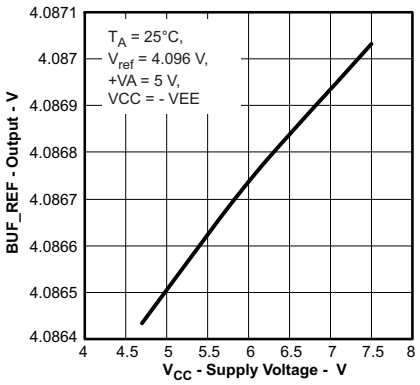
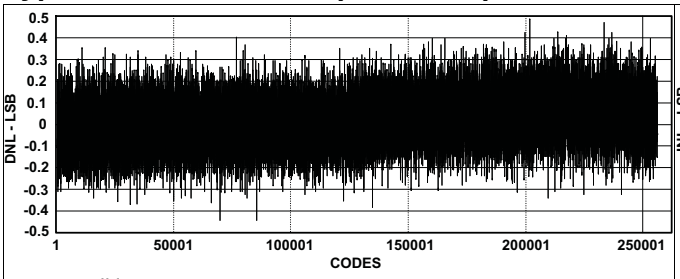


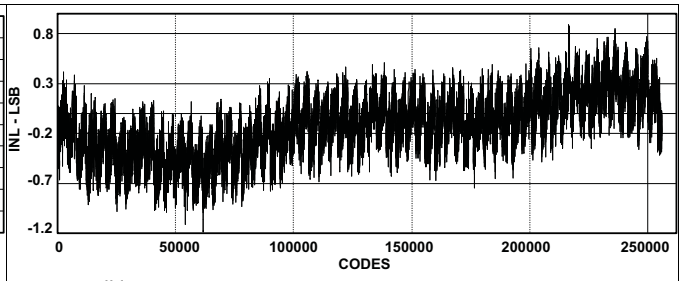

**Figure 65. BUF_REF Output Voltage vs OPA Supply Voltage (VCC)**

## Typical Characteristics (continued)



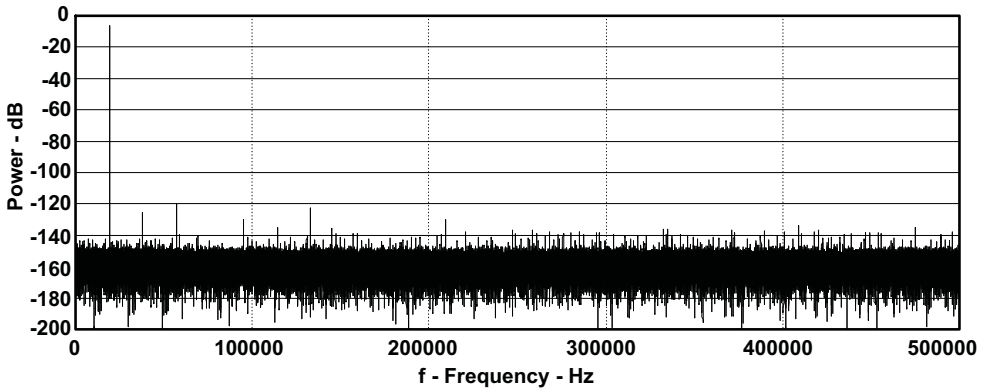

Test conditions: +VA = 5 V, +VBD = 5 V, $T_A$ =25°C, $F_s$ = 1 MSPS, $V_{ref}$ = 4.096 V

**Figure 66. TYPICAL DNL**




Test conditions: +VA = 5 V, +VBD = 5 V, $T_A$ =25°C, $F_s$ = 1 MSPS, $V_{ref}$ = 4.096 V

**Figure 67. TYPICAL INL**




Test conditions: $F_i$ = 19 kHz, $F_s$ = 1 MSPS, $V_{ref}$ = 4.096V, SNR = 97.8 dB, THD = 113 dB, SFDR = 115 dB

**Figure 68. TYPICAL FFT**

# 7 Device Description

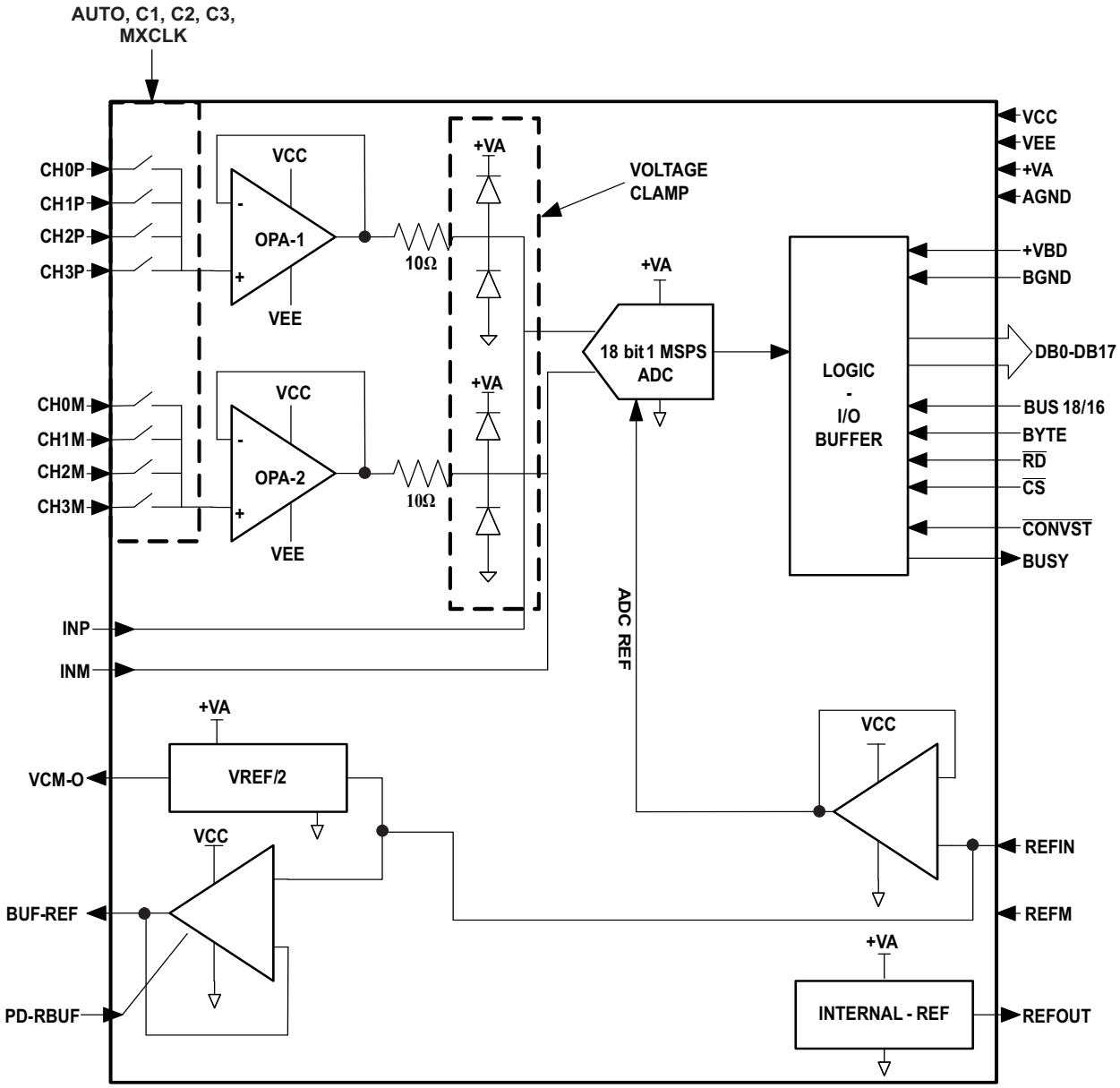
## 7.1 Overview

The ADS8284 features a high-speed successive approximation register (SAR) analog-to-digital converter (ADC). The architecture is based on charge redistribution which inherently includes a sample/hold function. See Figure 73 for the application circuit for the ADS8284.

The conversion clock is generated internally. The conversion time of 650 ns is capable of sustaining a 1 MHz throughput.

The analog input voltage to ADC is provided to two input pins AINP and AINM. When a conversion is initiated, the differential input on these pins is sampled on the internal capacitor array. While a conversion is in progress, both inputs are disconnected from any internal function.

## 7.2 Functional Block Diagram



## 7.3 Feature Description

### 7.3.1 Analog Input

The device features an analog multiplexer, a differential, high input impedance, unity gain ADC driver, and a high performance ADC. Typically alot of care is required for driving circuit component selection and board layout for high resolution ADC driving. However an on-board ADC driver simplifies the job for the user. All that is required is to decouple AINP and AINM with a 1-nF decoupling capacitor across these two pins as close to the device as possible. The multiplexer inputs tolerate source impedance of up to 50 Ω for specified device performance at an operating speed of 1-MSPS. This relaxes constraints on the signal conditioning circuit. In the case of true bipolar input signals, it is possible to condition them with a resister divider as shown in Figure 72. The device permits use of 1.2-kΩ resistors for the divider with effective source impedance of 600 Ω for signal bandwidth less than 10 kHz. A suitable capacitor value used to limit signal bandwidth limits noise coming from the resistor divider network. Care must be taken concerning absolute analog voltage at the multiplexer input pins. This voltage should not exceed VCC and VEE. The clamp at the driver OPA limits the voltage applied to the ADC input.

### 7.3.2 Reference

The ADS8284 can operate with an external reference with a range from 3.0 V to 4.2 V. The reference voltage on the input pin 10 (REFIN) of the converter is internally buffered. A clean, low noise, well-decoupled reference voltage on this pin is required to ensure good performance of the converter. A low noise band-gap reference like the REF5040 can be used to drive this pin. A 0.1-µF decoupling capacitor is required between REFIN and REFM pins (pin 10 and pin 9) of the converter. This capacitor should be placed as close as possible to the pins of the device. Designers should strive to minimize the routing length of the traces that connect the pins of the capacitor to the pins of the converter. An RC network can also be used to filter the reference voltage. A 100-Ω series resistor and a 0.1-µF capacitor, which can also serve as the decoupling capacitor can be used to filter the reference voltage.

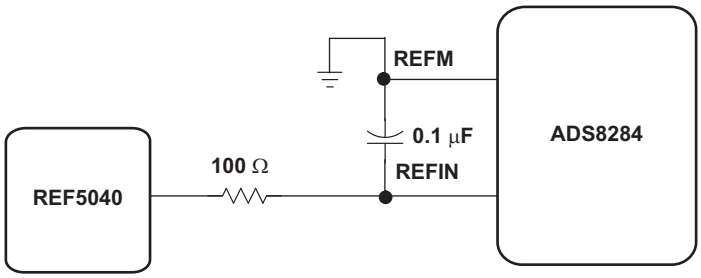



**Figure 69. ADS8284 Using External Reference**

The ADS8284 also has limited low pass filtering capability built into the converter. The equivalent circuitry on the REFIN input is as shown in Figure 70.

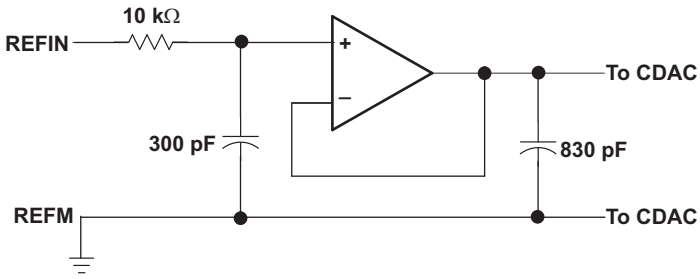



**Figure 70. Simplified Reference Input Circuit**

## Feature Description (continued)

The REFM input of the ADS8284 should always be shorted to AGND. A 4.096-V internal reference is included. When the internal reference is used, pin 11 (REFOUT) is connected to pin 10 (REFIN) with an 0.1-µF decoupling capacitor and 1-µF storage capacitor between pin 11 (REFOUT) and pin 9 ( REFM) (see Figure 74). The internal reference of the converter is double buffered. If an external reference is used, the second buffer provides isolation between the external reference and the CDAC. This buffer is also used to recharge all of the capacitors of the CDAC during conversion (see Figure 70). pin 11 (REFOUT) can be left unconnected (floating) if external reference is used.

## 7.4 Device Functional Modes

### 7.4.1 Reading Data

The ADS8284 outputs full parallel data in straight binary format as shown in Table 3. The parallel output is active when $\overline{CS}$ and $\overline{RD}$ are both low. There is a minimal quiet zone requirement around the falling edge of $\overline{CONVST}$. This is 50 ns prior to the falling edge of $\overline{CONVST}$ and 40 ns after the falling edge. No data read should attempted within this zone. Any other combination of $\overline{CS}$ and $\overline{RD}$ sets the parallel output to 3-state. BYTE and BUS18/$\overline{16}$ are used for multiword read operations. BYTE is used whenever lower bits on the bus are output on the higher byte of the bus. BUS18/$\overline{16}$ is used whenever the last two bits on the 18-bit bus is output on either bytes of the higher 16-bit bus. Refer to Table 3 for ideal output codes.

**Table 3. Ideal Input Voltages and Output Codes**

| DESCRIPTION | ANALOG VALUE | DIGITAL OUTPUT STRAIGHT BINARY | |
|---|---|---|---|
| | | BINARY CODY | HEX CODE |
| Full scale range | 2 × (+$V_{ref}$) | | |
| Least significant bit (LSB) | 2 × (+$V_{ref}$)/262144 | | |
| +Full scale | (+$V_{ref}$) – 1 LSB | 01 1111 1111 1111 1111 | 1FFFF |
| Midscale | 0 V | 00 0000 0000 0000 0000 | 00000 |
| Midscale – 1 LSB | 0 V – 1 LSB | 11 1111 1111 1111 1111 | 3FFFF |
| Zero | –$V_{ref}$ | 10 0000 0000 0000 0000 | 20000 |

The output data is a full 18-bit word (D17–D0) on DB17–DB0 pins (MSB–LSB) if both BUS18/$\overline{16}$ and BYTE are low.

The result may also be read on an 16-bit bus by using only pins DB17–DB2. In this case two reads are necessary: the first as before, leaving both BUS18/$\overline{16}$ and BYTE low and reading the 16 most significant bits (D17–D2) on pins DB17–DB2, then bringing BUS18/$\overline{16}$ high while holding BYTE low. When BUS18/$\overline{16}$ is high, the lower two bits (D1–D0) appear on pins DB3–DB2.

The result may also be read on an 8-bit bus for convenience. This is done by using only pins DB17–DB10. In this case three reads are necessary: the first as before, leaving both BUS18/$\overline{16}$ and BYTE low and reading the 8 most significant bits on pins DB17–DB10, then bringing BYTE high while holding BUS18/$\overline{16}$ low. When BYTE is high, the medium bits (D9–D2) appear on pins DB17–DB10. The last read is done by bringing BUS18/$\overline{16}$ high while holding BYTE high. When BUS18/$\overline{16}$ is high, the lower two bits (D1–D0) appear on pins DB11–DB10. The last read cycle is not necessary if only the first 16 most significant bits are of interest.

All of these multiword read operations can be performed with multiple active $\overline{RD}$ (toggling) or with $\overline{RD}$ held low for simplicity. This is referred to as the AUTO READ operation.

**Table 4. Conversion Data Read Out**

| BYTE | BUS18/$\overline{16}$ | DATA READ OUT | | | | |
|---|---|---|---|---|---|---|
| | | TERMINAS DB17–DB12 | TERMINAS DB11–DB10 | TERMINAS DB9–DB4 | TERMINAS DB3–DB2 | TERMINAS DB1–DB0 |
| High | High | All One's | D1–D0 | All One's | All One's | All One's |
| Low | High | All One's | All One's | All One's | D1–D0 | All One's |
| High | Low | D9–D4 | D3–D2 | All One's | All One's | All One's |
| Low | Low | D17–D12 | D11–D10 | D9–D4 | D3–D2 | D1–D0 |

# 8 Application and Implementation

## 8.1 Application Information

As discussed before, the ADS8284 is 18-bit analog SoC that includes various blocks like a multiplexer, ADC driver, internal reference, internal reference buffer, buffered reference output, and Ref/2 output on-board. The following diagram shows the recommended analog and digital interfacing of the ADS8284.

## 8.2 Typical Applications

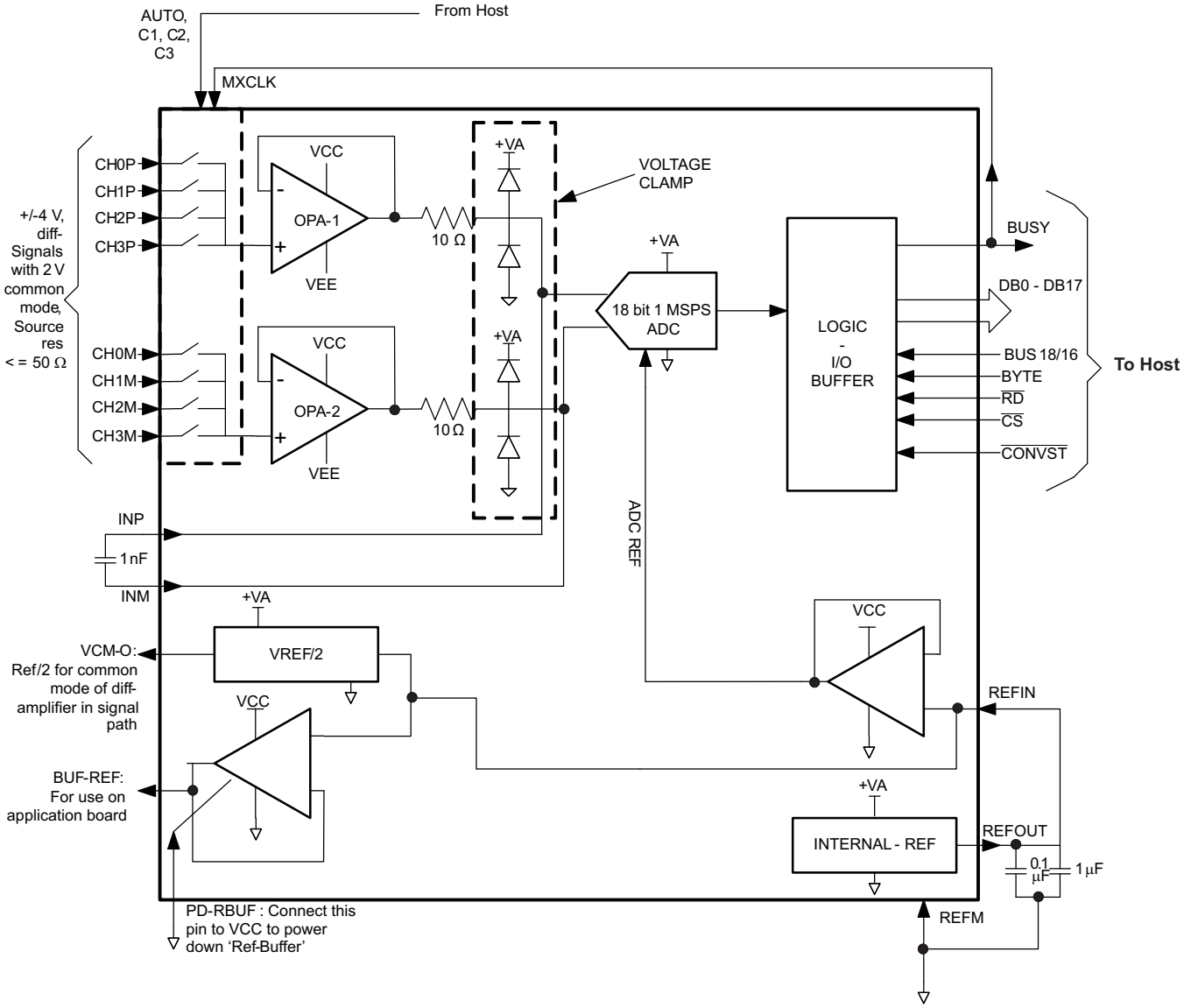
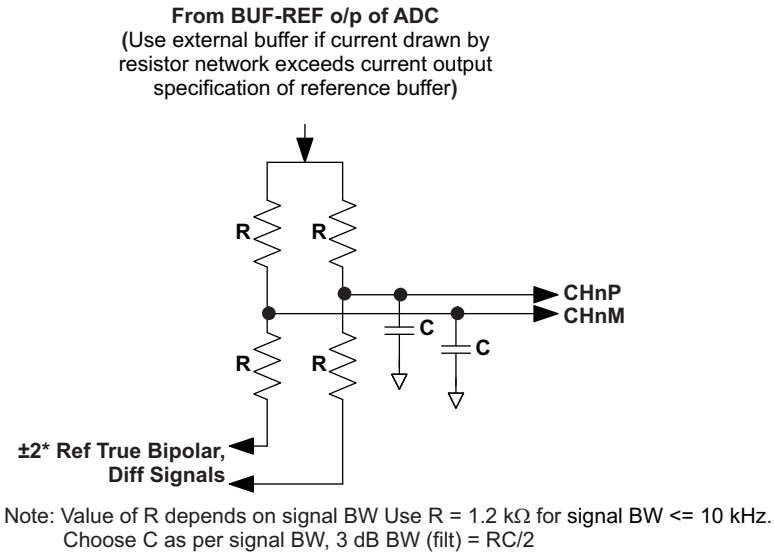



**Figure 71. Analog and Digital Interface Diagram**

## Typical Applications (continued)

As shown in Figure 71, the ADS8284 accepts unipolar differential analog inputs in the range of $\pm V_{ref}$ with a common-mode voltage of $V_{ref}/2$ (0 to $V_{ref}$ at positive input and $V_{ref}$ to 0 at negative input). An application may require the interfacing of true bipolar input signals. Figure 72 shows the conversion of bipolar input signals to unipolar differential signals.




Note: Value of R depends on signal BW Use R = 1.2 kΩ for signal BW <= 10 kHz.
Choose C as per signal BW, 3 dB BW (filt) = RC/2

**Figure 72. Conversion of Bipolar Input Signals to Unipolar Differential Signals**

## Typical Applications (continued)

Figure 73 shows a parallel interface between the ADS8284 and a typical microcontroller using an 8-bit data bus.

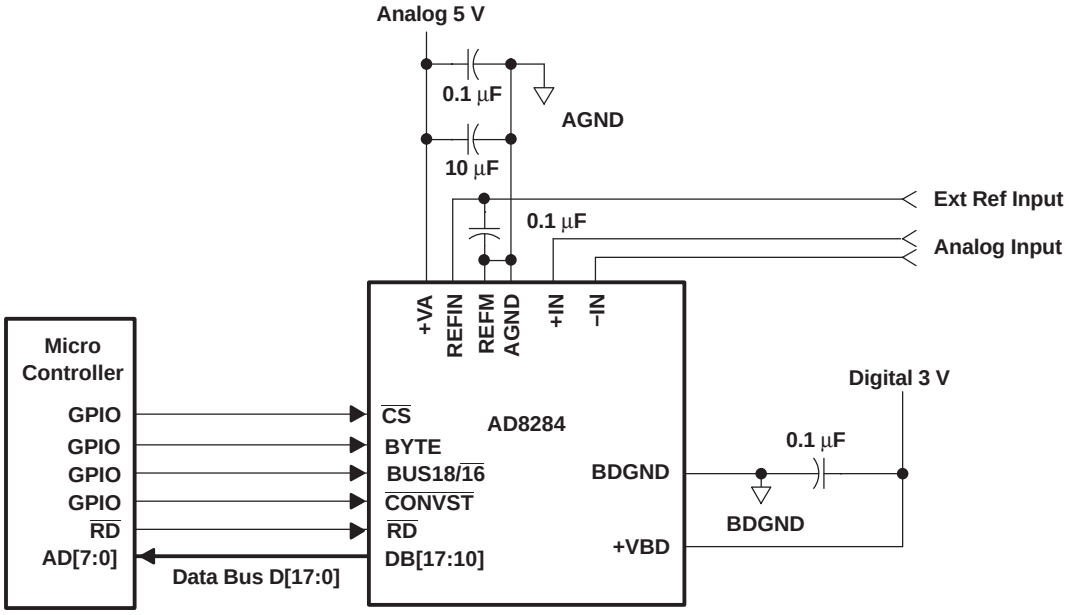



**Figure 73. ADS8284 Application Circuitry**

The BUSY signal is used as a falling edge interrupt to the microcontroller.

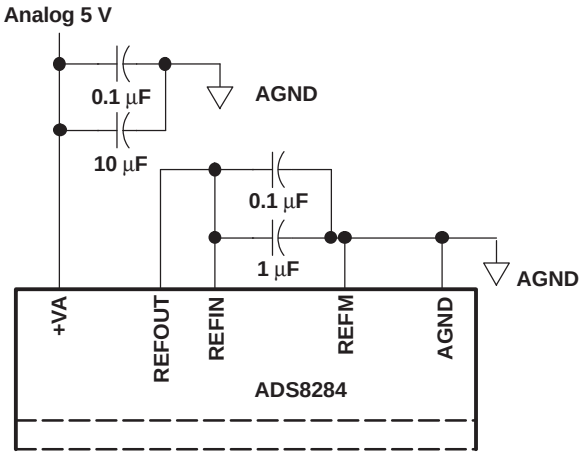



**Figure 74. ADS8284 Using Internal Reference**

# 9 Power Supply Recommendations

**Table 5. Power Recommendations**

| Voltage Supply | MIN | TYP | MAX |
|---|---|---|---|
| VBD | 2.7 V | 3.3 V | 5.25 V |
| VA | 4.75 V | 5 V | 5.25 V |
| VCC | 4.75 V | 5 V | 7.5 V |
| VEE | –7.5 V | –5 V | -3 V |

# 10 Device and Documentation Support

## 10.1 Trademarks

All trademarks are the property of their respective owners.

## 10.2 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

## 10.3 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms and definitions.

# 11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| ADS8284IBRGCR | NRND | VQFN | RGC | 64 | 2000 | Green (RoHS & no Sb/Br) | NIPDAU | Level-3-260C-168 HR | -40 to 85 | ADS8284 B | |
| ADS8284IBRGCT | NRND | VQFN | RGC | 64 | 250 | Green (RoHS & no Sb/Br) | NIPDAU | Level-3-260C-168 HR | -40 to 85 | ADS8284 B | |

**(1)** The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

**(2)** **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

**(3)** MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

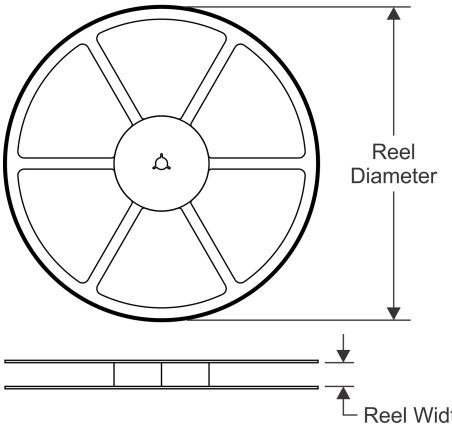
**(4)** There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

**(5)** Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

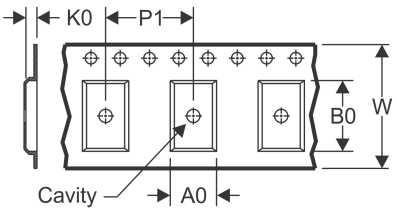
**(6)** Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

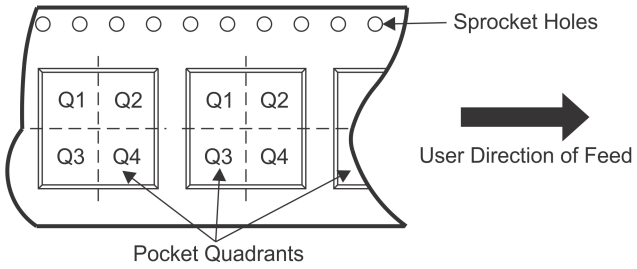



**TAPE DIMENSIONS**




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

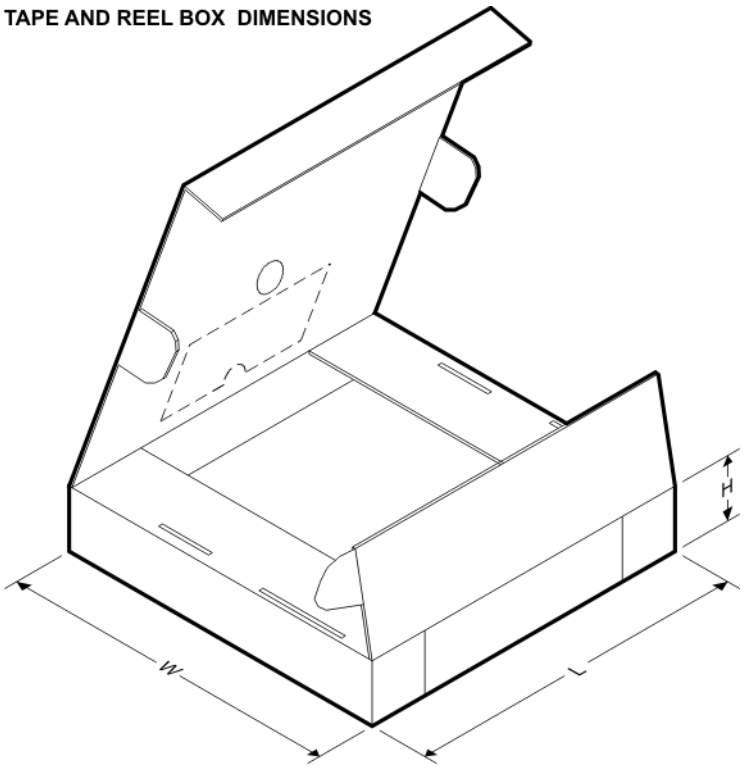
**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| ADS8284IBRGCR | VQFN | RGC | 64 | 2000 | 330.0 | 16.4 | 9.3 | 9.3 | 1.5 | 12.0 | 16.0 | Q2 |
| ADS8284IBRGCT | VQFN | RGC | 64 | 250 | 180.0 | 16.4 | 9.3 | 9.3 | 1.5 | 12.0 | 16.0 | Q2 |

TAPE AND REEL BOX DIMENSIONS




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| ADS8284IBRGCR | VQFN | RGC | 64 | 2000 | 350.0 | 350.0 | 43.0 |
| ADS8284IBRGCT | VQFN | RGC | 64 | 250 | 213.0 | 191.0 | 55.0 |

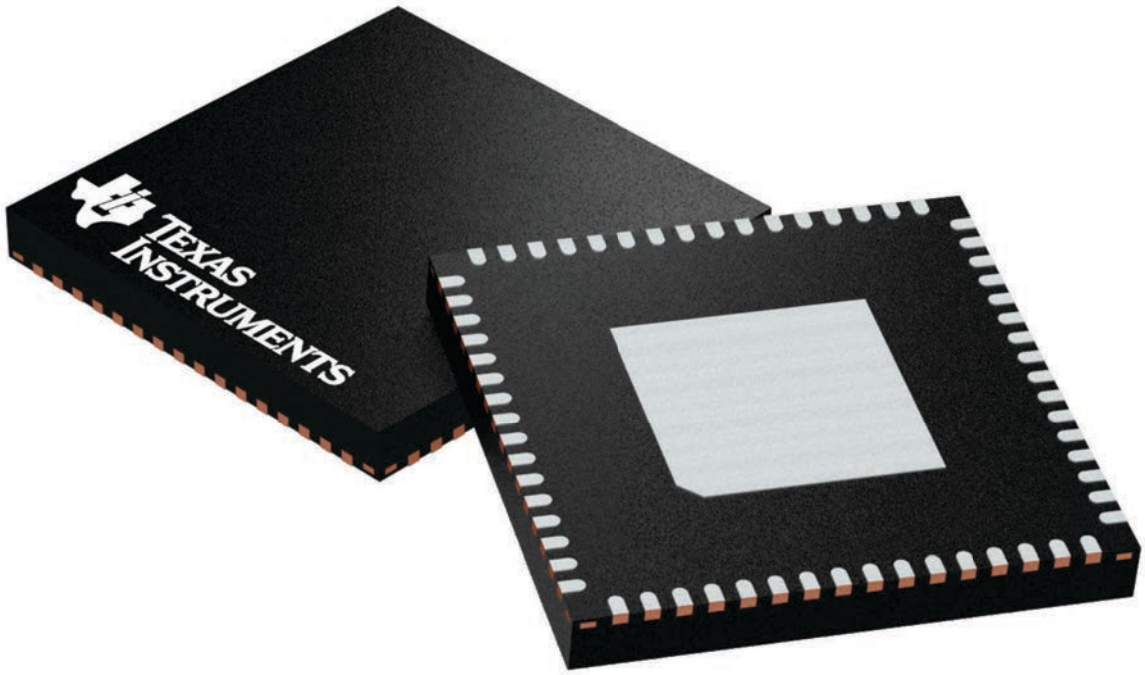
# GENERIC PACKAGE VIEW

## RGC 64

## VQFN - 1 mm max height

**9 x 9, 0.5 mm pitch**

PLASTIC QUAD FLATPACK - NO LEAD




Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

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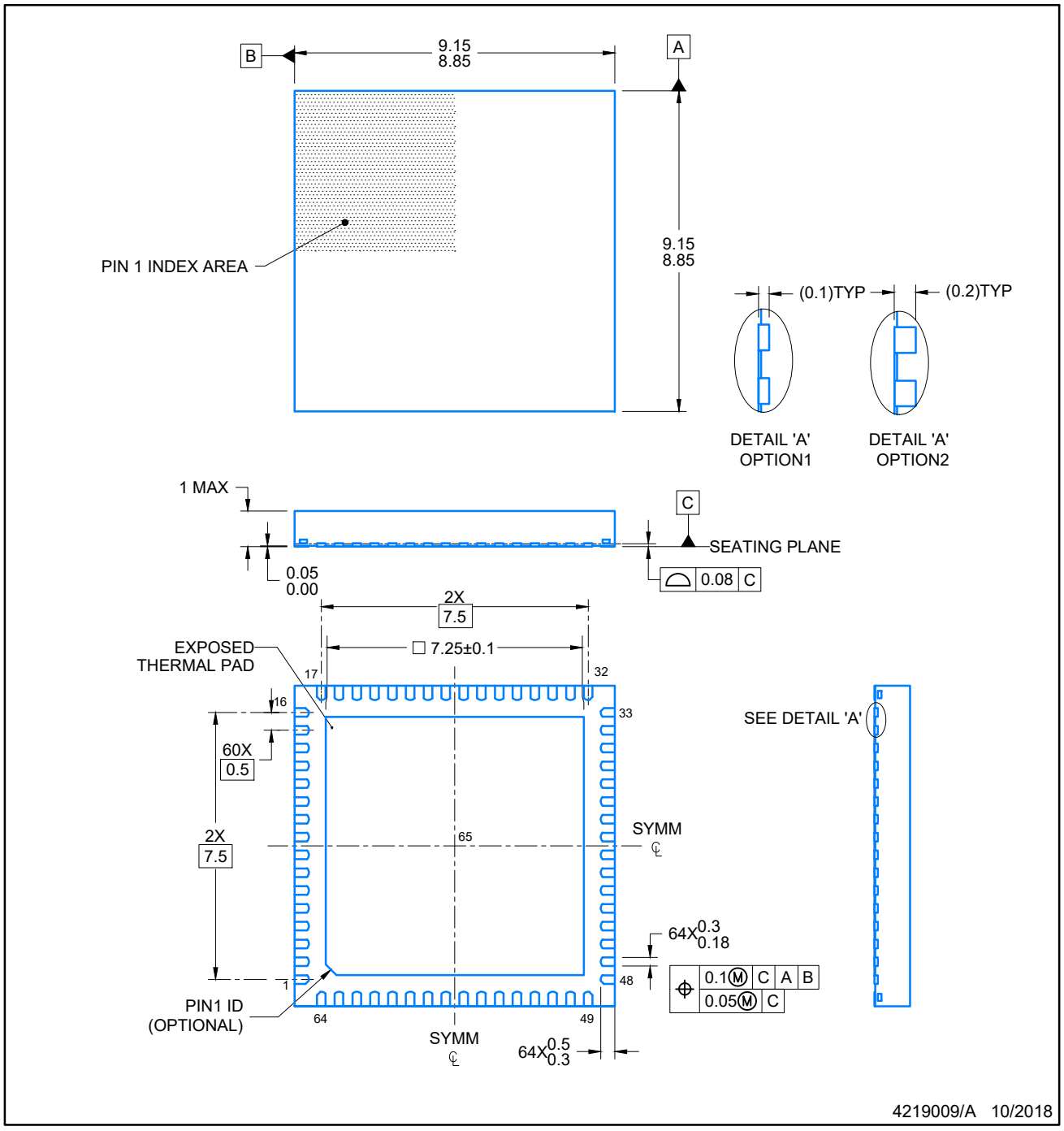
# PACKAGE OUTLINE

## RGC0064A

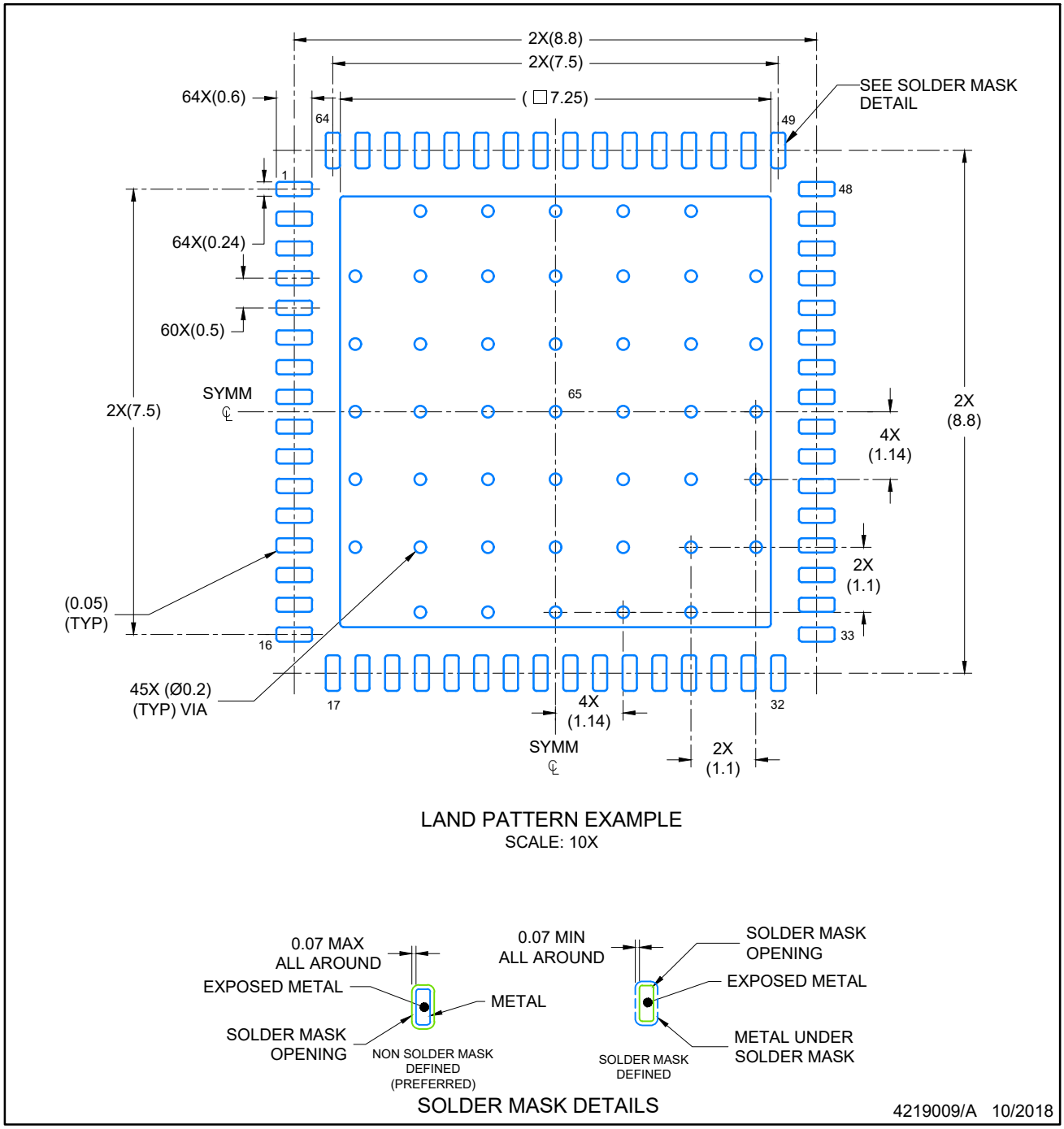
### VQFN - 1 mm max height

PLASTIC QUADFLAT PACK- NO LEAD



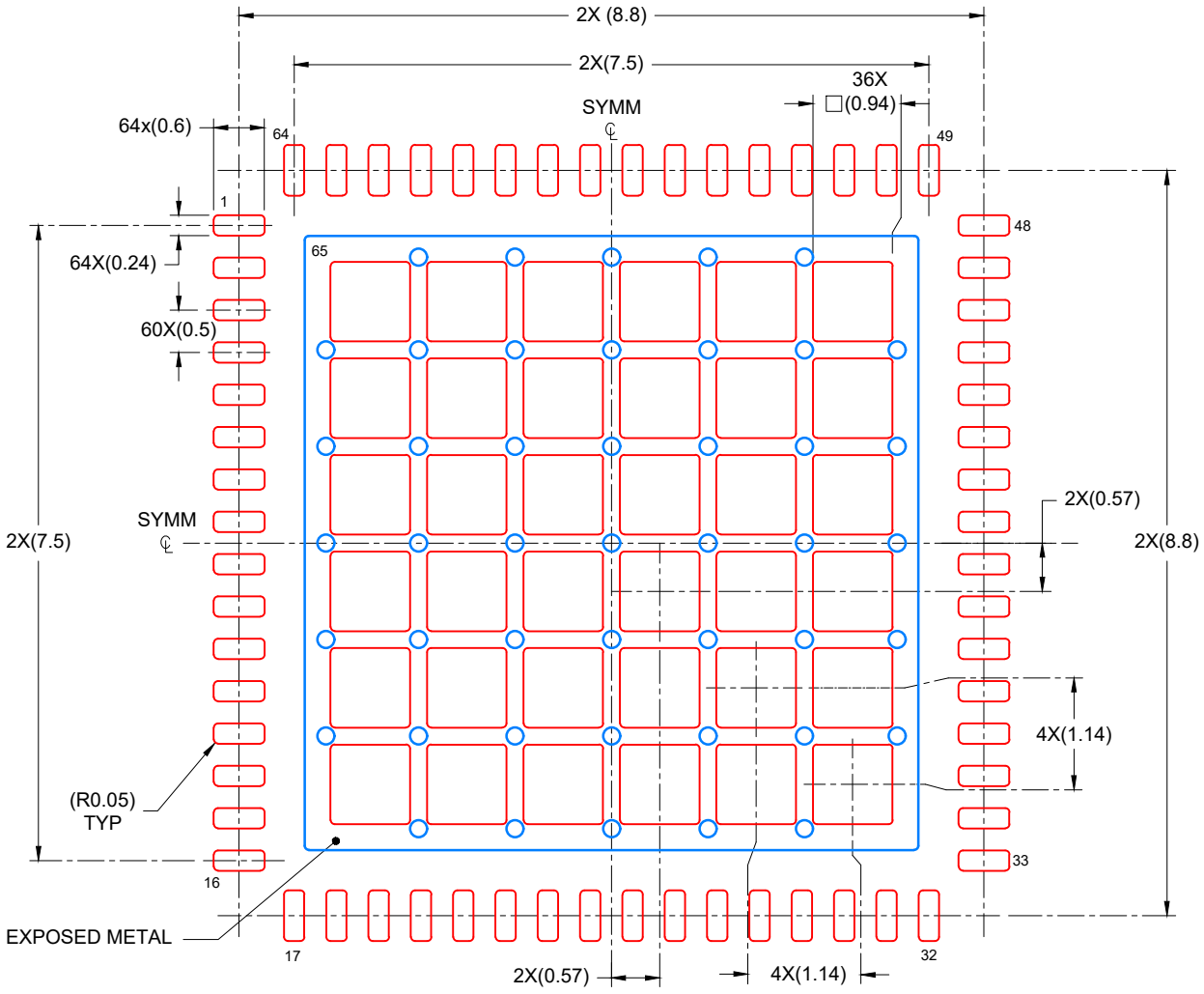

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.




NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.




SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
60% PRINTED COVERAGE BY AREA
SCALE: 12X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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