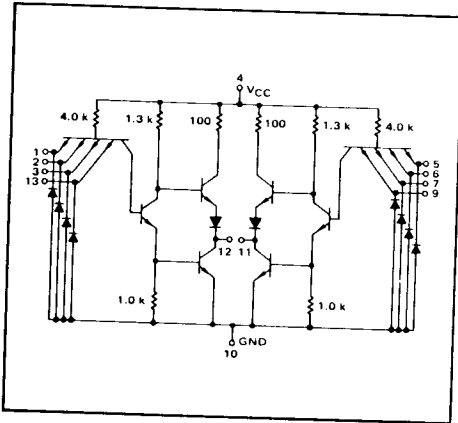


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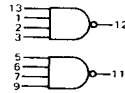
DUAL 4-INPUT "NAND" GATE

MTTL I MC500/400 series

MC500 · MC550
MC400 · MC450



This device consists of two 4 input NAND gates. The gates can be cross coupled to form a multiple-input R-S flip-flop or a circuit for eliminating contact bounce.



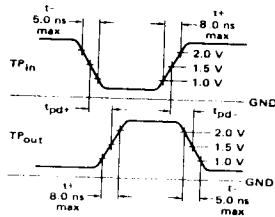
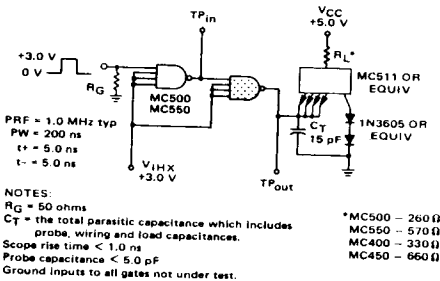
Positive Logic:
12 = $\overline{1 \cdot 2 \cdot 3 \cdot 4}$
Negative Logic:
12 = $\overline{1} \cdot \overline{2} \cdot \overline{3} \cdot \overline{4}$

Total Power Dissipation - 30 mW typ/pkg
Propagation Delay Time = 10 ns typ

TYPE NO.	INPUT LOADING FACTOR (I _I)	OUTPUT DRIVE (I _{OL})	TEMPERATURE RANGE
MC500 MC550	1 (-1.33 mA)	15 MC500 series Gates 7 MC500 series Gates	-55°C to +125°C
MC400 MC450	1 (-1.66 mA)	12 MC400 series Gates 6 MC400 series Gates	0° to +75°C

SWITCHING TIME TEST CIRCUIT

VOLTAGE WAVEFORMS AND DEFINITIONS



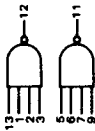
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MC500, MC550/MC400, MC450 (continued)

ELECTRICAL CHARACTERISTICS

Test procedures are shown for only one gate. The other gate is tested in the same manner. Further, test procedures are shown for only one input of the gate under test. To complete testing, sequence through remaining inputs.



Characteristic	Symbol	Pin Under Test	MC500, MC550 Test Limits						MC400, MC450 Test Limits						TEST CONDITIONS																					
			-55°C			+25°C			+125°C			0°C			+25°C			+75°C			mA				Volts											
			Min	Max	Unit	Min	Max	Unit	Min	Max	Unit	Min	Max	Unit	Min	Max	Unit	I _{OL}	I _{OH}	V _{IL}	V _{OL}	V _{IH}	V _{OH}	V _{CC}	V _{CH}	V _{IN}	V _{IO}	V _{OH}	V _{CH}	V _{IN}	V _{IO}	V _{OH}	V _{CH}			
			Min	Max	Unit	Min	Max	Unit	Min	Max	Unit	Min	Max	Unit	Min	Max	Unit	Min	Max	Unit	Min	Max	Unit	Min	Max	Unit	Min	Max	Unit	Min	Max	Unit	Min	Max	Unit	
Input Forward Current	I _F	1	-1.33	-	-1.33	-	-1.33	-	-1.33	-	-1.33	-	-1.68	-	-1.68	-	-1.68	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
Leakage Current	I _R	1	-	100	-	100	-	100	-	100	-	100	-	100	-	100	-	100	-	100	-	100	-	100	-	100	-	100	-	100	-	100	-	100	-	100
Inverse Beta Current	I _L	1	-	100	-	100	-	100	-	100	-	100	-	100	-	100	-	100	-	100	-	100	-	100	-	100	-	100	-	100	-	100	-	100	-	100
Breakdown Voltage	BV _{IL(10V)}	1	5.5	-	5.5	-	5.5	-	5.5	-	5.5	-	5.5	-	5.5	-	5.5	-	5.5	-	5.5	-	5.5	-	5.5	-	5.5	-	5.5	-	5.5	-	5.5	-	5.5	
	BV _{IO(10V)}	1	5.5	-	5.5	-	5.5	-	5.5	-	5.5	-	5.5	-	5.5	-	5.5	-	5.5	-	5.5	-	5.5	-	5.5	-	5.5	-	5.5	-	5.5	-	5.5	-	5.5	
Output	V _{OH(10V)}	12	-	0.45	-	0.45	-	0.45	-	0.45	-	0.45	-	0.45	-	0.45	-	0.45	-	0.45	-	0.45	-	0.45	-	0.45	-	0.45	-	0.45	-	0.45	-	0.45	-	0.45
	V _{OL(10V)}	12	2.5	-	2.4	-	2.7	-	2.5	-	2.4	-	2.5	-	2.5	-	2.5	-	2.5	-	2.5	-	2.5	-	2.5	-	2.5	-	2.5	-	2.5	-	2.5	-	2.5	
Leakage Current	I _{OLK}	12	-	250	-	250	-	250	-	250	-	250	-	250	-	250	-	250	-	250	-	250	-	250	-	250	-	250	-	250	-	250	-	250	-	250
Short-Circuit Current	I _{SC}	12	-10	-45	-	-10	-45	-	-10	-45	-	-10	-45	-	-10	-45	-	-10	-45	-	-10	-45	-	-10	-45	-	-10	-45	-	-10	-45	-	-10	-45	-	-10
Output Voltage	V _{OL}	12	-	0.40	-	0.45	-	0.40	-	0.45	-	0.40	-	0.40	-	0.40	-	0.40	-	0.40	-	0.40	-	0.40	-	0.40	-	0.40	-	0.40	-	0.40	-	0.40	-	0.40
	V _{OH}	12	2.8	-	3.2	-	3.35	-	3.0	-	3.1	-	3.15	-	3.15	-	3.15	-	3.15	-	3.15	-	3.15	-	3.15	-	3.15	-	3.15	-	3.15	-	3.15	-	3.15	
Power Requirements (Total Device)																																				
Maximum Power Supply Current	I _{max}	4	-	-	-	10	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	
Power Supply Drain	I _{DDH}	4	-	12	-	12	-	12	-	12	-	15	-	15	-	15	-	15	-	15	-	15	-	15	-	15	-	15	-	15	-	15	-	15	-	15
	I _{DDL}	4	-	6.0	-	6.0	-	6.0	-	6.0	-	6.0	-	6.0	-	6.0	-	6.0	-	6.0	-	6.0	-	6.0	-	6.0	-	6.0	-	6.0	-	6.0	-	6.0	-	6.0
Switching Parameters																																				
Turn-On Delay	t _{pd}	1,12	-	-	-	20	-	-	-	-	-	20	-	-	-	20	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	
Turn-Off Delay	t _{pd}	1,12	-	-	-	20	-	-	-	-	20	-	-	-	20	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	
Rise Time	t _r	1,12	-	-	-	8.0	-	-	-	-	8.0	-	-	-	8.0	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	
Fall Time	t _f	1,12	-	-	-	8.0	-	-	-	-	8.0	-	-	-	8.0	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	

* Prime Fan-Out.
 † Ground inputs to gates not under test during ALL tests, unless otherwise noted.
 ‡ The inputs of all gates must be ungrounded.

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