SN54LVT2952, SN74LVT2952 3.3-V ABT OCTAL BUS TRANSCEIVERS AND REGISTERS

WITH 3-STATE OUTPUTS SCBS152E – MAY 1992 – REVISED JULY 1995

- State-of-the-Art Advanced BiCMOS Technology (ABT) Design for 3.3-V Operation and Low-Static Power Dissipation
- Support Mixed-Mode Signal Operation (5-V Input and Output Voltages With 3.3-V V_{CC})
- Support Unregulated Battery Operation Down to 2.7 V
- Typical V_{OLP} (Output Ground Bounce) < 0.8 V at V_{CC} = 3.3 V, T_A = 25°C
- ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17
- Bus-Hold Data Inputs Eliminate the Need for External Pullup Resistors
- Support Live Insertion
- Package Options Include Plastic Small-Outline (DW), Shrink Small-Outline (DB), and Thin Shrink Small-Outline (PW) Packages, Ceramic Chip Carriers (FK), and Ceramic (JT) DIPs

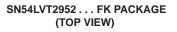
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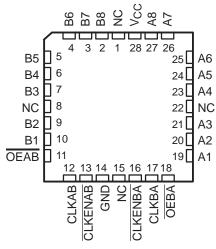
These octal bus transceivers and registers are designed specifically for low-voltage (3.3-V) V_{CC} operation, but with the capability to provide a TTL interface to a 5-V system environment.

The 'LVT2952 consist of two 8-bit back-to-back registers that store data flowing in both directions between two bidirectional buses. Data on the A or B bus is stored in the registers on the low-to-high

(TOP VIEW)								
B8 [B7] B6 [B5] B4 [B3] B2 [B1] OEAB [CLKAB]	1 2 3 4 5 6 7 8 9 10 11	24 23 22 21 20 19 18 17 16 15 14	V _{CC} A8 A7 A6 A5 A4 A3 A2 A1 OEBA CLKBA					
CLKAB	10	15	OEBA					

SN54LVT2952...JT PACKAGE SN74LVT2952...DB, DW, OR PW PACKAGE





NC - No internal connection

transition of the clock (CLKAB or CLKBA) input provided that the clock-enable (CLKENAB or CLKENBA) input is low. Taking the output-enable (OEAB or OEBA) input low accesses the data on either port.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

To ensure the high-impedance state during power up or power down, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN74LVT2952 is available in TI's shrink small-outline package (DB), which provides the same I/O pin count and functionality of standard small-outline packages in less than half the printed-circuit-board area.

The SN54LVT2952 is characterized for operation over the full military temperature range of -55° C to 125° C. The SN74LVT2952 is characterized for operation from -40° C to 85° C.



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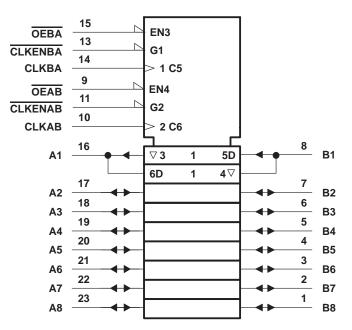
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FUNCTION TABLE [†]							
	INPUT	5		OUTPUT			
CLKENAB	CLKAB	OEAB	Α	В			
Н	Х	L	Х	в ₀ ‡			
Х	H or L	L	Х	в ₀ ‡ в ₀ ‡			
L	\uparrow	L	L	L			
L	\uparrow	L	Н	Н			
Х	Х	Н	Х	Z			

[†] A-to-B data flow is shown; B-to-A data flow is similar but uses CLKENBA, CLKBA, and OEBA.

[‡]Level of B before the indicated steady-state input conditions were established

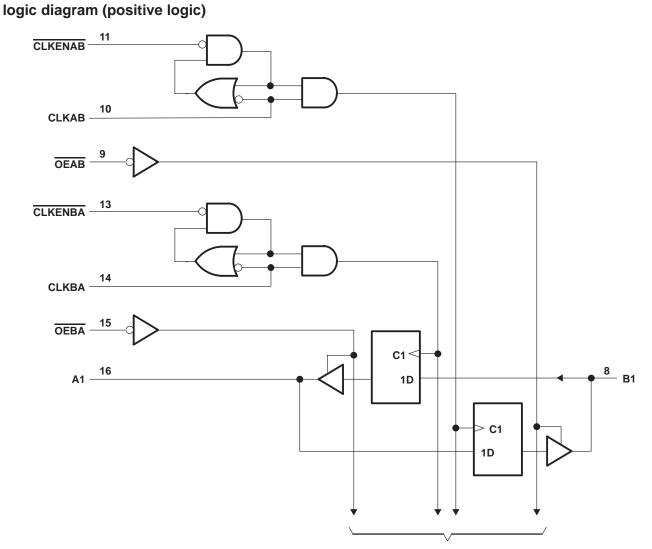
logic symbol§



§ This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12. Pin numbers shown are for the DB, DW, JT, and PW packages.



SN54LVT2952, SN74LVT2952 **3.3-V ABT OCTAL BUS TRANSCEIVERS AND REGISTERS** WITH 3-STATE OUTPUTS SCBS152E - MAY 1992 - REVISED JULY 1995



Pin numbers shown are for the DB, DW, JT, and PW packages.

To Seven Other Channels



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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage range, V _{CC} Input voltage range, V _I (see Note 1)	
Voltage range applied to any output in the high state or power-off state, V_{Ω} (see Note 1)	
Current into any output in the low state, I_{O} : SN54LVT2952	
SN74LVT2952	
Current into any output in the high state, I _O (see Note 2): SN54LVT2952	48 mA
SN74LVT2952	64 mA
Input clamp current, I _{IK} (V _I < 0)	–50 mA
Output clamp current, I_{OK} (V _O < 0)	–50 mA
Maximum power dissipation at $T_A = 55^{\circ}C$ (in still air) (see Note 3): DB package	0.65 W
DW package	
PW package	
Storage temperature range, T _{stg}	

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

2. This current flows only when the output is in the high state and $V_O > V_{CC}$.

 The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils. For more information, refer to the *Package Thermal Considerations* application note in the 1994 ABT Advanced BiCMOS Technology Data Book, literature number SCBD002B.

recommended operating conditions (see Note 4)

			SN54LV	T2952	SN74LV	T2952	
			MIN	MAX	MIN	MAX	UNIT
VCC	Supply voltage		2.7	3.6	2.7	3.6	V
VIH	High-level input voltage		2	EW	2		V
VIL	Low-level input voltage			0.8		0.8	V
VI	Input voltage			5.5		5.5	V
ЮН	High-level output current		(C)	-24		-32	mA
IOL	Low-level output current		200	48		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	Outputs enabled	4	10		10	ns/V
TA	Operating free-air temperature		-55	125	-40	85	°C

NOTE 4: Unused control inputs must be held high or low to prevent them from floating.

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

				SN	54LVT29	52	SN	74LVT29	52		
PARAMETER	T	TEST CONDITIONS				MAX	MIN	TYP [†]	MAX	UNIT	
VIK	V _{CC} = 2.7 V,	lj = -18 mA				-1.2			-1.2	V	
	$V_{CC} = MIN \text{ to } MAX^{\ddagger},$	I _{OH} = -100 μA		VCC-C).2		VCC-0	.2			
Maria	V _{CC} = 2.7 V,	I _{OH} = – 8 mA		2.4			2.4			V	
VOH		I _{OH} = – 24 mA		2						V	
	$V_{CC} = 3 V$	$I_{OH} = -32 \text{ mA}$					2				
	Vac 27V	I _{OL} = 100 μA				0.2			0.2		
	$V_{CC} = 2.7 V$	I _{OL} = 24 mA				0.5			0.5		
		I _{OL} = 16 mA				0.4			0.4	V	
VOL	$\lambda = -2\lambda $	I _{OL} = 32 mA				0.5			0.5	v	
	$V_{CC} = 3 V$	I _{OL} = 48 mA				0.55					
		I _{OL} = 64 mA			4				0.55		
	V _{CC} = 3.6 V,	$V_I = V_{CC}$ or GND	Control inputs		Ę.	±1			±1		
	$V_{CC} = 0$ or MAX [‡] ,	V _I = 5.5 V	Control inputs		,Q	10			10		
li VC		V _I = 5.5 V		20				20	μA		
	V _{CC} = 3.6 V	$V_I = V_{CC}$	A or B ports§	0	ବି	5			5		
		$V_{I} = 0$		8	~	-10			-10		
loff	$V_{CC} = 0,$	$V_{I} \text{ or } V_{O} = 0 \text{ to } 4.5$	V						±100	μΑ	
ha in	V/22 2)/	V _I = 0.8 V	A or D porto	75			75			A	
l _{l(hold)}	$V_{CC} = 3 V$	V _I = 2 V	A or B ports	-75			-75			μA	
IOZH	V _{CC} = 3.6 V,	V _O = 3 V				1			1	μΑ	
IOZL	V _{CC} = 3.6 V,	$V_{O} = 0.5 V$				-1			-1	μΑ	
		1- 0	Outputs high		0.13	0.19		0.13	0.19		
	$V_{CC} = 3.6 V,$ VI = V _{CC} or GND	$I_{O} = 0,$	Outputs low		8.8	12		8.8	12	mA	
			Outputs disabled		0.13	0.19		0.13	0.19		
∆ICC¶	$V_{CC} = 3 V \text{ to } 3.6 V,$ Other inputs at V_{CC} of	One input at V _{CC} · r GND	– 0.6 V,			0.2			0.2	mA	
Ci	V _I = 3 V or 0				4.5			4.5		pF	
C _{io}	V _O = 3 V or 0				11.5			11.5		pF	

[†] All typical values are at V_{CC} = 3.3 V, T_A = 25°C. [‡] For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

 $\$ Unused terminals at V_{CC} or GND

I This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.



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timing requirement over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

			SN54LVT2952 V _{CC} = 3.3 V ± 0.3 V								
					V _{CC} = 2.7 V		V _{CC} = 3.3 V ± 0.3 V		V _{CC} = 2.7 V		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
fclock	Clock frequency							150		150	MHz
		CLK high			M:		3.3		3.3		
t _w Pulse duration	CLK low			Ņ		3.3		3.3		ns	
		Data high	2.6		2.9		2.5		2.8		
	Setup time, A or B before CLK1	Data low	2.6	6	3.1		2.5		3		
t _{su}		Data high	0.9	20	0.8		0.9		0.8		ns
Setup time, CE before CLK↑	Data low	2.5	20	2.7		2.4		2.7			
4	Hold time, A or B after CLK↑		1.5	Q	0.7		1.5		0.7		
th	Hold time, CE after CLK↑		2.6		2.6		2.5		2.6		ns

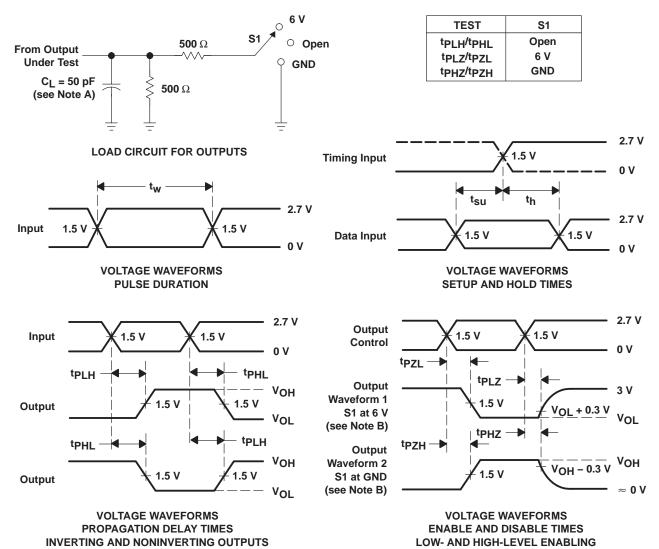
switching characteristics over recommended operating free-air temperature range, $C_L = 50 \text{ pF}$ (unless otherwise noted) (see Figure 1)

			SN		SN54LVT2952 SN74LVT2952			952	52			
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} = 3.3 V ± 0.3 V		V _{CC} = 2.7 V		V _{CC} = 3.3 V ± 0.3 V			V _{CC} =	UNIT	
			MIN	MAX	MIN	MAX	MIN	TYP†	MAX	MIN	MAX	
fmax					M		150			150		MHz
^t PLH	CLKBA or	A	1.3	6.4	2.7	7.4	1.3	3.6	6.1	2.7	7.1	
^t PHL	CLKAB	A or B	1.8	6.1	2.7	7	1.8	3.7	6	2.7	6.9	ns
^t PZH	OEBA or	A or B	1	6.3	2.6	7.3	1	3.2	5.6	2.6	6.7	
^t PZL	OEAB	A OF B	1.1	6,6	2.9	8.2	1.2	3.2	6.5	2.9	8	ns
^t PHZ	OEBA or	A or B	1	27	2.7	7.6	1	4.1	6.3	2.7	6.9	ns
^t PLZ	OEAB	AUB	1.6	Q 5.8	1.7	6	1.6	3.3	5.1	1.8	5.3	115

[†] All typical values are at V_{CC} = 3.3 V, T_A = 25° C.



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PARAMETER MEASUREMENT INFORMATION

NOTES: A. Cl includes probe and jig capacitance.

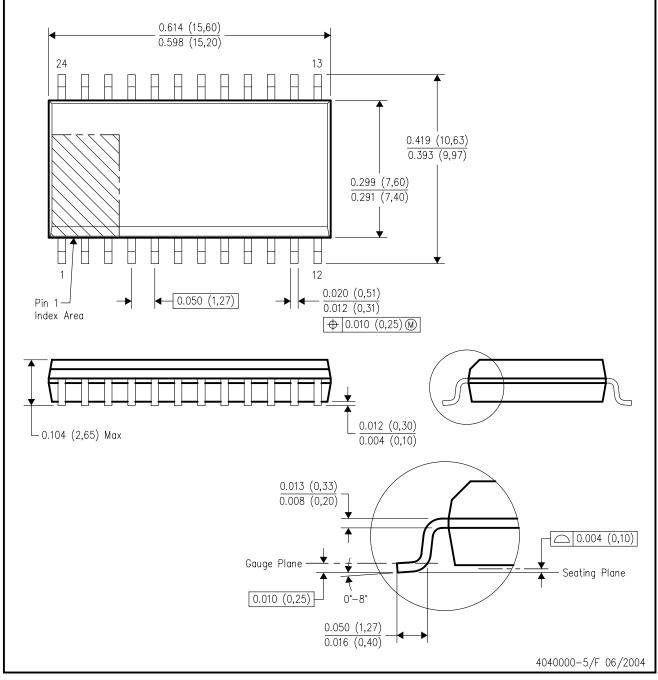
- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.
 Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, Z_O = 50 Ω , t_f \leq 2.5 ns, t_f \leq 2.5 ns.
- D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms



DW (R-PDSO-G24)

PLASTIC SMALL-OUTLINE PACKAGE



NOTES: A. All linear dimensions are in inches (millimeters).

B. This drawing is subject to change without notice.

C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).

D. Falls within JEDEC MS-013 variation AD.



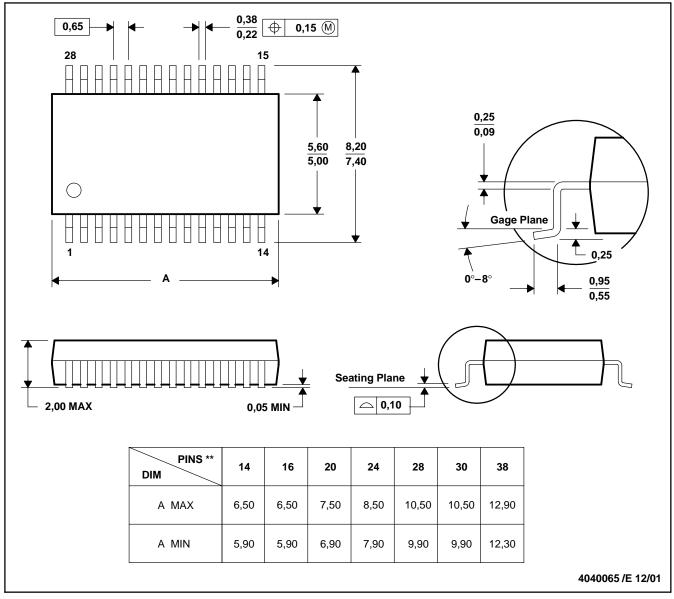
MECHANICAL DATA

MSSO002E - JANUARY 1995 - REVISED DECEMBER 2001

DB (R-PDSO-G**)

PLASTIC SMALL-OUTLINE

28 PINS SHOWN



NOTES: A. All linear dimensions are in millimeters.

- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
- D. Falls within JEDEC MO-150



MECHANICAL DATA

MTSS001C - JANUARY 1995 - REVISED FEBRUARY 1999

PW (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14 PINS SHOWN



NOTES: A. All linear dimensions are in millimeters.

- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
- D. Falls within JEDEC MO-153



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