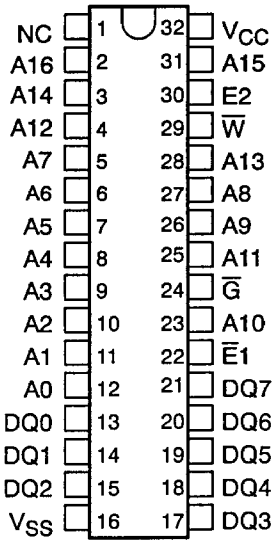
- **Organization . . . 131,072 × 8**
- **Single 5-V Power Supply (10% Tolerance)**
- **High-Density Packaging:**
  - **—Plastic 32-pin 600-Mil Dual-In-Line Package (NW Suffix)**
  - **—Plastic 32-pin 525-Mil Small Outline Package (DK Suffix)**
- **All Inputs/Outputs Fully TTL Compatible**
- **Max Access/Min Cycle Times**
  TMS62828L-85 . . . 85 ns
  TMS62828L-10 . . . 100 ns
  TMS62828L-12 . . . 120 ns
- **Power Saving CMOS Technology**
- **3-State Output Buffers**
- **Low Power Dissipation (V_{CC} = 5.5 V)**
  - **—Active . . . 385 mW Worst Case**
  - **—Standby . . . 0.55 mW Worst Case (CMOS Input Levels)**
  - **—Standby . . . 16.5 mW Worst Case (TTL Input Levels)**
- **Operating Temperature Range . . . 0°C to 70°C**

DK AND NW PACKAGES
(TOP VIEW)



PIN NOMENCLATURE	
A0-A16	Address Inputs
DQ0-DQ7	Data In-Data Out
$\overline{E}$1-E2	Chip Enables
$\overline{G}$	Output Enable
NC	No Connection
$\overline{W}$	Write Enable
V_{CC}	5-V Power Supply
V_{SS}	Ground

description

The TMS62828L is a common I/O, 1,048,576-bit low power static random-access memory organized as 131,072 words by 8 bits. The TMS62828L features maximum address access and minimum cycle times of 85, 100, and 120 ns. The TMS62828L is fabricated using CMOS technology. Maximum power dissipation is as low as 385 mW active. This reduces to a maximum of 0.55 mW (CMOS input levels) and 16.5 mW (TTL input levels) during standby operation.

All inputs and outputs are compatible with Series 54/74 TTL circuits without the use of external pull-up resistors. Each output can drive one Series 54/74 TTL circuit without external resistors. The data outputs are three-state for connecting multiple devices to a common bus.

The TMS62828L is offered in 600-mil plastic dual-in-line package (NW suffix) and a 525-mil plastic small outline package (DK suffix). Both are characterized for operation from 0°C to 70°C.

operation

address (A0-A16)

The 17 addresses select one of the 131,072 8-bit words in the RAM. The address inputs must be stable for the duration of a read or write cycle. The address inputs can be driven directly from standard Series 54/74 TTL without external pull-up resistors.

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chip enable/powerdown ($\overline{E}1$, E2)

The chip enable/powerdown terminals ($\overline{E}1$ and E2) can be driven directly by standard TTL circuits, and affect the powerdown/deselect function of the chip. Whenever $\overline{E}1$ is high or E2 is low, the device is put into a reduced power standby mode. Data is retained during the standby mode.

write enable ($\overline{W}$)

The read or write mode is selected through the write enable terminal ($\overline{W}$). A logic high selects the read mode; a logic low selects the write mode. $\overline{W}$ or $\overline{E}1$ must be high or E2 must be low when changing addresses to prevent inadvertently writing data into a memory location. The $\overline{W}$ input can be driven directly from standard TTL circuits.

output enable ($\overline{G}$)

The output enable terminal, which can be driven directly from standard TTL circuits, affects only the data-out terminals. When output enable is at a logic high level, the output terminals are disabled to the high-impedance state. Output enable provides greater output control flexibility, simplifying data bus design.

data in/data out (DQ0-DQ7)

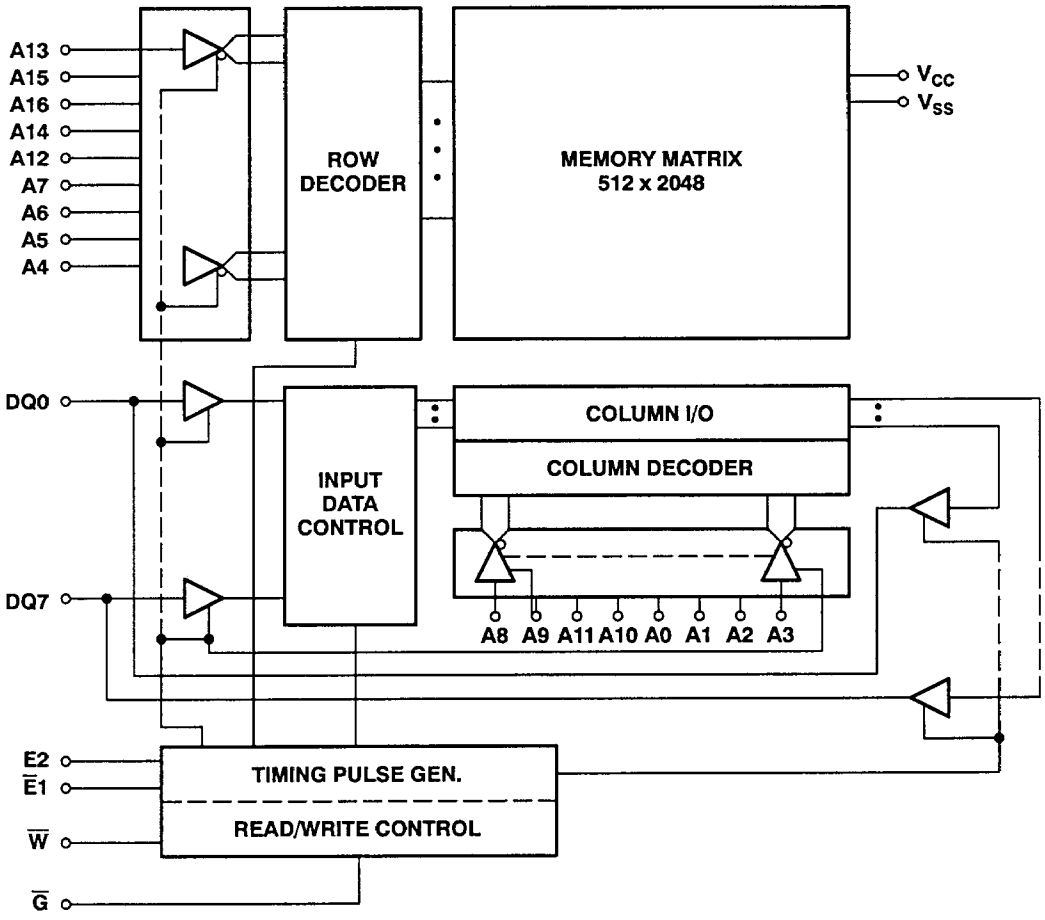
Data can be written into a selected device when write enable ($\overline{W}$) input is low, and chip enable/powerdown ($\overline{E}1$) is low, and chip enable (E2) is high. Data can be read when write enable ($\overline{W}$) is high, chip enable/powerdown ($\overline{E}1$) is low, chip enable (E2) is high, and output enable ($\overline{G}$) is low. The DQ terminals can be driven directly from standard TTL circuits. The three-state output buffers provide direct TTL compatibility.

FUNCTION TABLE

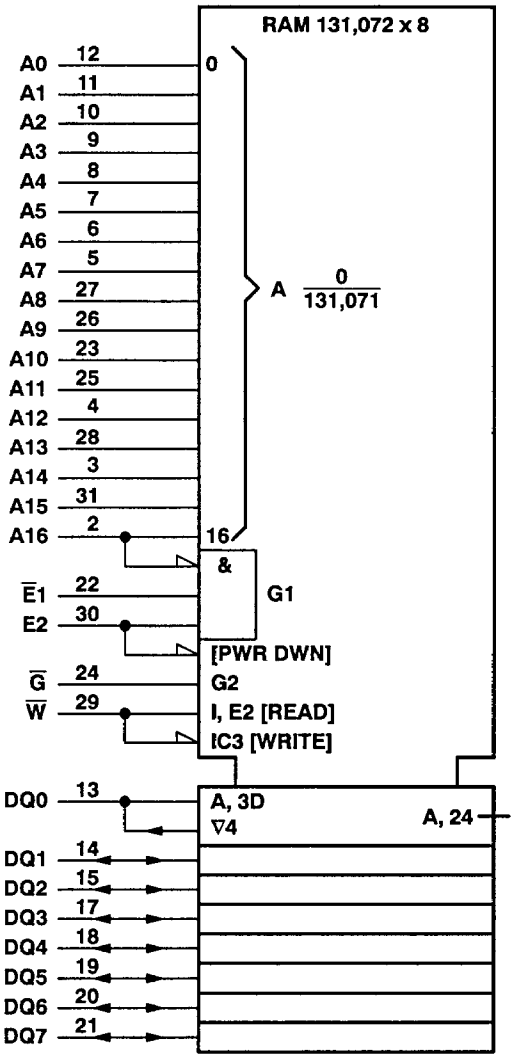
	MODE					
FUNCTION	Deselect Powerdown	Deselect Powerdown	Deselect	Read (Read Cycle)	Write (Write Cycle 1)	Write (Write Cycle 2)
$\overline{W}$	X	X	H	H	L	L
$\overline{E}1$	H	X	L	L	L	L
E2	X	L	H	H	H	H
$\overline{G}$	X	X	H	L	H	L
DQ0-DQ7(OUT)	HI-Z	HI-Z	HI-Z	D_{OUT}	D_{IN}	D_{IN}

X = Don't Care.

functional block diagram



logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

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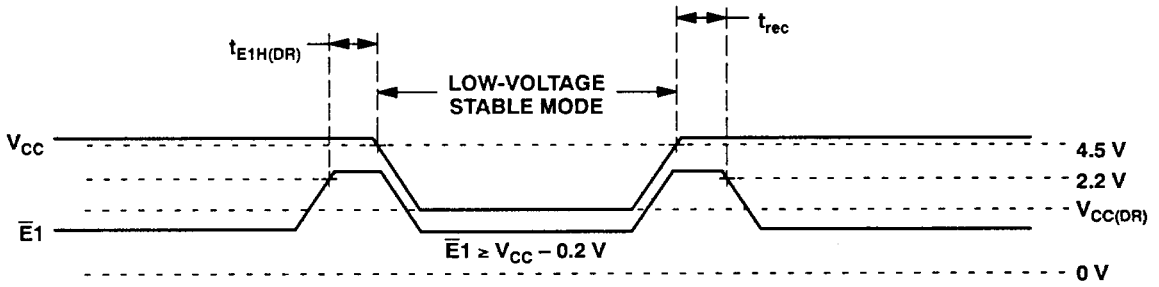
data retention specifications for low V_{CC} (T_A = 0°C to 70°C)

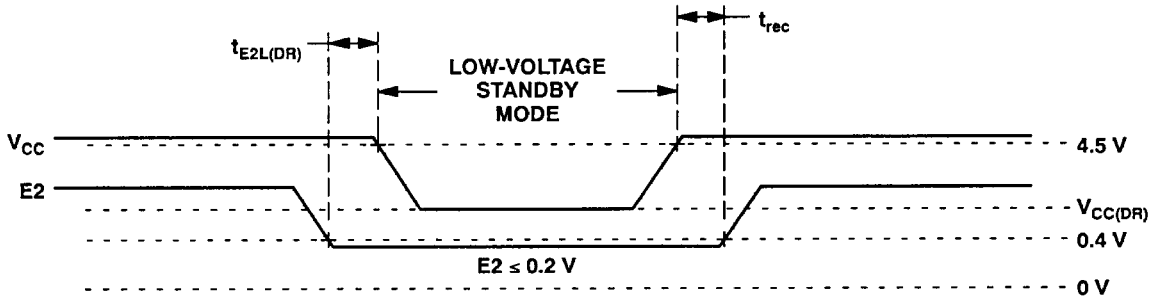
PARAMETER		TEST CONDITIONS	MIN	NOM	MAX	UNIT
$V_{CC(DR)}$	V_{CC} for data retention	$\overline{E}1 \geq V_{CC} - 0.2$ V, $E2 \geq V_{CC} - 0.2$ V or 0 V ≤ E2 ≤ 0.2 V, $V_{in} \geq 0$ V	2			V
$I_{CC(DR)}$	Low-voltage standby supply current	V_{CC} = 3.0 V, $V_{in} \geq 0$ V, $\overline{E}1 \geq V_{CC} - 0.2$ V, $E2 \geq V_{CC} - 0.2$ V or 0 V ≤ E2 ≤ 0.2 V		1	50†	µA
$t_{E1H(DR)}$	Chip deselect to V_{CC} going low	See "Data Retention Waveforms" below	0			ns
$t_{E2L(DR)}$	Chip deselect to V_{CC} going low		0			ns
t_{rec}	Operation recovery time		$t_{c(rd)}$‡			ns

† When V_{IL} min = – 0.3 V and T_A = 0°C to 40°C, then the maximum low voltage standby current can be reduced to 20 µA.
‡ $t_{c(rd)}$ is the read cycle time.

low V_{CC} data retention waveform ($\overline{E}1$ controlled)§



low V_{CC} data retention waveform (E2 controlled)§



§ In the low V_{CC} data-retention mode, E2 controls the address, $\overline{W}$, $\overline{E}1$, $\overline{G}$, and data-input buffers. When E2 controls data retention mode, these inputs can float. When $\overline{E}1$ controls the data-retention mode, E2 must be within 0.2 V of V_{CC} or GND and the other inputs (A0-A16, $\overline{W}$, DQ0-DQ7) can float.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range (see Notes 1 and 2) ..... −0.5 V to 7 V
Power dissipation ..... 1 W
Operating free-air temperature range ..... 0°C to 70°C
Temperature range powered down ..... −10°C to 85°C
Storage temperature range ..... −55°C to 125°C

† Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions beyond those indicated in the "Recommended Operating Conditions" section of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values are with respect to V_{SS}.
2. V_{CC} may go down to −3.0 V for a maximum time interval of 30 ns.

recommended operating conditions

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{IH}	High-level input voltage	2.2		6	V
V_{IL}	Low-level input voltage (see Note 3)	−0.3		0.8	V
T_A	Operating free-air temperature	0		70	°C

NOTE 3. The input voltage may go down to −3.0 V for a maximum time interval of 30 ns.

electrical characteristics over full ranges of recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP‡	MAX	UNIT
V_{OH}	High-level output voltage	I_{OH} = −1 mA	2.4			V
V_{OL}	Low-level output voltage	I_{OL} = 2.1 mA			0.4	V
I_I	Input current	V_{in} = GND to V_{CC}			2	µA
I_O	Output current	$\overline{E}1 = V_{IH}$ or $E2 = V_{IL}$, $\overline{G} = V_{IH}$ or $\overline{W} = V_{IL}$, $V_{I/O}$ = GND to V_{SS}			2	µA
I_{CC}	Operating power supply current	$\overline{E}1 = V_{IL}$, $E2 = V_{IH}$, $I_{I/O}$ = 0 mA		15	35	mA
$I_{CC(AV)1}$	Average operating current	Minimum cycle, Duty = 100%, $\overline{E}1 = V_{IL}$, $E2 = V_{IH}$, $I_{I/O}$ = 0 mA		45	70	mA
$I_{CC(AV)2}$	Average operating current	Cycle = 1 µs, Duty = 100%, $I_{I/O}$ = 0 mA, $\overline{E}1 \le 0.2$ V, $E2 \ge V_{CC} - 0.2$ V, $V_{IH} \ge V_{CC} - 0.2$ V, $V_{IL} \le 0.2$ V		15	30	mA
$I_{CC(SB)1}$	Standby supply current (TTL levels)	$\overline{E}1 = V_{IH}$, $E2 = V_{IH}$ or $E2 = V_{IL}$		1	3	mA
$I_{CC(SB)2}$	Standby supply current (low-power CMOS levels)	$V_{in} \ge 0$ V, $\overline{E}1 \ge V_{CC} - 0.2$ V, $E2 \ge V_{CC} - 0.2$ V or 0 V ≤ E2 ≤ 0.2 V		.002	.1	mA

‡ Typical values are measured at V_{CC} = 5 V, T_A = 25°C, and specified loading.

capacitance, T_A = 25°C, f = 1 MHz§

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
C_i	Input capacitance	V_{in} = 0 V			8	pF
$C_{i/o}$	Input/output capacitance	$V_{i/o}$ = 0 V			10	pF

§ Capacitance measurements are made on a sample basis only.

timing requirements over recommended supply voltage range and operating temperature range (read cycle) (see Note 4)

PARAMETER		ALTERNATE SYMBOL	TMS62828L-85		TMS62828L-10		TMS62828L-12		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
$t_{c(rd)}$	Read cycle time	t_{RC}	85		100		120		ns

switching characteristics over full ranges of recommended operating conditions (read cycle) (see Note 4)

PARAMETER		ALTERNATE SYMBOL	TMS62828L-85		TMS62828L-10		TMS62828L-12		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
$t_{a(A)}$	Access time from address	t_{AA}		85		100		120	ns
$t_{a(E1)}$	Access time from E1	t_{CO1}		85		100		120	ns
$t_{a(E2)}$	Access time from E2	t_{CO2}		85		100		120	ns
$t_{a(G)}$	Access time from $\overline{G}$	t_{OE}		45		50		60	ns
$t_{en(E1)}$	Output enable time from $\overline{E}1$ (see Note 5)	t_{LZ1}	10		10		10		ns
$t_{en(E2)}$	Output enable time from E2 (see Notes 5 and 6)	t_{LZ2}	10		10		10		ns
$t_{en(G)}$	Output enable time from $\overline{G}$ (see Notes 5 and 6)	t_{OLZ}	5		5		5		ns
$t_{dis(E1)}$	Output disable time from $\overline{E}1$ (see Notes 5 and 6)	t_{HZ1}	0	30	0	35	0	45	ns
$t_{dis(E2)}$	Output disable time from E2 (see Notes 5 and 6)	t_{HZ2}	0	30	0	35	0	45	ns
$t_{dis(G)}$	Output disable time from $\overline{G}$ (see Notes 5 and 6)	t_{OHZ}	0	30	0	35	0	45	ns
$t_{v(A)}$	Output data valid time after address change	t_{OH}	10		10		10		ns

NOTES: 4. Timing requirements and switching characteristics are defined under the following conditions:

Input pulse levels	0.8 V to 2.4 V
Input rise and fall time	5 ns
Input timing reference level	1.5 V
Output timing reference level	1.5 V
Output load (including scope and jig)	1 TTL gate and C_L (100 pF)

5. $t_{dis(E1)}$, $t_{dis(E2)}$, and $t_{dis(G)}$ are defined as the time at which the outputs achieve the open circuit conditions and are not referenced to output voltage levels.
6. At any given temperature and voltage condition, the slowest output disable time, t_{dis}, is faster than the fastest output enable time, t_{en}, both for a given device and from device to device. This parameter is sampled and not 100% tested.

timing requirements over recommended supply voltage range and operating temperature range (write cycle) (see Note 4)

PARAMETER		ALTERNATE SYMBOL	TMS62828L-85		TMS62828L-10		TMS62828L-12		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
$t_{c(W)}$	Write cycle time	t_{WC}	85		100		120		ns
$t_{su(E)}$	Chip enable setup time	t_{CW}	75		90		100		ns
$t_{su(A)}$	Address setup time	t_{AS}	0		0		0		ns
t_{AVWH}	Address valid time to write high	t_{AW}	75		90		100		ns
$t_{w(W)}$	Write pulse duration	t_{WP}	65		75		85		ns
$t_{rec(W)}$	Write recovery time	t_{WR}	5		5		10		ns
$t_{su(D)}$	Data setup time before write high	t_{DW}	35		40		45		ns
$t_{h(D)}$	Data hold time after write high	t_{DH}	0		0		0		ns
$t_{v(W)}$	Output data valid time after write high (see Note 7)	t_{OW}	5		5		5		ns

switching characteristics over full ranges of recommended operating conditions (write cycle) (see Note 4)

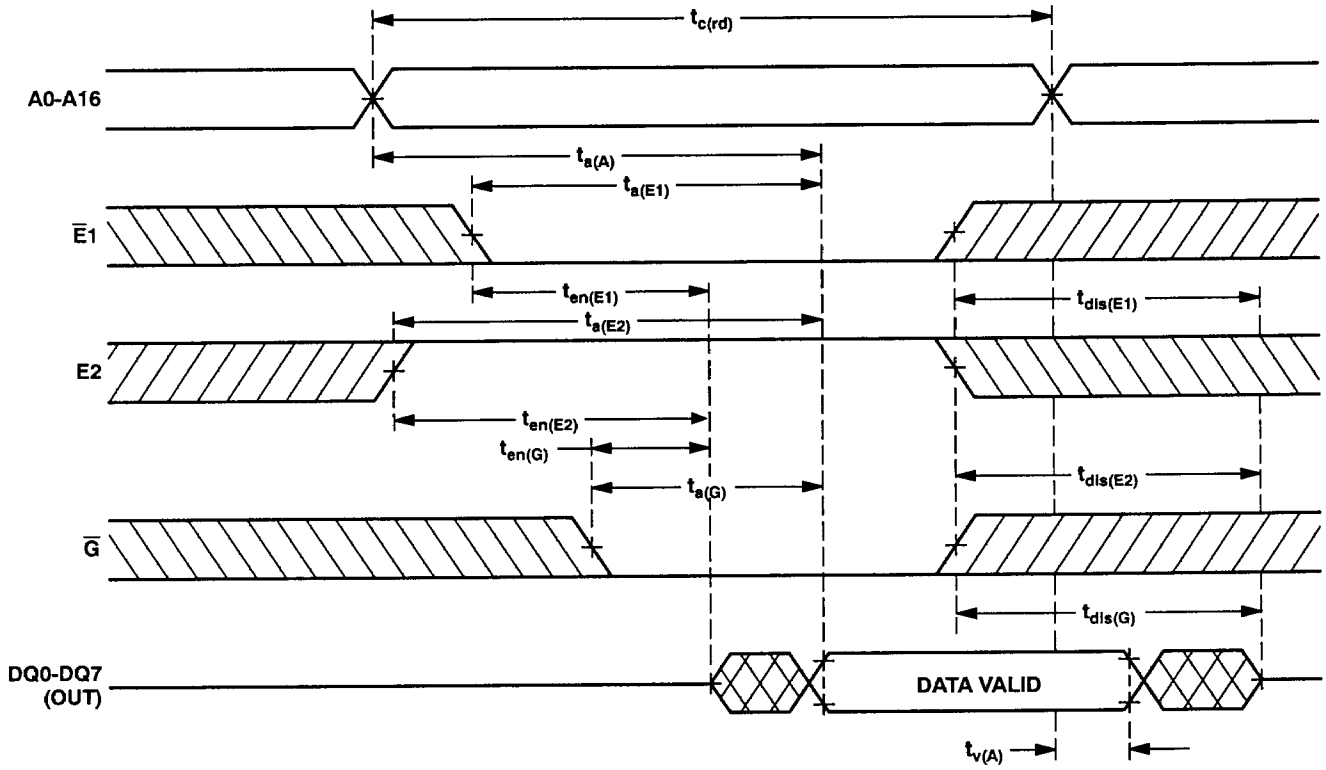
PARAMETER		ALTERNATE SYMBOL	TMS62828L-85		TMS62828L-10		TMS62828L-12		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
$t_{dis(W)}$	Output disable time from $\overline{W}$ (see Note 7)	t_{WHZ}	0	30	0	35	0	40	ns

NOTES: 4. Timing requirements and switching characteristics are defined under the following conditions:

Input pulse levels	0.8 V to 2.4 V
Input rise and fall time	5 ns
Input timing reference level	1.5 V
Output timing reference level	1.5 V
Output load (including scope and jig)	1 TTL gate and C_L (100 pF)

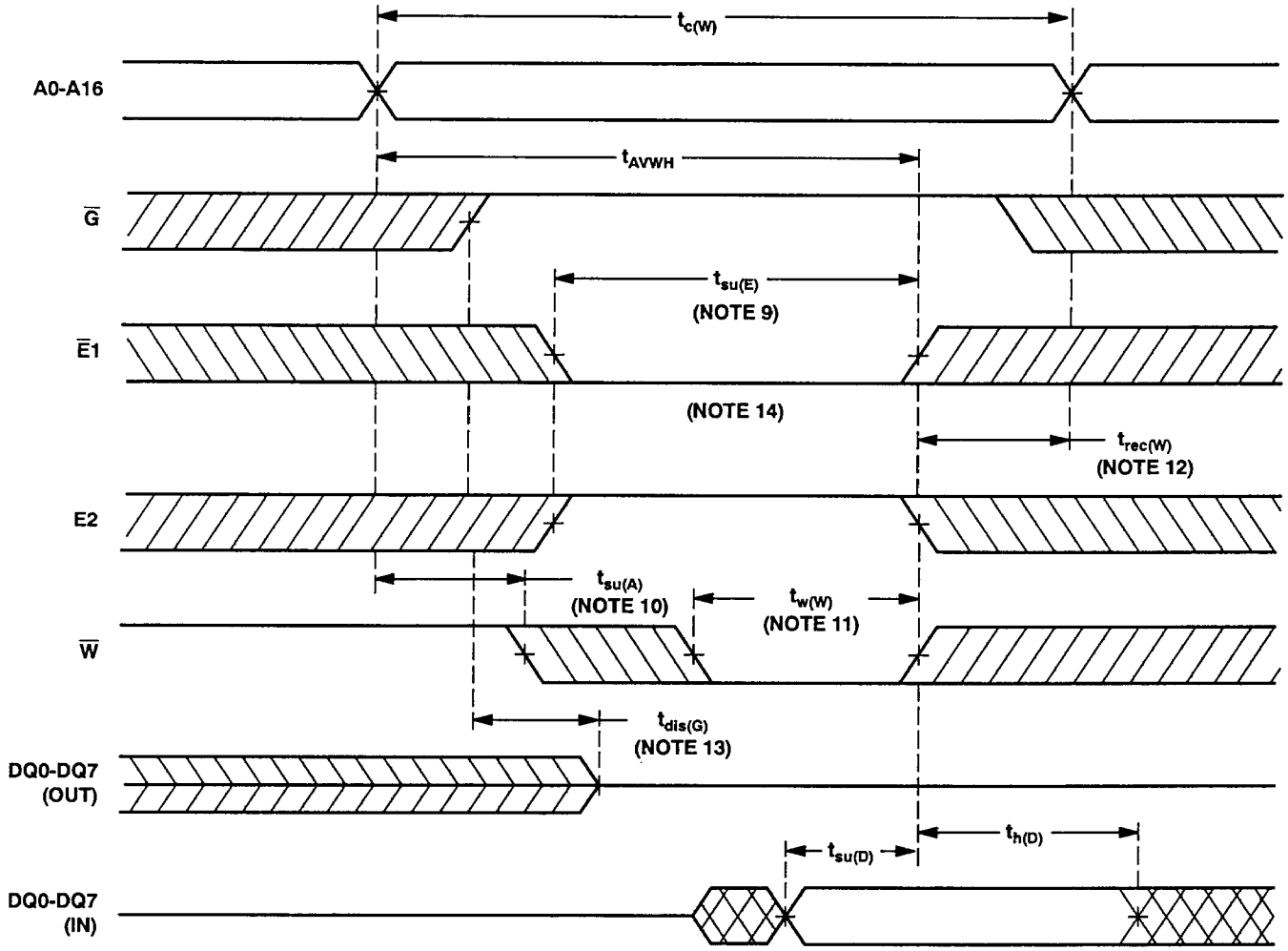
7. This parameter is sampled and not 100% tested.

read cycle timing



NOTE 8: $\overline{W}$ is high during the read cycle.

write cycle timing ($\overline{G}$ controlled)



NOTES: 9. $t_{su(E)}$ is measured from the later of $\overline{E}1$ going low or E2 going high to the end of write.
10. $t_{su(A)}$ is measured from the address valid to the beginning of write.
11. A write occurs during the overlap of a low $\overline{E}1$, a high E2, and a low $\overline{W}$. A write begins at the latest transition among $\overline{E}1$ going low, E2 going high, and $\overline{W}$ going low. A write ends at the earliest transition among $\overline{E}1$ going high, E2 going low, and $\overline{W}$ going high. $t_{w(W)}$ is measured from the beginning of write to the end of write.
12. $t_{rec(W)}$ is measured from the earliest of $\overline{E}1$ or $\overline{W}$ going high or E2 going low to the end of the write cycle.
13. During this period, I/O pins are in the output state, therefore; the input signals of the opposite phase to the outputs must not be applied.
14. If the $\overline{E}1$ low transition occurs simultaneously with the $\overline{W}$ low transitions or after the $\overline{W}$ low transitions, output remains in a high-impedance state.

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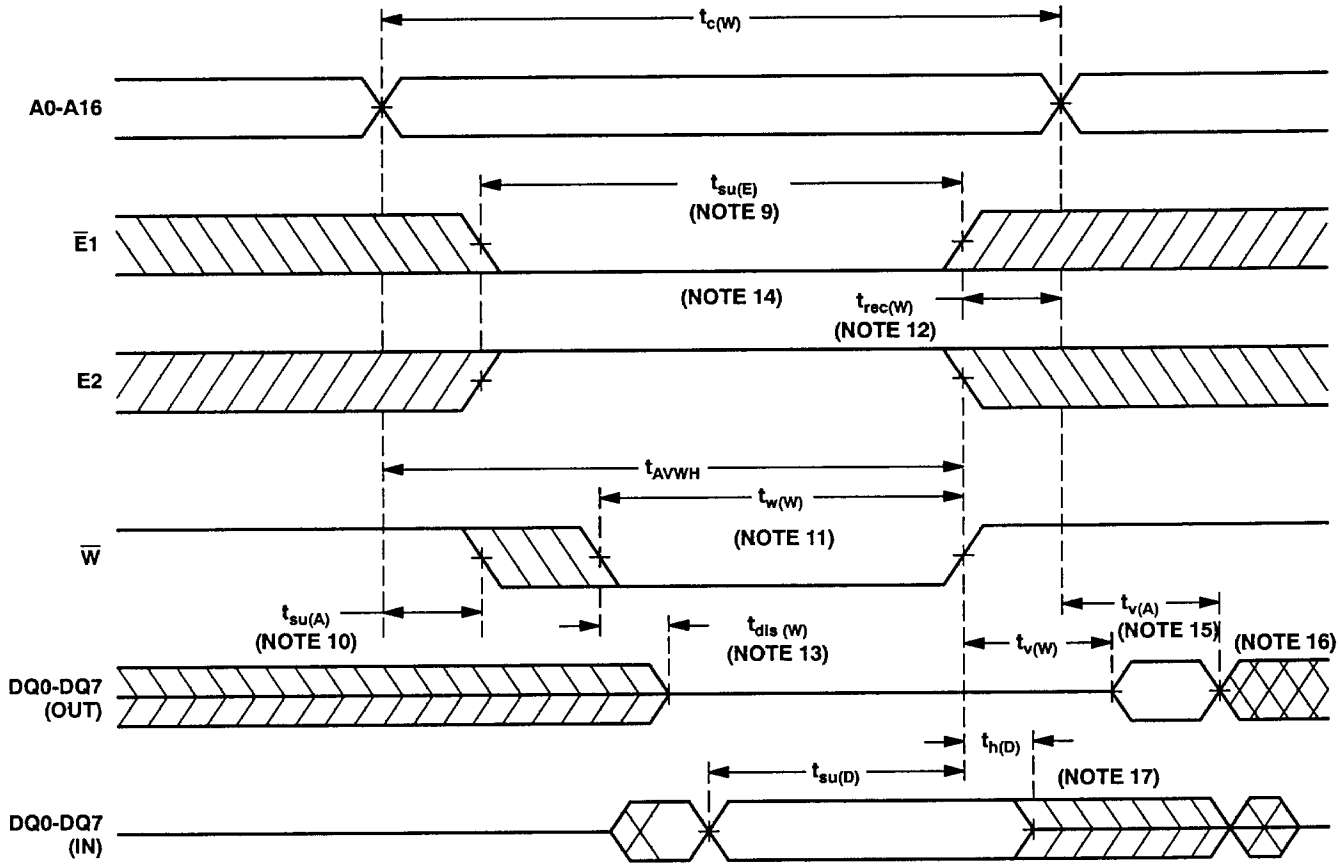
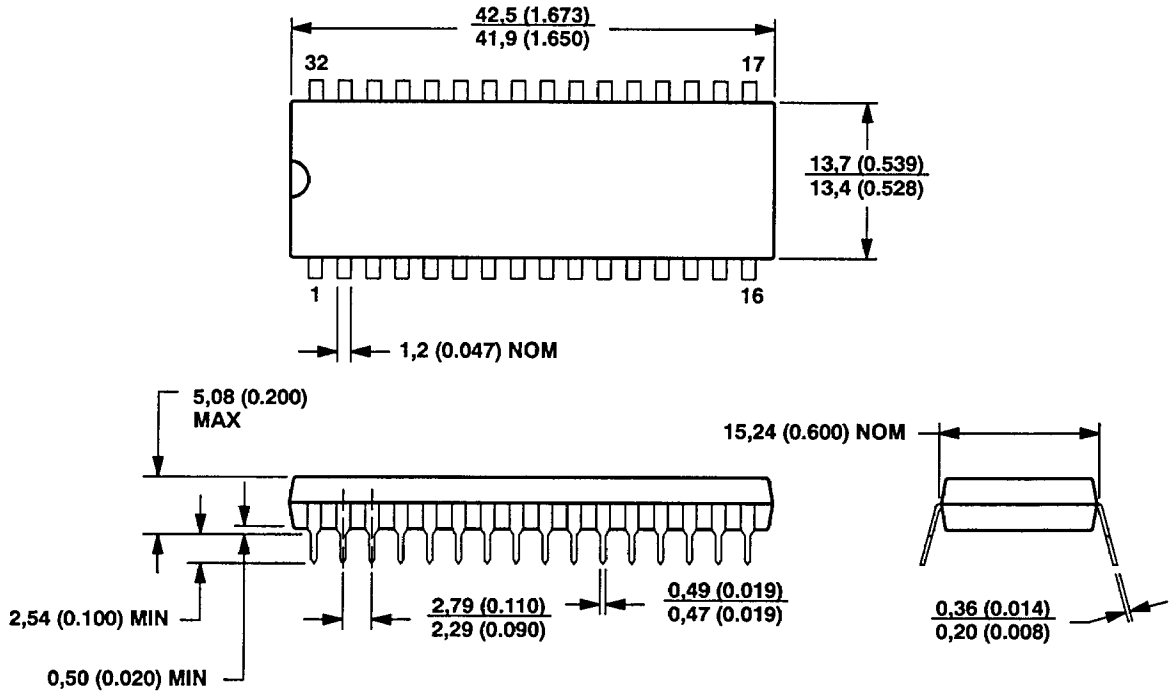
write cycle timing ($\overline{G}$ low controlled)



NOTES: 9. $t_{su(E)}$ is measured from the later of $\overline{E}1$ going low or E2 going high to the end of write.
10. $t_{su(A)}$ is measured from the address valid to the beginning of write.
11. A write occurs during the overlap of a low $\overline{E}1$, a high E2, and a low $\overline{W}$. A write begins at the latest transition among $\overline{E}1$ going low, E2 going high, and $\overline{W}$ going low. A write ends at the earliest transition among $\overline{E}1$ going high, E2 going low, and $\overline{W}$ going high. $t_{w(W)}$ is measured from the beginning of write to the end of write.
12. $t_{rec(W)}$ is measured from the earliest of $\overline{E}1$ or $\overline{W}$ going high or E2 going low to the end of the write cycle.
13. During this period, I/O pins are in the output state, therefore; the input signals of the opposite phase to the outputs must not be applied.
14. If the $\overline{E}1$ low transition occurs simultaneously with the $\overline{W}$ low transitions or after the $\overline{W}$ low transitions, output remains in a high-impedance state.
15. DQ0-DQ7 (OUT) is the same phase of the latest written data in this write cycle.
16. DQ0-DQ7 (OUT) is the read data of the next address.
17. If $\overline{E}1$ is low and E2 is high during this period, I/O pins are in the output state, therefore the input signals of opposite phase to the output must not be applied to them.

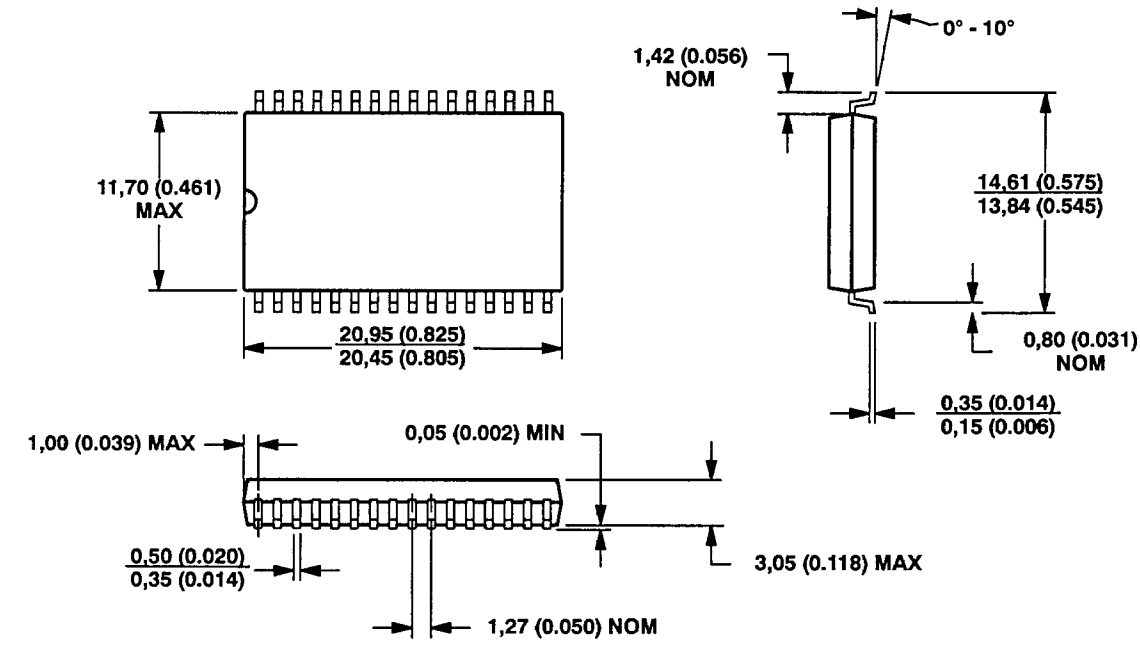
MECHANICAL DATA

32-pin 600-mil plastic dual-in-line package (NW suffix)



ALL DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

32-pin 525-mil plastic small outline package (DK suffix)



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