HARRIS

RFM15N05L/06L
RFP15N05L/06L

N-Channel Logic Level Power Field-Effect Transistors (L^2FET)

August 1991

Features

- 15A, 50V and 60V
- $r_{DS(ON)} = 0.14\Omega$
- Design Optimized for 5V Gate Drives
- Can be Driven Directly from QMOS, NMOS, TTL Circuits
- Compatible with Automotive Drive Requirements
- SOA is Power-Dissipation Limited
- Nanoscecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance
- Majority Carrier Device

Description

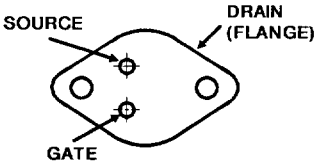
The RFM15N05L and RFM15N06L and the RFP15N05L and RFP15N06L are N-channel enhancmement-mode silicon-gate power field-effect transistors specifically designed for applications such as switching regulators, switching converters, motor drivers, relay drivers and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The RFM series types are supplied in the JEDEC TO-204AA steel package and the RFP series types in the JEDEC TO-220AB plastic package.

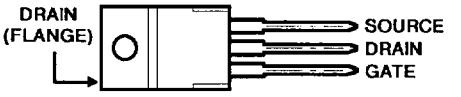
Because of space limitations branding (marking) on type RFP15N05L is F15N05L and on type RFP15N06L is F15N06L.

Package

TO-204AA
BOTTOM VIEW

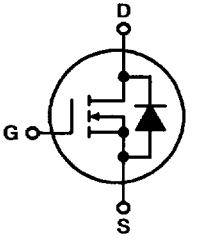


TO-220AB
TOP VIEW



Terminal Diagram

N-CHANNEL ENHANCEMENT MODE



Absolute Maximum Ratings ($T_C = +25^oC$) Unless Otherwise Specified

	RFM15N05L	RFM15N06L	RFP15N05L	RFP15N06L	UNITS
Drain-Source Voltage ..... V_{DS}	50	60	50	60	V
Drain-Gate Voltage ($R_{GS} = 1M\Omega$) ..... V_{DGR}	50	60	50	60	V
Continuous Drain Current					
RMS Continuous ..... I_D	15	15	15	15	A
Pulsed Drain Current ..... I_{DM}	40	40	40	40	A
Gate-Source Voltage ..... V_{GS}	±10	±10	±10	±10	V
Maximum Power Dissipation					
$T_C = +25^oC$ ..... P_D	75	75	60	60	W
Above $T_C = +25^oC$, Derate Linearly	0.6	0.6	0.48	0.48	W/^{o}C
Operating and Storage Junction Temperature Range ..... T_J, T_{STG}	-55 to +150	-55 to +150	-55 to +150	-55 to +150	^{o}C

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

File Number **1558.1**

ELECTRICAL CHARACTERISTICS, At Case Temperature (T_C = 25° C) unless otherwise specified

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS				UNITS
			RFM15N05L RFP15N05L		RFM15N06L RFP15N06L		
			MIN.	MAX.	MIN.	MAX.	
Drain-Source Breakdown Voltage	BV_{DSS}	I_D = 1 mA V_{GS} = 0	50	—	60	—	V
Gate-Threshold Voltage	$V_{GS(th)}$	V_{GS} = V_{DS} I_D = 1 mA	1	2	1	2	V
Zero-Gate Voltage Drain Current	I_{DSS}	V_{DS} = 40 V	—	1	—	—	μA
		V_{DS} = 50 V	—	—	—	1	
		T_C = 125° C V_{DS} = 40 V	—	50	—	—	
		V_{DS} = 50 V	—	—	—	50	
Gate-Source Leakage Current	I_{GSS}	V_{GS} = ±10 V V_{DS} = 0	—	100	—	100	nA
Drain-Source On Voltage	$V_{DS(on)}$[a]	I_D = 7.5 A V_{GS} = 5 V	—	1.05	—	1.05	V
		I_D = 15 A V_{GS} = 5 V	—	3.0	—	3.0	
Static Drain-Source On Resistance	$r_{DS(on)}$[a]	I_D = 7.5 A V_{GS} = 5 V	—	0.14	—	0.14	Ω
Forward Transconductance	g_{fs}[a]	V_{DS} = 10 V I_D = 7.5 A	4.0	—	4.0	—	mho
Input Capacitance	C_{iss}	V_{DS} = 25 V V_{GS} = 0 V f = 1 MHz	—	900	—	900	pF
Output Capacitance	C_{oss}		—	450	—	450	
Reverse-Transfer Capacitance	C_{rss}		—	200	—	200	
Turn-On Delay Time	$t_{d(on)}$	V_{DD} = 30 V I_D = 7.5 A R_{gen} = ∞ R_{gs} = 6.25 Ω V_{GS} = 5 V	16(typ)	40	16(typ)	40	ns
Rise Time	t_r		250(typ)	325	250(typ)	325	
Turn-Off Delay Time	$t_{d(off)}$		200(typ)	325	200(typ)	325	
Fall Time	t_f		225(typ)	325	225(typ)	325	
Thermal Resistance Junction-to-Case	$R\theta_{JC}$	RFM15N05L, RFM15N06L	—	1.67	—	1.67	°C/W
		RFP15N05L, RFP15N06L	—	2.083	—	2.083	

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS				UNITS
			RFM15N05L RFP15N05L		RFM15N06L RFP15N06L		
			MIN.	MAX.	MIN.	MAX.	
Diode Forward Voltage	V_{SD}[a]	I_{SD} = 7.5A	—	1.4	—	1.4	V
Reverse Recovery Time	t_{rr}	I_F = 4A, di_F/dt = 100A/μs	225 (typ.)		225 (typ.)		ns

[a] Pulsed: Pulse duration = 300 μs, duty cycle = 2%.

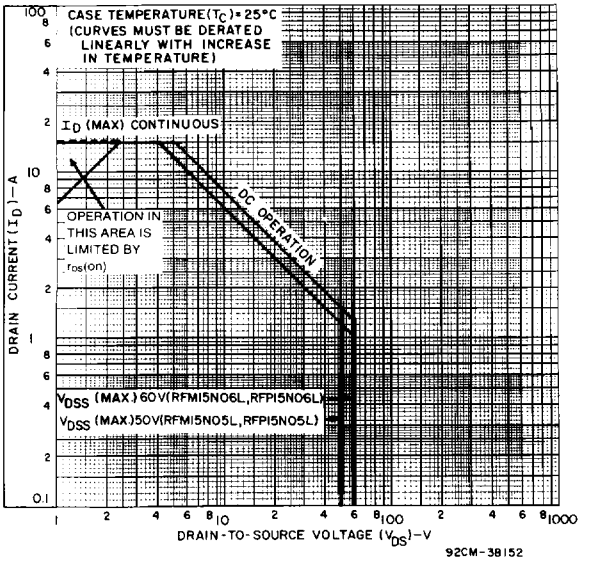


Fig. 1 - Maximum safe operating areas for all types.

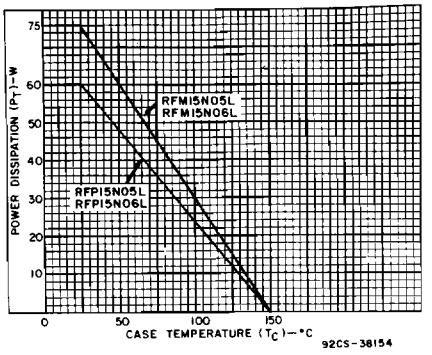


Fig. 2 - Power dissipation vs. case temperature derating curve for all types.

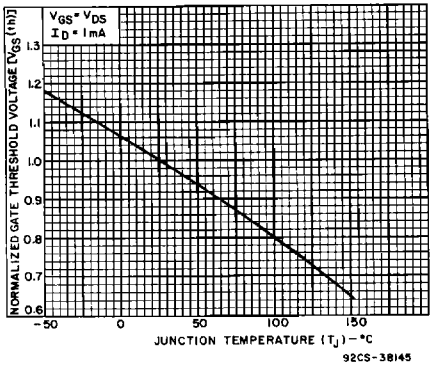


Fig. 3 - Typical normalized gate threshold voltage as a function of junction temperature for all types.

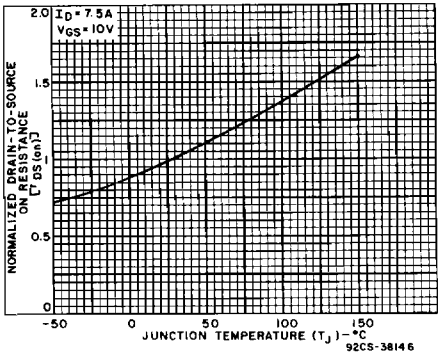


Fig. 4 - Normalized drain-to-source on resistance vs. junction temperature for all types.

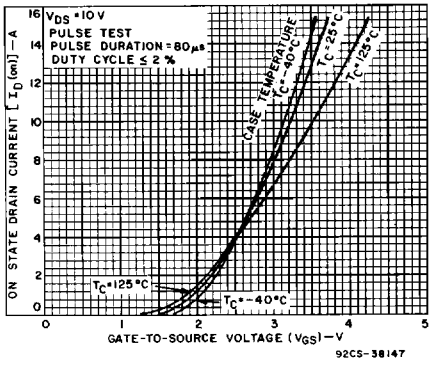


Fig. 5 - Typical transfer characteristics for all types.

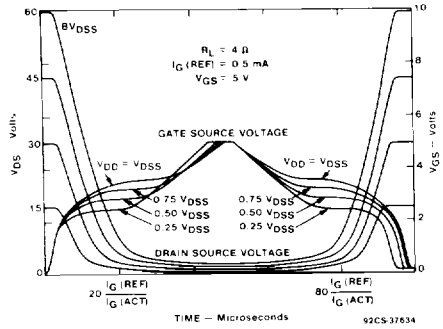


Fig. 6 - Normalized switching waveforms for constant gate-current. Refer to Harris application notes AN7254 and AN-7260.

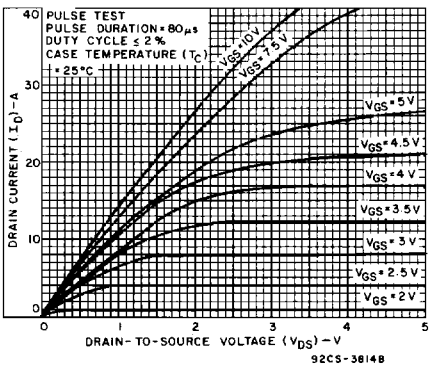


Fig. 7 - Typical saturation characteristics for all types.

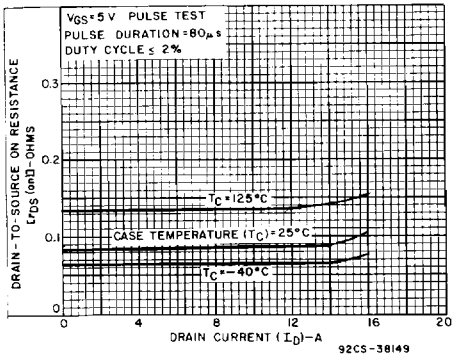


Fig. 8 - Typical drain-to-source on resistance as a function drain current for all types.

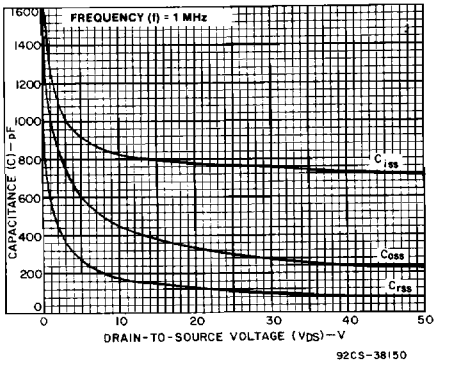


Fig. 9 - Capacitance as a function of drain-to-source voltage for all types.

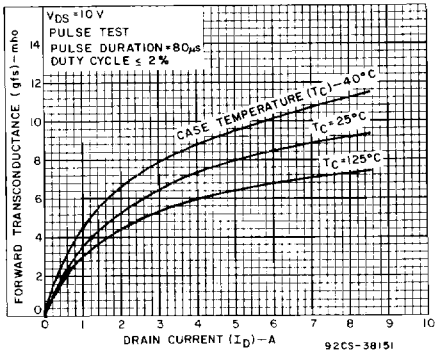


Fig. 10 - Typical forward transconductance as a function of drain current for all types.

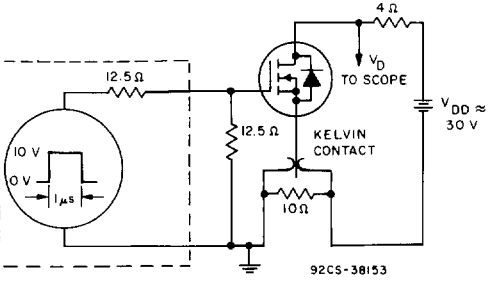


Fig. 11 - Switching Time Test Circuit.