82510

Asynchronous Serial Controller

The Intel CHMOS 82510 is designed to increase system efficiency in asynchronous environments such as modems or serial ports - including expanding performance areas: MCS-51 9-bit format and high speed async. The functional support provided in the 82510 is unparalleled - two baud rate generators/timers provide independent data rates or protocol timeouts; a crystal oscillator and smart modem I/O simplify system logic. New features - dual FIFOs and Control Character Recognition (CCR) - dramatically reduce CPU interrupts and increase software efficiency. All interrupts are maskable at two levels and the multipersonality I/O pins are configurable as desired.

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Quality Overview

- ISO-9001
- AS9120 certification
- Qualified Manufacturers List (QML) MIL-PRF-38535
    - Class Q Military
    - Class V Space Level
- Qualified Suppliers List of Distributors (QSLD)
    - Rochester is a critical supplier to DLA and meets all industry and DLA standards.

Rochester Electronics, LLC is committed to supplying products that satisfy customer expectations for quality and are equal to those originally supplied by industry manufacturers.

The original manufacturer's datasheet accompanying this document reflects the performance and specifications of the Rochester manufactured version of this device. Rochester Electronics guarantees the performance of its semiconductor products to the original OEM specifications. 'Typical' values are for reference purposes only. Certain minimum or maximum ratings may be based on product characterization, design, simulation, or sample testing.

82510
ASYNCHRONOUS SERIAL CONTROLLER

- **Asynchronous Operation**
  - **— 5- to 9-Bit Character Format**
  - **— Baud Rate DC to 288k**
  - **— Complete Error Detection**
- **Multiple Sampling Windows**
- **Two, Independent, Four-Byte Transmit and Receive FIFOs with Programmable Threshold**
- **Two, 16-Bit Baud Rate Generators/ Timers**
- **System Clock Options**
  - **— On-Chip Crystal Oscillator**
  - **— External Clocks, Low/High Speed**
- **MCS-51 9-Bit Protocol Support**
- **IBM PC AT* (INS 8250A/16450®) Software Compatible**
- **Control Character Recognition**
- **CHMOS III with Power Down Mode**
- **Interrupts Maskable at Two Levels**
- **Auto Echo and Loopback Modes**
- **Seven I/O Pins, Dedicated and General Purpose**
- **28-Lead DIP and PLCC Packages**
  (See Packaging Spec., Order #: 231369)

The Intel CHMOS 82510 is designed to increase system efficiency in asynchronous environments such as modems or serial ports—including expanding performance areas: MCS-51 9-bit format and high speed async. The functional support provided in the 82510 is unparalleled—two baud rate generators/timers provide independent data rates or protocol timeouts; a crystal oscillator and smart modem I/O simplify system logic. New features—dual FIFOs and Control Character Recognition (CCR)—dramatically reduce CPU interrupts and increase software efficiency. The 82510's software versatility allows emulation of the INS8250A/16450 for IBM PC AT* compatibility or a high-performance mode, configured by 35 control registers. All interrupts are maskable at two levels. The multipersonality I/O pins are configurable as desired. A DPLL and multiple sampling of serial data improve data reliability for high-speed, asynchronous communication. The compact 28-pin 82510 is fabricated with CHMOS III technology and includes a software powerdown option.

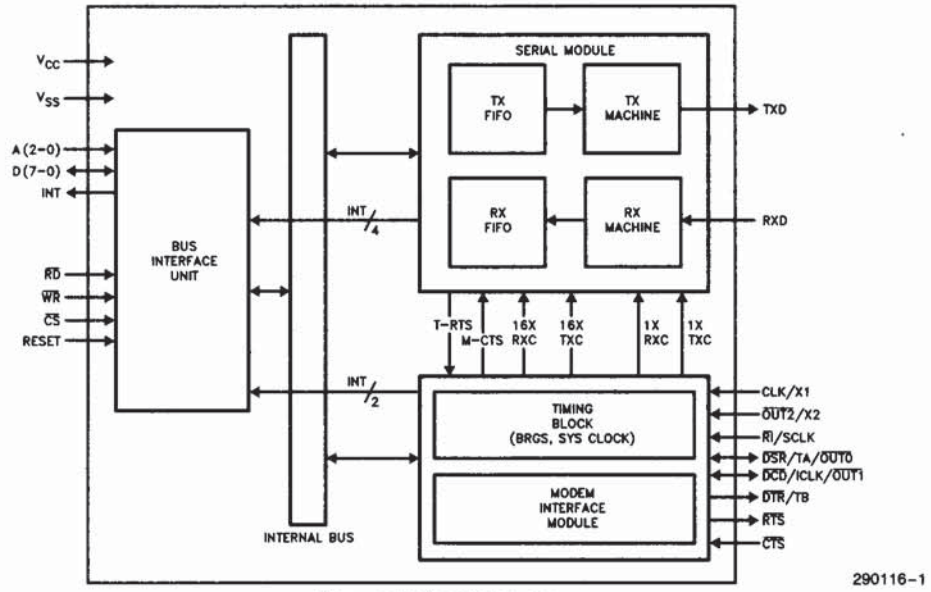

Figure 1. Block Diagram

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October 1989
Order Number: 290116-004

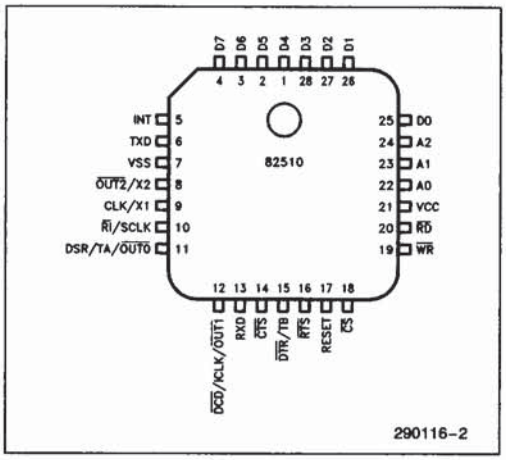

Figure 2. PLCC Pinout

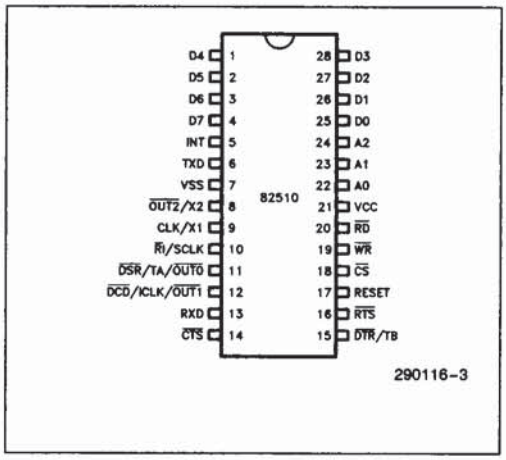

Figure 3. DIP Pinout

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82510 PINOUT DEFINITION

Symbol	Pin No.	Type	Name and Description
RESET	17	I	**RESET:** A high on this input pin resets the 82510 to the Default Wake-up mode.
$\overline{CS}$	18	I	**CHIP SELECT:** A low on this input pin enables the 82510 and allows read or write operations.
A2–A0	24-22	I	**ADDRESS PINS:** These inputs interface with three bits of the System Address Bus to select one of the internal registers for read or write.
D7–D0	4* 25	I/O	**DATA BUS:** Bi-directional, three state, eight-bit Data Bus. These pins allow transfer of bytes between the CPU and the 82510.
$\overline{RD}$	20	I	**READ:** A low on this input pin allows the CPU to read Data or Status bytes from the 82510.
$\overline{WR}$	19	I	**WRITE:** A low on this input allows the CPU to write Data or Control bytes to the 82510.
INT	5	O	**INTERRUPT:** A high on this output pin signals an interrupt request to the CPU. The CPU may determine the particular source and cause of the interrupt by reading the 82510 Status registers.
CLK/X1	9	I	**MULTIFUNCTION:** This input pin serves as a source for the internal system clock. The clock may be asynchronous to the serial clocks and to the processor clock. This pin may be used in one of two modes: CLK — in this mode an externally generated TTL compatible clock should be used to drive this input pin; X1 — in this mode the clock is internally generated by an on-chip crystal oscillator. This mode requires a crystal to be connected between this pin (X1) and the X2 pin. (See System Clock Generation.)
$\overline{OUT2}$/X2	8	O	**MULTIFUNCTION:** This is a dual function pin which may be configured to one of the following functions: $\overline{OUT2}$ — a general purpose output pin controlled by the CPU, only available when CLK/X1 pin is driven by an externally generated clock; X2 - this pin serves as an output pin for the crystal oscillator. *Note*: The configuration of the pin is done only during hardware reset. For more details refer to the System Clock Generation.
TXD	6	O	**TRANSMIT DATA:** Serial data is transmitted via this output pin starting at the Least Significant bit.

*Pins 28–25 and Pins 4–1.

82510 PINOUT DEFINITION (Continued)

Symbol	Pin No.	Type	Name and Description
RXD	13	I	**RECEIVE DATA:** Serial data is received on this input pin starting at the Least Significant bit.
$\overline{RI}$/SCLK	10	I	**MULTIFUNCTION:** This is a dual function pin which can be configured to one of the following functions. $\overline{RI}$ - Ring Indicator - Input, active low. This is a general purpose input pin accessible by the CPU. SCLK - This input pin may serve as a source for the internal serial clock(s), RxClk and/or TxClk. See Figure 12, BRG sources and outputs.
$\overline{DTR}$/TB	15	O	**MULTIFUNCTION:** This is a dual function pin which may be configured to one of the following functions. $\overline{DTR}$ - Data Terminal Ready. Output, active low. This is a general purpose output pin controlled by the CPU. TB - This pin outputs the BRGB output signal when configured as either a clock generator or as a timer. When BRGB is configured as a timer this pin outputs a "timer expired pulse." When BRGB is configured as a clock generator it outputs the BRGB output clock.
$\overline{DSR}$/TA/ $\overline{OUT0}$	11	I/O	**MULTIFUNCTION:** This is a multifunction pin which may be configured to one of the following functions. $\overline{DSR}$ - Data Set Ready. Input, active low. This is a general purpose input pin accessible by the CPU. TA - This pin is similar in function to pin TB except it outputs the signals from BRGA instead of BRGB. $\overline{OUT0}$ - Output pin. This is a general purpose output pin controlled by the CPU.
$\overline{RTS}$	16	O	**REQUEST TO SEND:** Output pin, active low. This is a general purpose output pin controlled by the CPU. In addition, in automatic transmission mode this pin, along with $\overline{CTS}$, controls the transmission of data. (See Transmit modes for further detail.) During hardware reset this pin is an input. It is used to determine the System Clock Mode. (See System Clock Generation for further detail.)
$\overline{CTS}$	14	I	**CLEAR TO SEND:** Input pin, active low. In automatic transmission mode it directly controls the Transmit Machine. (See transmission mode for further details.) This pin can be used as a General Purpose Input.
$\overline{DCD}$/ICLK/ $\overline{OUT1}$	12	I/O	**MULTIFUNCTION:** This is a multifunction pin which may be configured to one of the following functions. $\overline{DCD}$ - Data Carrier Detected. Input pin, active low. This is a general purpose input pin accessible by the CPU. ICLK - This pin is the output of the internal system clock. $\overline{OUT1}$ - General purpose output pin. Controlled by the CPU.
V_{CC}	21	P	**V_{CC}:** Device power supply.
V_{SS}	7	P	**V_{SS}:** Ground.

Table 1. Multifunction Pins

Pin #	I/O	Timing	Modem
8	*$\overline{OUT2}$	X2	—
9	—	*CLK/X1	—
10	—	SCLK	*$\overline{RI}$
11	$\overline{OUT0}$	TA	*$\overline{DSR}$
12	$\overline{OUT1}$	ICLK	*$\overline{DCD}$
14	—	—	*$\overline{CTS}$
15	—	TB	*$\overline{DTR}$
16	—	—	*$\overline{RTS}$

*Default

GENERAL DESCRIPTION

The 82510 can be functionally divided into seven major blocks (See Fig 1): Bus Interface Unit, Timing Unit, Modem Module, Tx FIFO, Rx FIFO, Tx Machine, and Rx Machine. Six of these blocks (all except Bus Interface Unit) can generate block interrupts. Three of these blocks can generate second-level interrupts which reflect errors/status within the block (Receive Machine, Timing Unit, and the Modem Module).

The Bus interface unit allows the 82510 to interface with the rest of the system. It controls access to device registers as well as generation of interrupts to the external world. The FIFOs buffer the CPU from the Serial Machines and reduce the interrupt overhead normally required for serial operations. The threshold (level of occupancy in the FIFO which will generate an interrupt) is programmable for each FIFO. The timing unit controls generation of the system clock through either its on-chip crystal oscillator, or an externally generated clock. It also provides two Baud Rate Generators/Timers with various options and modes to support serial communication.

FUNCTIONAL DESCRIPTION

CPU Interface

The 82510 has a simple demultiplexed Bus Interface, which consists of a bidirectional three-state eight-bit, data bus and a three-bit address bus. An Interrupt pin along with the Read, Write and Chip Select are the remaining signals used to interface with the CPU. The three address lines along with the Bank Pointer register are used to select the registers. The 82510 is designed to interface to all Intel microprocessor and microcontroller families. Like most other I/O based peripherals it is programmed through its registers to support a variety of functions.

Its register set can be used in 8250A/16450 compatibility or High Performance modes. The 8250A/16450 mode is the default wake-up mode in which only the 8250A/16450 compatible registers are accessible. The remaining registers are default configured to support 8250A/16450 emulation.

Software Interface

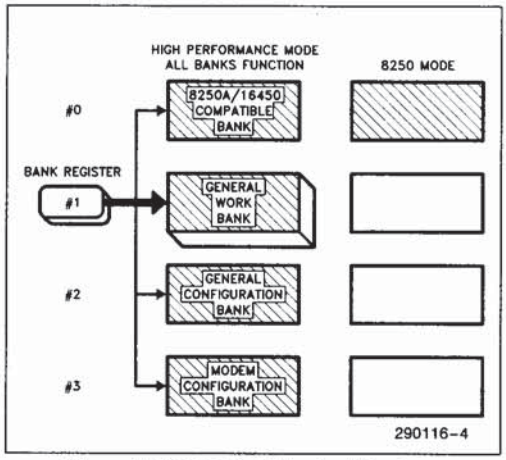


Figure 4. 82510 Register Architecture

The 82510 is configured and controlled through its 35 registers which are divided into four banks. Only one bank is accessible at any one time. The bank switching is done by changing the contents of the bank pointer (GIR/BANK–BANK0, BANK1). The banks are logically grouped into 8250A/16450 compatible (0), General Work Bank (1), General Configuration (2), and Modem Configuration (3). The 8250A/16450 compatible bank (Bank 0) is the default bank upon power up.

The 82510 registers can be categorized under the following:

Table 2. 82510 Register/Block Functions

	Status	Enable	Configuration	Command	Data
FIFO	FLR	—	FMD	—	—
MODEM	MSR	MIE	PMD	MCR	—
RX	RST, RXF	RIE	RMD	RCM	RXD, RXF
TX	LSR	LSR	TMD	TCM	TXD, TXF
TIMER	TMST	TMIE	CLCF, BACF, BBCF	TMCR	BBL, BBH BAL, BAH
DEVICE	GSR, GIR	GER	IMD	ICM	—
8250	LSR, MSR, GIR	GER	LCR, MCR	MCR	TXD, RXD BAL, BAH

8250 Compatibility

Upon power up or reset, the 82510 comes up in the default wake up mode. The 8250A/16450 compatible bank, bank zero, is the accessible bank and all the other registers are configured via their default values to support this mode. An 18.432 MHz crystal frequency is necessary.

Table 3. 8250A/16450 Compatible Registers

	82510 Registers (Bank 0)		8250A Registers	
Address	**Read**	**Write**	**Read**	**Write**
00 (DLAB = 0)	RxD	TxD	RBR	THR
01 (DLAB = 0)	GER	GER	IER	IER
00 (DLAB = 1)	BAL	BAL	DLL	DLL
01 (DLAB = 1)	BAH	BAH	DLM	DLM
02	GIR/BANK	BANK	IIR	—
03	LCR	LCR	LCR	LCR
04	MCR	MCR	MCR	MCR
05	LSR	LSR	LSR	LSR
06	MSR	MSR	MSR	MSR
07	ACR0	ACR0	SCR	SCR

Table 4. Default Wake-Up Mode

RxD	—	ACR1	00H	RxF	—
TxD	—	RIE	1EH	TxF	—
BAL	02H	RMD	00H	TMST	30H
BAH	00H	CLCF	00H	TMCR	—
GER	00H	BACF	04H	FLR	00H
GIR/BANK	01H	BBCF	84H	RCM	—
LCR	00H	PMD	FCH	TCM	—
MCR	00H	MIE	0FH	GSR	12H
LSR	60H	TMIE	00H	ICM	—
MSR	00H	BBL	05H	FMD	00H
ACR0	00H	BBH	00H	TMD	00H
RST	00H			IMD	0CH

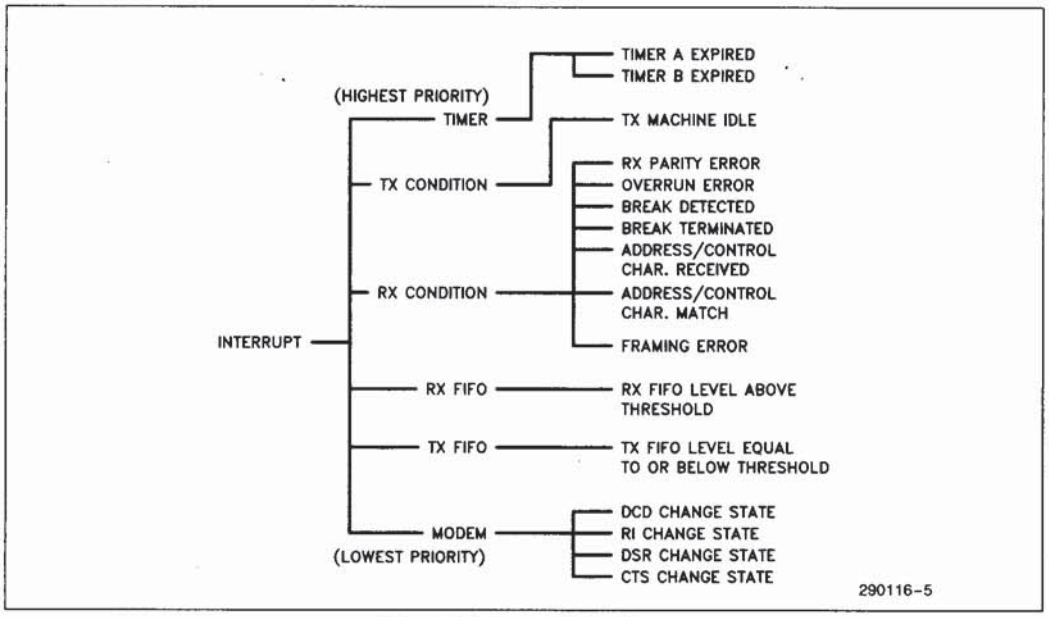


Figure 5. Interrupt Structure

Interrupts

There are two levels of interrupt/status reporting within the 82510. The first level is the block level interrupts such as RX FIFO, Tx FIFO, Rx Machine, Tx Machine, Timing unit, and Modem Module. The status of these blocks is reported in the General Status and General Interrupt Registers. The second level is the various sources within each block; only three of the blocks generate second level interrupts (Rx Machine, Timing Unit, and Modem Module). Interrupt requests are maskable at both the block level and at the individual source level within the module. If more than one unmasked block requests interrupt service an on-chip interrupt controller will resolve contention on a priority basis (each block has a fixed priority). An interrupt request from a particular block is activated if one of the unmasked status bits within the status register for the block is set. A CPU service operation, e.g., reading the appropriate status register, will reset the status bits.

ACKNOWLEDGE MODES

The interrupt logic will assert the INT pin when an interrupt is coded into the General Interrupt register. The INT pin is forced low upon acknowledgment. The 82510 has two modes of interrupt acknowledgment:

1. Manual Acknowledge

The CPU must issue an explicit Interrupt Acknowledge command via the Interrupt Acknowledge bit of the Internal Command register. As a result the INT pin is forced low for two clocks and then updated.

2. Automatic Acknowledge

As opposed to the Manual Acknowledge mode, when the CPU must issue an explicit interrupt acknowledge command, an interrupt service operation is considered as an automatic acknowledgment. This forces the INT pin low for two clock cycles. After two cycles the INT pin is updated, i.e., if there is still an active non-masked interrupt request the INT pin is set HIGH.

INTERRUPT SERVICE

A service operation is an operation performed by the CPU, which causes the source of the 82510 interrupt to be reset (it will reset the particular status bit causing the interrupt). An interrupt request within the 82510 will not reset until the interrupt source has been serviced. Each source can be serviced in two or three different ways; one general way is to disable the particular status bit causing the interrupt, via the corresponding block enable register. Setting the appropriate bit of the enable register to zero will mask off the corresponding bit in the status register, thus causing an edge on the input line to the interrupt logic. The same effect can be achieved by masking

off the particular block interrupt request in GSR via the *General Enable Register.* Another method, which is applicable to all sources, is to issue the Status Clear command from the *Internal Command Register.* The detailed service requirements for each source are given below:

Table 5. Service Procedures

Interrupt Source	Status Bits & Registers	Interrupt Masking	Specific Service
Timers	TMST (1–0) GSR (5)	TMIE (1–0) GER (5)	Read TMST
Tx Machine	GSR (4) LSR (6)	GER (4)	Write Character to tX FIFO
Rx Machine	LSR (4–1) RST (7–1) GSR (2)	RIE (7–1) GER (2)	Read RST or LSR Write 0 to bit in RST/LSR
Rx FIFO	RST/LSR (0) GSR (0)	GER (0)	Write 0 to LSR/RST Bit zero. Read Character
Tx FIFO	LSR (5) GSR (1)	GER (1)	Write to FIFO Read GIR(1)
Modem	MSR (3-0) GSR (3)	MIE (3-0) GER (3)	Read MSR write 0 into the appropriate bits of MSR (3–0).

NOTE:
1. Only if pending interrupt is Tx FIFO.

System Clock Generation

The 82510 has two modes of System Clock Operation. It can accept an externally generated clock, or it can use a crystal to internally generate its system clock.

CRYSTAL OSCILLATOR

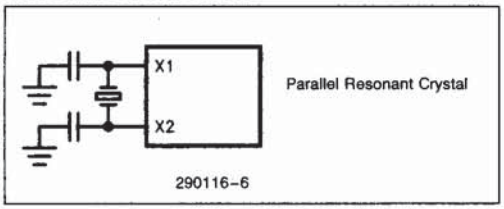


Figure 6. Crystal Oscillator

The 82510 has an on-chip oscillator to generate its system clock. The oscillator will take the inputs from a crystal attached to the X1 and X2 pins. This mode is configured via a hardware strapping option on $\overline{RTS}$.

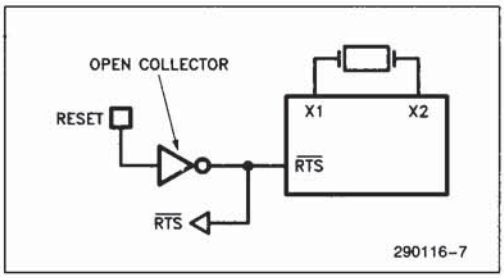


Figure 7. Strapping Option

During hardware reset the $\overline{RTS}$ pin is an input; it is weakly pulled high from within and then checked. If it is driven low externally then the 82510 is configured for the Crystal Oscillator; otherwise an external clock is expected.

EXTERNALLY GENERATED SYSTEM CLOCK

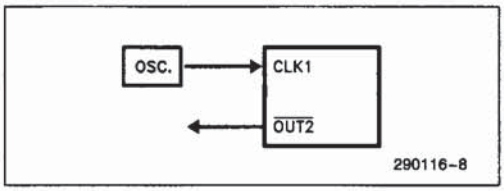


Figure 8. External Clock

This is the default configuration. Under normal conditions the system clock is divided by two; however, the user may disable divide by two via a hardware strapping option on the $\overline{DTR}$ pin. The Hardware strapping option is similar to the one used on the $\overline{RTS}$ pin. It is forbidden to strap both $\overline{DTR}$ and $\overline{RTS}$.

Transmit

The two major blocks involved in transmission are the Transmit FIFO and the Transmit Machine. The Tx FIFO acts as a buffer between the CPU and the Tx Machine. Whenever a data character is written to the Transmit Data register, it, along with the Transmit Flags (if applicable), is loaded into the Tx FIFO.

TX FIFO

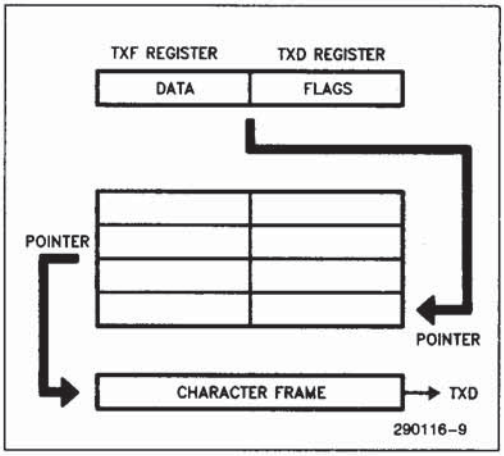


Figure 9. Tx FIFO

The Tx FIFO can hold up to four, eleven-bit characters (nine-bits data, parity, and address flag). It has separate read and write mechanisms. The read and write pointers are incremented after every operation to allow data transfer to occur in a First In First Out fashion. The Tx FIFO will generate a maskable interrupt when the level in the FIFO is below, or equal to, the Threshold. The threshold is user programmable.

For example, if the threshold equals two, and the number of characters in the Tx FIFO decreases from three to two, the FIFO will generate an interrupt. The threshold should be selected with regard to the system's interrupt service latency.

NOTE:
There is a one character transmission delay between FIFO empty and Transmitter Idle, so a threshold of zero may be selected without getting an underrun condition. Also if more than four characters are written to the FIFO an overrun will occur and the extra character will not be written to the Tx FIFO. This error will not be reported to the CPU.

TX MACHINE

The Tx Machine reads characters from the Tx FIFO, serializes the bits, and transmits them over the TXD pin according to the timing signals provided for transmission. It will also generate parity, transmit break (upon CPU request), and manage the modem handshaking signals ($\overline{CTS}$ and $\overline{RTS}$) if configured so. The Tx machine can be enabled or disabled through the Transmit Command register or $\overline{CTS}$. If the transmitter is disabled in the middle of a character transmission the transmission will continue until the end of the character; only then will it enter the disable state.

TRANSMIT CLOCKS

There are two modes of transmission clocking, 1X and 16X. In the 1X mode the transmitted data is synchronous to the transmit clock as supplied by the SCLK pin. In this mode stop-bit length is restricted to one or two bits only. In the 16X mode the data is not required to be synchronous to the clock. (Note: The Tx clock can be generated by the BRGs or from the SCLK pin.)

MODEM HANDSHAKING

The transmitter has three modes of handshaking.

Manual Mode—In this mode the $\overline{CTS}$ and $\overline{RTS}$ pins are not used by the Tx Machine (transmission is started regardless of the $\overline{CTS}$ state, and $\overline{RTS}$ is not forced low). The CPU may manage the handshake itself, by accessing the $\overline{CTS}$ and $\overline{RTS}$ signals through the MODEM CONTROL and MODEM STATUS registers.

Semi-Automatic Mode—In this mode the $\overline{RTS}$ pin is activated whenever the transmitter is enabled. The $\overline{CTS}$ pin's state controls transmission. Transmission is enabled only if $\overline{CTS}$ is active. If $\overline{CTS}$ becomes inactive during transmission, the Tx Machine will complete transmission of the current character and then go to the inactive state until $\overline{CTS}$ becomes active again.

Automatic Mode—This mode is similar to the semi-automatic mode, except that $\overline{RTS}$ will be activated as long as the transmitter is enabled and there are more characters to transmit. The CPU need only fill the FIFO, the handshake is done by the Tx Machine. When both the shift register and the FIFO are empty $\overline{RTS}$ automatically goes inactive. (Note: The $\overline{RTS}$ pin can be forced to the active state by the CPU, regardless of the handshaking mode, via the MODEM CONTROL register.)

Receive

The 82510 reception mechanism involves two major blocks; the Rx Machine and the Rx FIFO. The Rx Machine will assemble the incoming character and its associated flags and then LOAD them on to the Rx FIFO. The top of the FIFO may be read by reading the Receive Data register and the Receive Flags Register. The receive operation can be done in two modes. In the *normal* mode the characters are received in the standard Asynchronous format and only control characters are recognized. In the *ulan* mode, the nine bit protocol of the MCS-51 family is supported and the ulan Address characters, rather than Control Characters are recognized.

RX FIFO

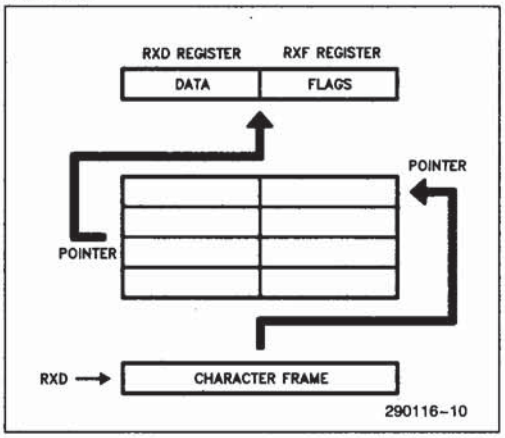


Figure 10. Rx FIFO

The Rx FIFO is very similar in structure and basic operation to the Tx FIFO. It will generate a maskable interrupt when the FIFO level is above the threshold. The Rx FIFO can also be configured to operate as a one-byte buffer. This mode is used for 8250 compatible software drivers. An overrun will occur when the FIFO is full and the Rx Machine has a new character for the FIFO. In this situation the oldest character is discarded and the new character is loaded from the Rx Machine. An Overrun error bit will also be set in the RECEIVE STATUS and LINE STATUS registers.

The user has the option to disable the loading of incoming characters on to the Rx FIFO by using the UNLOCK/LOCK FIFO commands. (See RECEIVE COMMAND register.) When the Rx FIFO is locked, it will ignore load requests from the Rx Machine, and thus the received characters will not be loaded into the FIFO and may be lost (if another character is received). These two commands are useful when the CPU is not willing to receive characters, or is waiting for specific Control/Address characters. In uLAN mode there are three options of address recognition, each of these options varies in the amount of CPU offload, and degree of FIFO control through OPEN/LOCK FIFO commands.

Automatic Mode—In this mode the Rx Machine will open the FIFO whenever an Address Match occurs; it will LOCK the FIFO if an address mismatch occurs.

Semi-Automatic Mode—In this mode the Rx Machine will open the FIFO whenever an address character is received. It will not lock the FIFO if the Address does not match. The user is responsible for locking the Rx FIFO.

Manual Mode—In this mode the Rx Machine does not control the FIFO automatically; however, the user may UNLOCK/LOCK the FIFO by using the RECEIVE COMMAND register.

RX MACHINE

The RX Machine has two modes of clocking the incoming data—16X or 1X. In 16X synchronization is done internally; in the 1X mode the data must be synchronous to the SCLK pin input. The Rx Machine synchronizes the data, passes it through a digital filter to filter out the spikes, and then uses the voting counter to generate the data bit (multiple sampling of input RXD). Bit polarity decisions are made on the basis of majority voting; i.e., if the majority of the samples are "1" the result is a "1" bit. If all samples are not in agreement then the bit is also reported as a noisy bit in the RECEIVE FLAGS register. The sampling window is programmable for either 3/16 or 7/16 samples. The 3/16 mode is useful for high frequency transmissions, or when serious RC delays are expected on the channel. The 7/16 is best suited for noisy media. The Rx machine also has a DPLL to overcome frequency shift problems; however, using it in a very noisy environment may increase the error, so the user can disable the DPLL via the Receive Mode register. The Rx Machine will generate the parity and the address marker as well as any framing error indications.

Start Bit Detection—The falling edge of the Start bit resets the DPLL counter and the Rx Machine starts sampling the input line (the number of samples is determined by the configuration of the sampling window mode). The Start bit verification can be done through either a majority voting system or an absolute voting system. The absolute voting requires that all the samples be in agreement. If one of the samples does not agree then a false Start bit is determined and the Rx Machine returns to the Start Bit search Mode. Once a Start bit is detected the Rx Machine will use the majority voting sampling window to receive the data bits.

Break Detection—If the input is low for the entire character frame including the stop Bit, then the Rx Machine will set Break Detected as well as Framing Error in the RECEIVE STATUS and LINE STATUS registers. It will push a NULL character onto the Rx FIFO with a framing-error and Break flag (As part of the Receive Flags). The Rx Machine then enters the Idle state. When it sees a mark it will set Break Terminated in RECEIVE STATUS and LINE STATUS registers and resume normal operation.

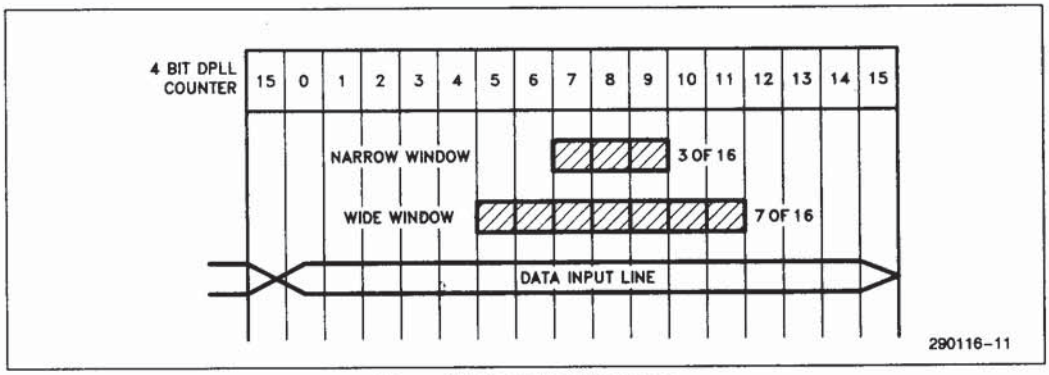


Figure 11. Sampling Windows

Control Characters—The Rx machine can generate a maskable interrupt upon reception of standard ASCII or EBCDIC control characters, or an Address marker is received in the uLAN mode. The Rx machine can also generate a maskable interrupt upon a match with programmed characters in the Address/Control Character 0 or Address/Control Character 1 registers.

Table 6. Control Character Recognition

CONTROL CHARACTER RECOGNITION	
A}	STANDARD SET
	■ ASCII: 000X XXXX + 0111 1111 (ASCII DEL) (00 - 1FH + 7 FH)
	OR
	■ EBCDIC: 00XX XXXX (00 - 3FH)
B}	User Programmed
	■ ACR0, ACR1 XXXX XXXX REGISTERS

Baud-Rate Generators/Timers

The 82510 has two-on-chip, 16-bit baud-rate generators. Each BRG can also be configured as a Timer, and is completely independent of the other. This can be used when the Transmit and Receive baud rates are different. The mode, the output, and the source of each BRG is configurable, and can also be optionally output to external devices via the TA, TB pins (see Fig. 12. BRG Sources and Outputs).

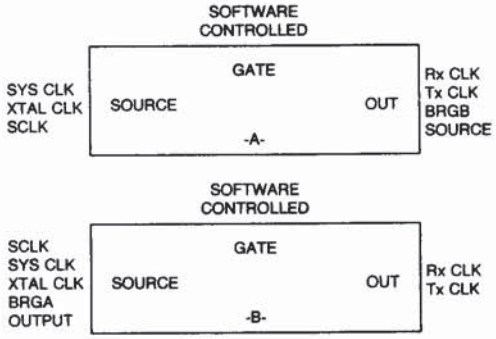


Figure 12. BRG Sources and Outputs

BAUD RATE GENERATION

The Baud Rate is generated by dividing the source clock with the divisor count. The count is loaded from the divisor count registers into a count down register. A 50% duty cycle is generated by counting down in steps of two. When the count is down to 2 the entire count is reloaded and the output clock is toggled. Optionally the two BRGs may be cascaded to provide a larger divisor. Note that this is the default configuration and used for 8250A/16450 emulation.

$$f_O = f_{in}/Divisor$$

where $f$in is the input clock frequency and Divisor is the count loaded into the appropriate count registers. System clock frequencies can be selected (4 → 9.216 MHz) to eliminate baud rate error for high baud rates.

Table 7. Standard Baud Rates

Bit Rate	16x Divisor	% Error
110	5236 (1474h)	.007%
300	1,920 (780h)	—
1200	480 (1E0h)	—
2400	240 (F0h)	—
9600	60 (3Ch)	—
19,200	30 (1Eh)	—
38,400	15 (0Fh)	—
56,000	10 (0Ah)	2.8%
288,000	2 (02h)	—

Source CLK = Internal Sys. Clk
= 18.432 MHz/2 (Crystal)
= 9.216 MHz (External 1X clock)

NOTE:
Internal system clock is ½ crystal frequency or ½ external clock frequency when using ÷2 clock option.

The BRG counts down in increments of two and then is divided by two to generate a 50% duty cycle; however, for odd divisors it will count down the first time by one. All subsequent countdowns will then continue in steps of two. In those cases the duty cycle is no longer exactly 50%. The deviation is given by the following equation:

$$\text{deviation} = 1/(2 \cdot \text{divisor})$$

The BRG can operate with any divisor between 1 and 65,535; however, for divisors between 1 and 3 the duty cycle is as follows:

Table 8. Duty Cycles

Divisor	Duty Cycle
3	33%
2	50%
1	Same as Source
0	FORBIDDEN

Timer Mode

Each of the 82510 BRGs can be used as Timers. The Timer is used to generate time delays by counting the internal system clock. When enabled the Timer uses the count from the Divisor/Count registers to count down to 1. Upon terminal count a maskable Timer Expired interrupt is generated. The delay between the trigger and the terminal count is given by the following equation:

$$\text{Delay} = \text{Count} \cdot (\text{System Clock Period})$$

To start counting, the Timer has to be triggered via the Start Timer Command. To restart the Timer after terminal count or while counting, the software has to issue the trigger command again. While counting the Timer can be enabled or disabled by using a software controlled Gate. It is also possible to output a pulse generated upon terminal count through the TA or TB pins.

In 1X clock mode the only clock source available is the SCLK pin. The serial machines (both Tx Machine and Rx Machine) can independently use one of two clock modes, either 1X or 16X. Also no configuration changes are allowed during operation as each write in the BRG configuration registers causes a reset signal to be sent to the BRG logic. The mode or source clocks may be changed only after a Hardware or Software reset. The Divisor (or count, depending upon the mode) may be updated during operation unless the particular BRG machine is being used as a clock source for one of the serial machines, and the particular serial machine is in operation at the time. Loading the count registers with "0" is forbidden in all cases, and loading it with a "1" is forbidden in the Timer Mode only.

SERIAL DIAGNOSTICS

The 82510 supports two modes of Loopback operation, Local Loopback and Remote Loopback as well as an Echo mode for diagnostics and improved throughput.

LOCAL LOOPBACK

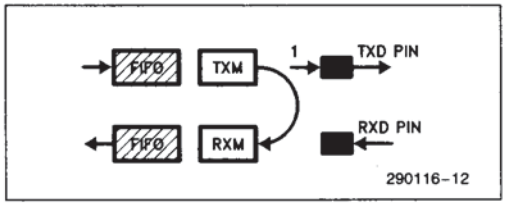


Figure 13. Local Loopback

The Tx Machine output and Rx Machine input are shorted internally, TXD pin output is held at Mark. This feature allows simulation of Transmission/Reception of characters and checks the Tx FIFO, Tx Machine, Rx Machine, and Rx FIFO along with the software without any external side effects. The modem outputs $\overline{OUT1}$, $\overline{OUT2}$, $\overline{DTR}$ and $\overline{RTS}$ are internally shorted to $\overline{RI}$, $\overline{DCD}$, $\overline{DSR}$ and $\overline{CTS}$ respectively. $\overline{OUT0}$ is held at a mark state.

REMOTE LOOPBACK

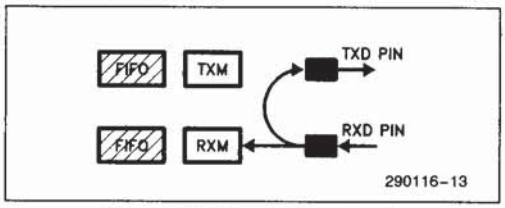


Figure 14. Remote Loopback

The TXD pin and RXD pin are shorted internally (the data is not sent on to the RX Machine). This feature allows the user to check the communications channel as well as the Tx and Rx pin circuits not checked in the Local Loopback mode.

AUTO ECHO

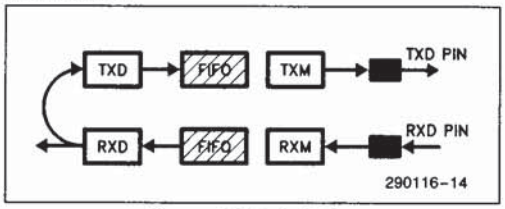


Figure 15. Auto Echo

In Echo Mode the received characters are automatically transmitted back. When the characters are read from the Rx FIFO they are automatically pushed back onto the Tx FIFO (the flags are also included). The Rx Machine baud rate must be equal to, or less than, the Tx Machine baud rate or some of the characters may be lost. The user has an option of preventing echo of special characters; Control Characters and characters with Errors.

Power Down Mode

The 82510 has a "power down" mode to reduce power consumption when the device is not in use. The 82510 powers down when the power down command is issued via the Internal Command Register (ICM). There are two modes of power down, Sleep and Idle.

In Sleep mode, even the system clock of the 82510 is shut down. The system clock source of the 82510 can either be the Crystal Oscillator or an external clock source. If the Crystal Oscillator is being used and the power down command is issued, then the 82510 will automatically enter the Sleep mode. If an external clock is being used, then the user must disable the external clock in addition to issuing the Power Down command, to enter the Sleep mode. The benefit of this mode is the increased savings in power consumption (typical power consumption in the Sleep mode is in the ranges of 100s of microAmps). However, upon wake up, the user must reprogram the device. To exit this mode the user can either issue a Hardware reset, or read the FIFO Level Register (FLR) and then issue a software reset. In either case the contents of the 82510 registers are not preserved and the device must be reprogrammed prior to operation. If the Crystal Oscillator is being used then the user must allow enough time for the oscillator to wake up before issuing the software reset.

The 82510 is in the idle mode when the Power Down command is issued and the system clock is still running (i. e. the system clock is generated externally and not disabled by the user). In this mode the contents of all registers and memory cells are preserved, however, the power consumption in this mode is greater than in the Sleep mode. Reading FLR will take the 82510 out of this mode.

NOTE:
The data read from FLR when exiting Power Down is invalid and should be ignored.

DETAILED REGISTER DESCRIPTION

Table 9. Register Map

Bank	Address	Read Register	Write Register
0 (NAS) 8250A/16450	0 (DLAB = 0)	RXD	TXD
	1 (DLAB = 0)	GER	GER
	0 (DLAB = 1)	BAL	BAL
	1 (DLAB = 1)	BAH	BAH
	2	GIR/BANK	BANK
	3	LCR	LCR
	4	MCR	MCR
	5	LSR	LSR
	6	MSR	MSR
	7	ACR0	ACR0
1 (WORK)	0	RXD	TXD
	1	RXF	TXF
	2	GIR/BANK	BANK
	3	TMST	TMCR
	4	FLR	MCR
	5	RST	RCM
	6	MSR	TCM
	7	GSR	ICM
2 (GENERAL CONF)	0	—	—
	1	FMD	FMD
	2	GIR/BANK	BANK
	3	TMD	TMD
	4	IMD	IMD
	5	ACR1	ACR1
	6	RIE	RIE
	7	RMD	RMD
3 (MODEM CONF)	0 (DLAB = 0)	CLCF	CLCF
	1 (DLAB = 0)	BACF	BACF
	0 (DLAB = 1)	BBL	BBL
	1 (DLAB = 1)	BBH	BBH
	2	GIR/BANK	BANK
	3	BBCF	BBCF
	4	PMD	PMD
	5	MIE	MIE
	6	TMIE	TMIE
	7	—	—

(1) ACRO is used in INS8250 as a Scratch-Pad Register
(2) DLAB = LCR Bit #7

The 82510 has thirty-five registers which are divided into four banks of register banks. Only one bank is accessible at any one time. The bank is selected through the BANK1-0 bits in the GIR/BANK register. The individual registers within a bank are selected by the three address lines (A2–0). The 82510 registers can be grouped into the following categories.

BANK ZERO 8250A/16450—COMPATIBLE BANK										
Register	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**	**Address**	**Default**
TxD (33)	Tx Data bit 7	Tx Data bit 6	Tx Data bit 5	Tx Data bit 4	Tx Data bit 3	Tx Data bit 2	Tx Data bit 1	Tx Data bit 0	0	—
RxD (35)	Rx Data bit 7	Rx Data bit 6	Rx Data bit 5	Rx Data bit 4	Rx Data bit 3	Rx Data bit 2	Rx Data bit 1	Rx Data bit 0	0	—
BAL (11)	BRGA LSB Divide Count (DLAB = 1)								0	02H
BAH (12)	BRGA MSB Divide Count (DLAB = 1)								1	00H
GER (16)	0	0	Timer Interrupt Enable	Tx Machine Interrupt Enable	Modem Interrupt Enable	Rx Machine Interrupt Enable	Tx FIFO Interrupt Enable	Rx FIFO Interrupt Enable	1	00H
GIR/BANK (21)	0	BANK Pointer bit 1	BANK Pointer bit 0	0	Active Block Int bit 2	Active Block Int bit 1	Active Block Int bit 0	Interrupt Pending	2	01H
LCR (2)	DLAB Divisor Latch Access bit	Set Break	Parity Mode bit 2	Parity Mode bit 1	Parity Mode bit 0	Stop bit Length bit 0	Character Length bit 1	Character Length bit 0	3	00H
MCR (32)	0	0	OUT 0 Complement	Loopback Control bit	OUT 2 Complement	OUT 1 Complement	RTS Complement	DTR Complement	4	00H
LSR (22)	0	TxM Idle	Tx FIFO Interrupt	Break Detected	Framing Error	Parity Error	Overrun Error	Rx FIFO Int Req	5	60H
MSR (27)	DCD Input Inverted	RI Input Inverted	DSR Input Inverted	CTS Input Inverted	State Change in DCD	State (H → L) Change in RI	State Change in DSR	State Change in CTS	6	00H
ACR0 (5)	Address or Control Character Zero								7	00H

BANK ONE—GENERAL WORK BANK										
Register	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**	**Address**	**Default**
TxD (33)	Tx Data bit 7	Tx Data bit 6	Tx Data bit 5	Tx Data bit 4	Tx Data bit 3	Tx Data bit 2	Tx Data bit 1	Tx Data bit 0	0	—
RxD (35)	Rx Data bit 7	Rx Data bit 6	Rx Data bit 5	Rx Data bit 4	Rx Data bit 3	Rx Data bit 2	Rx Data bit 1	Rx Data bit 0	0	—
RxF (24)	—	Rx Char OK	Rx Char Noisy	Rx Char Parity Error	Address or Control Character	Break Flag	Rx Char Framing Error	Ninth Data bit of Rx Char	1	—
TxF (34)	Address Marker bit	Software Parity bit	Ninth bit of Data Char	0	0	0	0	0	1	—
GIR/BANK (21)	0	BANK Pointer bit 1	BANK Pointer bit 0	0	Active Block Int bit 2	Active Block Int bit 1	Active Block Int bit 0	Interrupt Pending	2	01H
TMST (26)	—	—	Gate B State	Gate A State	—	—	Timer B Expired	Timer A Expired	3	30H
TMCR (31)	0	0	Trigger Gate B	Trigger Gate A	0	0	Start Timer B	Start Timer A	3	—
MCR (32)	0	0	OUT 0 Complement	Loopback Control bit	OUT 2 Complement	OUT 1 Complement	RTS Complement	DTR Complement	4	00H

NOTE:
The register number is provided as a reference number for the register description.

BANK ONE—GENERAL WORK BANK (Continued)										
Register	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**	**Address**	**Default**
FLR (25)	—	Rx FIFO Level			—	Tx FIFO Level			4	00H
RST (23)	Address/ Control Character Received	Address/ Control Character Match	Break Terminated	Break Detected	Framing Error	Parity Error	Overrun Error	Rx FIFO Interrupt Requested	5	00H
RCM (30)	Rx Enable	Rx Disable	Flush RxM	Flush Rx FIFO	Lock Rx FIFO	Open Rx FIFO	0	0	5	—
MSR (27)	DCD Complement	RI Input Inverted	DSR Input Inverted	CTS Input Inverted	State Change in DCD	State Change in RI	State Change in DSR	State Change in CTS	6	00H
TCM (29)	0	0	0	0	Flush Tx Machine	Flush Tx FIFO	Tx Enable	Tx Disable	6	—
GSR (20)	—	—	Timer Interrupt	TxM Interrupt	Modem Interrupt	RxM Interrupt	Tx FIFO Interrupt	Rx FIFO Interrupt	7	12H
ICM (28)	0	0	0	Software Reset	Manual Int Acknowledge Command	Status Clear	Power Down Mode	0	7	—

BANK TWO—GENERAL CONFIGURATION										
Register	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**	**Address**	**Default**
FMD (4)	0	0	Rx FIFO Threshold		0	0	Tx FIFO Threshold		1	00H
GIR/BANK (21)	0	BANK Pointer bit 1	BANK Pointer bit 0	0	Active Block Int bit 2	Active Block Int bit 1	Active Block Int bit 0	Interrupt Pending	2	01H
TMD (3)	Error Echo Disable	Control Character Echo Disable	9-bit Character Length	Transmit Mode		Software Parity Mode	Stop Bit Length		3	00H
IMD (1)	0	0	0	0	Interrupt Acknowledge Mode	Rx FIFO Depth	ulan Mode Select	Loopback or Echo Mode of Operation	4	0CH
ACR1 (6)	Address or Control Character 1								5	00H
RIE (17)	Address/ Control Character Recognition Interrupt Enable	Address/ Control Character Match Interrupt Enable	Break Terminate Interrupt Enable	Break Detect Interrupt Enable	Framing Error Interrupt Enable	Parity Error Interrupt Enable	Overrun Error Interrupt Enable	0	6	1EH
RMD (7)	Address/Control Character Mode		Disable DPLL	Sampling Window Mode	Start bit Sampling Mode	0	0	0	7	00H

BANK THREE—MODEM CONFIGURATION										
Register	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**	**Address**	**Default**
CLCF (8)	Rx Clock Mode	Rx Clock Source	Tx Clock Mode	Tx Clock Source	0	0	0	0	0	00H
BACF (9)	0	BRGA Clock Source	0	0	0	BRGA Mode	0	0	1	04H
BBL (13)	BRGB LSB Divide Count (DLAB = 1)								0	05H
BBH (14)	BRGB MSB Divide Count (DLAB = 1)								1	00H

BANK THREE—MODEM CONFIGURATION (Continued)										
Register	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**	**Address**	**Default**
GIR/BANK (21)	0	BANK Pointer bit 1	BANK Pointer bit 0	0	Active Block Int bit 2	Active Block Int bit 1	Active Block Int bit 0	Interrupt Pending	2	01H
BBCF (10)	BRGB Clock Source		0	0	0	BRGB Mode	0	0	3	84H
PMD (15)	DCD/ICLK/ OUT 1 Direction	DCD/ICLK/ OUT 1 Function	DSR/TA/ OUT 0 Direction	DSR/TA/ OUT 0 Function	RI/SCLK Function	DTR/TB Function	0	0	4	FCH
MIE (19)	0	0	0	0	DCD State Change Int Enable	RI State Change Int Enable	DSR State Change Int Enable	CTS State Change Int Enable	5	0FH
TMIE (18)	0	0	0	0	0	0	Timer B Interrupt Enable	Timer A Interrupt Enable	6	00H

2

CONFIGURATION

These read/write registers are used to configure the device. They may be read at anytime; however, they may be written to only when the device is idle. Typically they are written to only once after system power up. They are set to default values upon Hardware or Software Reset (Default Wake-Up Mode). The default values are chosen so as to allow the 82510 to be fully software compatible with the IBM PC Async Adapter (INS 8250A/ 16450) when in the default wakeup mode. The 82510 can operate in the High Performance mode by programming the configuration registers as necessary.

The configuration options available to the user are listed below.

Table 11. Configuration Options

Interrupt Acknowledge Mode
- Automatic
- Manual

Receive
- Sampling Window Size
- Start Bit Detection Mode
- DPLL Disable/Enable

μLAN (8051)
Address Recognition
- Manual, Semi-Automatic, Automatic

Diagnostics
- Loopback
  - Remote
  - Local
- Echo
  - Yes/No
  - Disable Error Echo
  - Disable Control/Address Char. Echo

FIFO
- RX FIFO Depth
- RX, TX Threshold

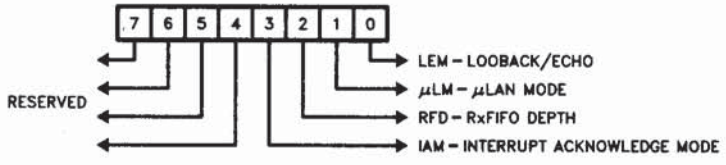
Clock Options
- RX, TX Clock Mode
  - 1X
  - 16X
- RX, TX Clock Source
  - BRGA
  - BRGB
- BRGA/B Operation Mode
  - Timer
  - BRG
- BRGA/B Divide Count
- BRGA/B Source
  - Sys Clock
  - SCLK Pin
  - BRGA Output (BRGB Only)

Control Character Recognition
- None
- Standard
  - ASCII
  - EBCDIC
- Two User Programmed

TX Operation
- RTS/CTS Control Manual, Semi-Automatic, Automatic
- Parity Mode
- Stop Bit Length
- Character Size

I/O Pins
- Select Function for Each Multifunction Pin
- Select Direction for Multifunction Pin (If Applicable)

1. IMD—INTERNAL MODE REGISTER



IMD—Internal Mode Register

This register defines the general device mode of operation. The bit functions are as follows:

7–4: Reserved

IAM: Interrupt Acknowledge Mode Bit

0 — Manual acknowledgement of pending interrupts
1 — Automatic acknowledgement of pending interrupts (upon CPU service)

This bit, when set, configures the 82510 for the automatic acknowledge mode. This causes the 82510 INT line to go low for two clock cycles upon service of the interrupt. After two clock cycles it is then updated. It is useful in the edge triggered mode. In manual acknowledgement mode the CPU must explicitly issue a command to clear the INT pin. (The INT pin then goes low for a minimum of two clock cycles until another enabled status register bit is set.)

RFD: Receive FIFO Depth

0 — Four Bytes
1 — One Byte

This bit configures the depth of the Rx FIFO. With a FIFO depth of one, the FIFO will act as a 1-byte buffer to emulate the 8250A.

ULM: uLAN Mode

0 — Normal Mode
1 — uLAN Mode

This bit, enables the 82510 to recognize and/or match address using the 9-bit MCS-51 asynchronous protocol.

LEM: Loopback/Echo Mode Select

This bit selects the mode of loopback operation, or the mode of echo operation; depending upon which operation mode is selected by the Modem Control register bit LC.

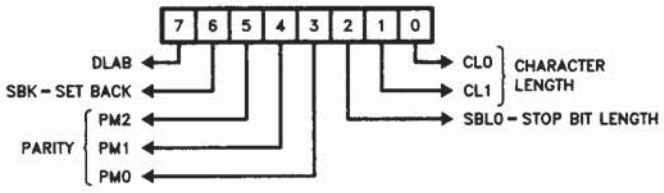
In *loopback* mode (Modem Control register bit LC = 1) it selects between local and remote loopback.

0 — Local Loopback
1 — Remote Loopback

In *echo* mode (Modem Control register bit LC = 0) it selects between echo or non-echo operation.

0 — No Echo
1 — Echo Operation

2. LCR—LINE CONFIGURE REGISTER



LCR—Line Configure Register

This register defines the basic configuration of the serial link.

DLAB—Divisor Latch Access Bit—This bit, when set, allows access to the Divisor Count registers BAL,BAH;BBL,BBH registers.

SBK—Set Break Bit—This bit will force the TxD pin low. The TxD pin will remain low (regardless of all activities) until this bit is reset.

PM2—PM0—Parity Mode Bits—These three bits combine with the SPF bit of the Transmit Mode register to define the various parity modes. See Table 12.

Table 12. Parity Modes

PM0	SPF	PM2	PM1	Function
0	X	X	X	No Parity
1	0	0	0	Odd Parity
1	0	0	1	Even Parity
1	0	1	0	High Parity
1	0	1	1	Low Parity
1	1	0	0	Software Parity

SBL0—Stop Bit Length—This bit, together with SBL1 and SBL2 bits of the Transmit Mode register, defines the Stop-bit lengths for transmission. The Rx machine can identify 3/4 stop bit or more. See Table 13.

Table 13. Stop Bit Length

SBL2	SBL1	SBL0	Stop Bit Length 16X	1X
0	0	0	4/4	—
0	0	1	6/4 or 8/4*	—
0	1	0	3/4	1
0	1	1	4/4	1
1	0	0	5/4	1
1	0	1	6/4	1
1	1	0	7/4	1
1	1	1	8/4	2

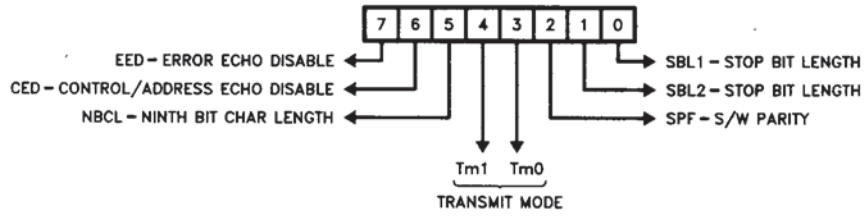
*6/4 if character length is 5 bits; else 8/4

CL0—CL1—Character Length Bits—These bits, together with the Transmit Mode register bit NBCL, define the character length. See Table 14.

Table 14. Character Length

NBCL	CL1	CL0	Character Length
0	0	0	5 BITS
0	0	1	6 BITS
0	1	0	7 BITS
0	1	1	8 BITS
1	0	0	9 BITS

3. TMD—Transmit Machine Mode Register



TMD—Transmit Machine Mode Register

This register together with the Line Configure Register defines the Tx machine mode of operation.

EED—Error Echo Disable—Disables Echo of characters received with errors (valid in echo mode only).

CED—Control Character Echo Disable—Disables Echo of characters recognized as control characters (or address characters in uLAN mode). Valid in echo mode only.

NBCL—Nine-Bit Length—This bit, coupled with LCR (CL0, CL1), selects Transmit/Receive character length of nine bits. See Table 14.

TM1—TM0—Transmit Mode—These bits select one of three modes of control over the $\overline{CTS}$ and $\overline{RTS}$ lines.

00—Manual Mode—In this mode the CPU has full control of the Transmit operation. The CPU has to explicitly enable/disable transmission, and activate/check the $\overline{RTS}$/$\overline{CTS}$ pins.

01—Reserved

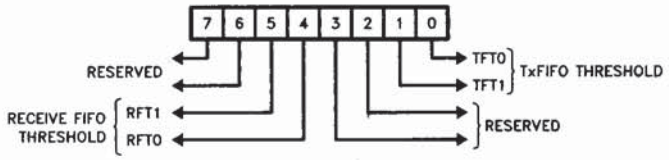
10—Semi-Automatic Mode—In this mode the 82510 transmits only when $\overline{CTS}$ input is active. The 82510 activates the $\overline{RTS}$ output as long as transmission is enabled.

11—Automatic Mode—In this mode the 82510 transmits only when $\overline{CTS}$ input is active. The $\overline{RTS}$ output is activated only when transmission is enabled and there is more data to transmit.

SPF—Software Parity Force—This bit defines the parity modes along with the PM0, PM1, and PM2 bits of the LCR register. When software parity is enabled the software must determine the parity bit through the TxF register on transmission, or check the parity bit in RxF upon reception. See Table 12.

SBL2—SBL1—Stop Bit Length—These bits, together with the SBL0 bit of the LCR register define the stop bit length. See Table 13.

4. FMD—FIFO MODE REGISTER



FMD—FIFO Mode Register

This register configures the Tx and Rx FIFO's threshold levels—the occupancy levels that can cause an interrupt.

7—6—Reserved

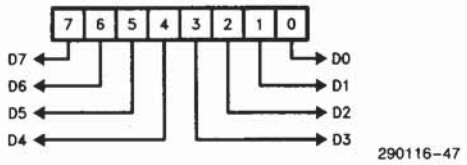
RFT1—RFT0—Receive FIFO Threshold—When the Rx FIFO occupancy is greater than the level indicated by these bits the Rx FIFO Interrupt is activated.

3—2—Reserved

TFT1—TFT0—Transmit FIFO Threshold—When the TX FIFO occupancy is less than or equal to the level indicated by these bits the Tx FIFO Interrupt is activated.

2

5. ACR0—ADDRESS/CONTROL CHARACTER REGISTER 0



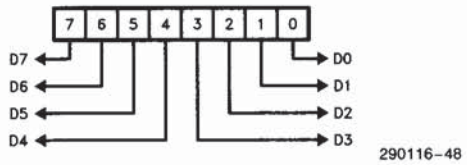
ARC0—Address/Control Character Register 0

This register contains a byte which is compared to each received character. The exact function depends on the configuration of the IMD register.

In normal mode this register may be used to program a special control character; a matched character will be reported in the RECEIVE STATUS register. The maximum length of the control characters is eight bits. If the length is less than eight bits then the character must be right justified and the leading bits be filled with zeros.

In uLAN mode this register contains the eight-bit station address for recognition. In this mode only incoming address characters (i.e., characters with address bit set) will be compared to these register. The PCRF bit in the RECEIVE STATUS register will be set when an Address or Control Character match occurs.

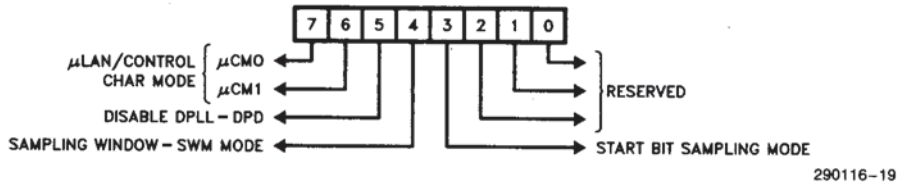
6. ACR1—ADDRESS/CONTROL CHARACTER REGISTER 1



ARC1—Address/Control Character Register 1

NOTE:
This register is identical in function to ACR0.

7. RMD—RECEIVE MACHINE MODE REGISTER



RMD—Receive Machine Mode Register

This register defines the Rx Machine mode of operation.

uCM0, uCM1—uLAN/Control Character Recognition Mode—In normal mode it defines the Control Character recognition mode. In ulan mode they define modes of address recognition.

In *uLAN* mode: selects the mode of address recognition.

00—Manual Mode—Rx Machine reports reception of any address character, via CRF bit of RECEIVE STATUS register, and writes it to the Rx FIFO.

01—Semi-Automatic Mode—Operates the same as Manual Mode but, in addition, the Rx Machine OPENS (unlocks) the Rx FIFO upon reception of any address characters. Subsequent received characters will be written into the FIFO. (Note: it is the user's responsibility to LOCK the FIFO if the address character does not match the station's address.)

10—Automatic Mode—The Rx Machine will OPEN (unlock) the Rx FIFO upon Address Match. In addition the Rx Machine LOCKs the Rx FIFO upon recognition of address mismatch; i.e., it controls the flow of characters into the Rx FIFO depending upon the results of the address comparison. If a match occurs it will allow characters to be sent to the FIFO; if a mismatch occurs it will keep the characters out of the FIFO by LOCKING it.

11—Reserved

In *normal* Mode: selects the mode of Standard Set Control Character Recognition (programmed control characters are always recognized).

00— No Standard Set Control Characters Recognized.

01— ASCII Control Characters (00H—1 FH + 7FH).

10— Reserved.

11— EBCDIC Control Character Recognized (00H – 3FH).

DPD—Disable Digital Phase Locked Loop—When set, disables the DPLL machine. (Note: using the DPLL in a very noisy media, may increase the error rate.)

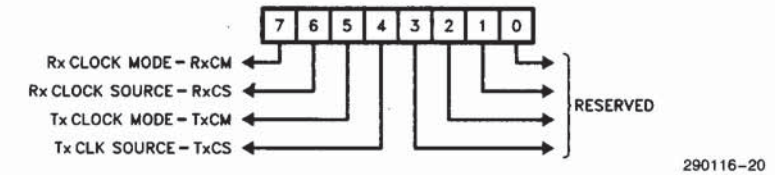
SWM—Sampling Window Mode—This bit controls the mode of data sampling:

0—Small Window, 3/16 sampling.
1—Large Window, 7/16 sampling.

SSM—Start Bit Sampling Mode—This bit controls the mode of Start Bit sampling.

0— Majority Voting for start bit. In this mode a majority of the samples determines the bit.
1— In this mode if one of the bit samples is not '0', the start bit will not be detected.

8. CLCF—CLOCKS CONFIGURE REGISTER



CLCF—Clocks Configure Register

This register defines the Transmit and Receive Code modes and sources.

RxCM—Rx Clock Mode—This bit selects the mode of the receive clock which is used to sample the received data.

0— 16X Mode.
1— 1X Mode. In this mode the receive data must be synchronous to the Rx Clock; supplied via the SCLK pin.

RxCS—Rx Clock Source—This bit selects the source of the internal receive clock in the case of 16X mode (as programmed by the RxCM bit above).

0—BRGB Output
1—BRGA Output

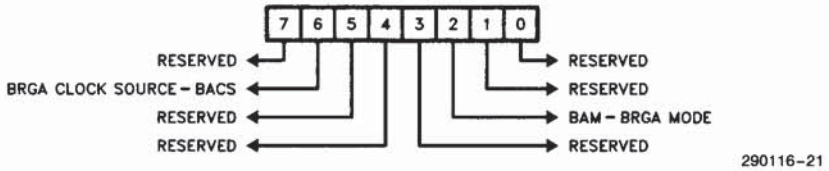
TxCM—Transmit Clock Mode—This bit selects the mode of the Transmit Data Clock, which is used to clock out the Transmit Data.

0— 16X Mode
1— 1X Mode. In this mode the Transmit data is synchronous to the Serial Clock; supplied via the SCLK pin.

TxCS—Transmit Clock Source—Selects the source of internal Transmit Clock in case of 16X mode.

0—BRGB Output.
1—BRGA Output.

9. BACF—BRGA CONFIGURATION REGISTER



BACF—BRGA Configuration Register

This register defines the BRGA clock sources and the mode of operation.

BACS—BRGA Clock Source—Selects the input clock source for Baud Rate Generator A.

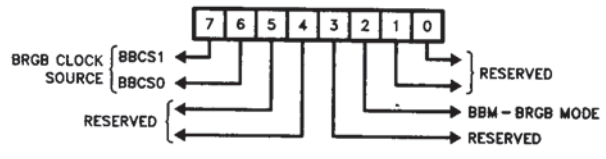
0—System Clock
1—SCLK Pin

This bit has no effect if BRGA is configured as a timer.

BAM—BRGA Mode of Operation—Selects between the Timer mode or the Baud Rate Generator Mode.

0— Timer Mode (in this mode the input clock source is always the system clock).
1— Baud Rate Generator Mode

10. BBCF—BRGB CONFIGURATION REGISTER



BBCF—BRGB Configuration Register

This register defines the BRGB clock sources and mode of operation. (Note: BRGB can also take its Input Clock from the output of BRGA.)

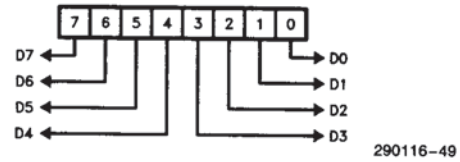
BBCS1, BBCS0—These two bits together define the input Clock Sources for BRGB. These bits have no effect when in the timer mode.

00— System Clock
01— SCLK Pin
10— BRGA Output
11— Reserved

BBM—BRGB Mode of Operation.

0— Timer Mode (In this mode the input clock source is always the system clock.)
1— BRG Mode

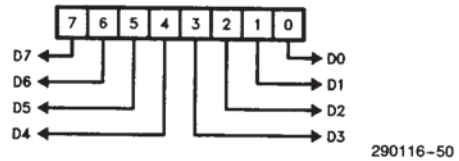
11. BAL—BRGA DIVIDE COUNT LEAST SIGNIFICANT BYTE



BAL—BRGA Divide Count Low Byte

This register contains the least significant byte of the BRGA divisor/count.

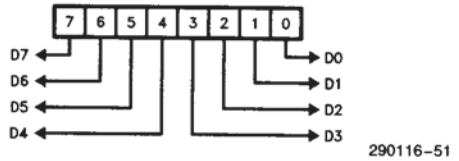
12. BAH—BRGA DIVIDE COUNT MOST SIGNIFICANT BYTE



BAH—BRGA Divide Count High Byte

This register contains the most significant byte of the BRGA divisor/count.

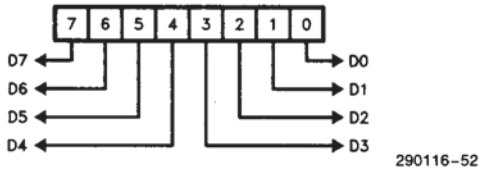
13. BBL—BRGB DIVIDE COUNT LEAST SIGNIFICANT BYTE



BBL—BRGB Divide Count Low Byte

This register contains the least significant byte of the BRGB divisor/count.

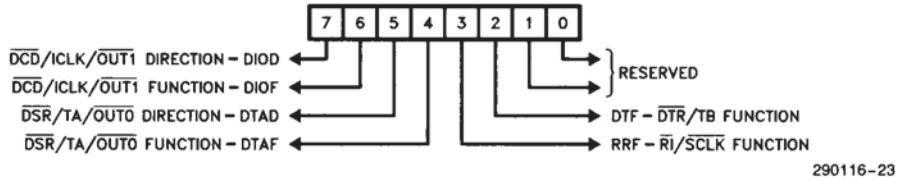
14. BBH—BRGB DIVIDE COUNT MOST SIGNIFICANT BYTE



BBH—BRGB Divide Count High Byte

This register contains the most significant byte of the BRGB divisor/count.

15. PMD—I/O PIN MODE REGISTER



PMD—I/O Pin Mode Register

This register is used to configure the direction and function of the multifunction pins. The following options are available on each pin.

1. Direction: Input or Output Pin.
   - 0— Defines the Pin as an output pin (general purpose or special function).
   - 1— Defines the pin as an input pin.
2. Function: General purpose or special purpose pin (no effect if the pin is programmed as an Input).
   - 0— special function output pin.
   - 1— general purpose output pin.
     DIOD—DCD/ICLK/OUT1 Direction.
   - 0— Output: ICLK or OUT1 (depending on bit DIOF)
   - 1— Input: DCD.
     DIOF—DCD/ICLK/OUT1 Function (output mode only).
   - 0— ICLK (Output of the Internal System Clock).
   - 1— OUT1 general purpose output, Controlled by MODEM CONTROL Register
     DTAD—DSR/TA/OUT0 Direction.
   - 0— Output: TA or OUT0 (Dependent upon DTAF).
   - 1— Input: DSR.
     DTAF—DSR/TA/OUT0 Direction (output mode only).
   - 0— TA (BRGA Output or Timer A Termination Pulse).
   - 1— OUT0 (general purpose output, controlled by MODEM CONTROL).
     RRF—RI/SCLK Function
   - 0— SCLK (Receive and/or Transmit Clock)
   - 1— RI
     DTF—DTR/TB Function
   - 0— TB (BRGB Output Clock on Timer B termination pulse depending upon the mode of BRGB).
   - 1— DTR

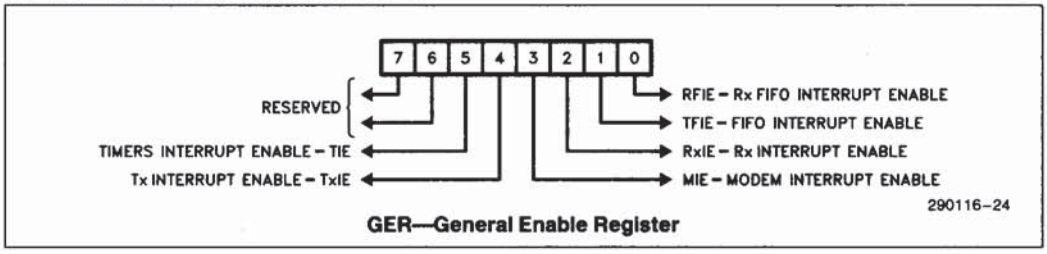
INTERRUPT/STATUS REGISTERS

The 82510 uses a two layer approach to handle interrupt and status generation. Device level registers show the status of the major 82510 functional block (MODEM, FIFO, Tx MACHINE, Rx MACHINE, TIMERS, etc.). Each block may be examined by reading its individual block level registers. Also each block has interrupt enable/generation logic which may generate a request to the built-in interrupt controller, the interrupt requests are then resolved on a priority basis.

Interrupt Masking

The 82510 has a device enable register, GER, which can be used to enable or mask-out any block interrupt request. Some of the blocks (Rx Machine, Modem, Timer) have an enable register associated with their status register which can be used to mask out the individual sources within the block. Interrupts are enabled when programmed high.

16. GER—GENERAL ENABLE REGISTER



GER—General Enable Register

This register enables or disables the bits of the GSR register from being reflected in the GIR register. It serves as the device enable register and is used to mask the interrupt requests from any of the 82510 block (See Figure 1).

TIE—Timers Interrupt Enable

TxIE—Transmit Machine Interrupt Enable.

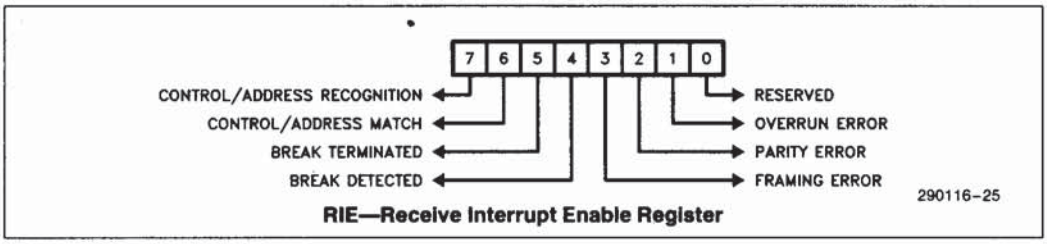
MIE—Modem Interrupt Enable.

RxIE—Rx Machine Interrupt Enable.

TFIE—Transmit FIFO Interrupt Enable.

RFIE—Receive FIFO Interrupt Enable.

17. RIE—RECEIVE INTERRUPT ENABLE REGISTER



RIE—Receive Interrupt Enable Register

This register enables interrupts from the Rx Machine. It is used to mask out interrupt requests generated by the status bits of the RST register.

CRE—Control/uLAN Address Character Recognition Interrupt Enable.—Enables Interrupt when CRF bit of RST register is set.

PCRE—Programmable Control/Address Character Match Interrupt Enable.—Enables Interrupt on PCRF bit of RST.

BkTe—Break Termination Interrupt Enable.

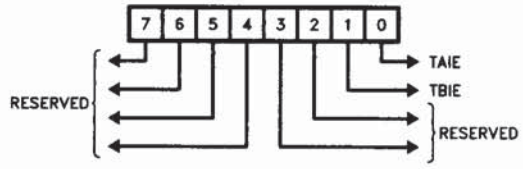
BkDE—Break Detection Interrupt Enable—Enable Interrupt on BkD bit of RST.

FEE—Framing Error Enable—Enable Interrupt on FE bit of RST.

PEE—Parity Error Enable—Enable Interrupt on PE bit of RST.

OEE—Overrun Error Enable—Enable Interrupt on OE bit of RST.

18. TMIE—TIMER INTERRUPT ENABLE REGISTER



TMIE—Timers/Interrupt Enable Register

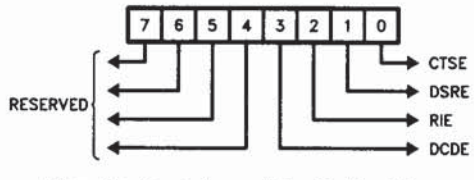
This is the enable register for the Timer Block. It is used to mask out interrupt requests generated by the status bits of the TMST register.

TBIE—Timer B Expired Interrupt Enable—Enables Interrupt on TBEx bit of TMST.

TAIE—Timer A Expired Interrupt Enable—Enables Interrupt on TAEx bit of TMST.

2

19. MIE—MODEM INTERRUPT ENABLE REGISTER



MIE—Modem Interrupt Enable Register

This register enables interrupts from the Modem Block. It is used to mask out interrupt requests generated by the status bits of the MODEM STATUS register.

DCDE—Delta $\overline{\text{DCD}}$ Interrupt Enable—Enables Interrupt on DDCD bit of MODEM STATUS.

RIE—Delta $\overline{\text{RI}}$ Interrupt Enable—Enables Interrupt on DRI bit of MODEM STATUS.

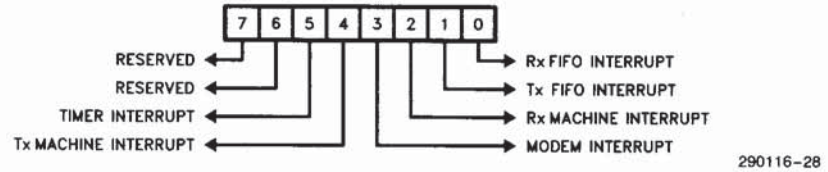
DSRE—Delta $\overline{\text{DSR}}$ Interrupt Enable—Enables Interrupt on $\overline{\text{DSR}}$ bit of MODEM STATUS.

CTSE—Delta $\overline{\text{CTS}}$ Interrupt Enable—Enables Interrupt on DCTS bits of MODEM STATUS.

STATUS/INTERRUPT

The 82510 has two device status registers, which reflect the overall status of the device, and five block status registers. The two device status registers, GSR and GIR, and supplementary in function. GSR reflects the interrupt status of all blocks, whereas GIR depicts the highest priority interrupt only. GIR is updated after the GSR register; the delay is of approximately two clock cycles.

20. GSR—GENERAL STATUS REGISTER



GSR—General Status Register

This register reflects all the pending block-level Interrupt requests. Each bit in GSR reflects the status of a block and may be individually enabled by GER. GER masks-out interrupts from GIR; it does not have any effect on the bits in GSR. The only way that the bits can be masked out in GSR (i.e., not appear in GSR) is if they are masked out at the lower level.

TIR—Timers Interrupt Request—This bit indicates that one of the timers has expired. (See TMST)

TxIR—Transmit Machine Interrupt Request—Indicates that the Transmit Machine is either empty or disabled (Idle).

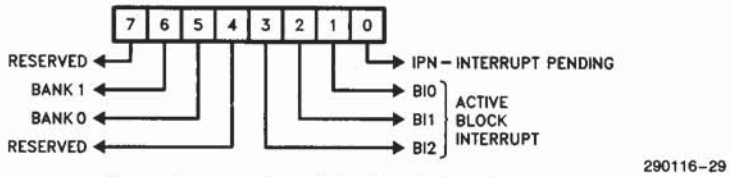
MIR—Modem Interrupt Request—This bit, if set, indicates an interrupt from the Modem Module. (As reflected in MODEM STATUS.)

RxIR—Receive Machine Interrupt Request—(As reflected in RST.)

TFIR—Transmit FIFO Interrupt Request—Tx FIFO occupancy is below or equal to threshold.

RFIR—Receive FIFO Interrupt Request—Rx FIFO Occupancy is above threshold.

21. GIR/BANK—GENERAL INTERRUPT REGISTER/BANK REGISTER



General Interrupt Register/Bank Register

This register holds the highest priority enabled pending interrupt from GSR. In addition it holds a pointer to the current register segment. Writing into this register will update only the BANK bits.

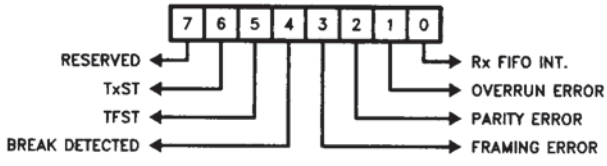
BANK1, BANK0—Bank Pointer Bits—These two bits point to the currently accessible register bank. The user can read and write to these bits. The address of this register is always two within all four register banks.

BI2, BI1, BI0,—Interrupt Bits 0-2—These three bits reflect the highest priority enabled pending interrupt from GSR.

101: Timer Interrupt (highest priority)
100: Tx Machine Interrupt
011: Rx Machine Interrupt
010: Rx FIFO Interrupt
001: Tx FIFO Interrupt
000: Modem Interrupt (lowest priority)

IPN—Interrupt Pending—This bit is active low. It indicates that there is an interrupt pending. The interrupt logic asserts the INT pin as soon as this bit goes active. (Note: the GIR register is continuously updated; so that, while the user is serving one interrupt source, a new interrupt with higher priority may enter GIR and replace the older interrupt.)

22. LSR—LINE STATUS REGISTER



LSR—Line Status Register

This register holds the status of the serial link. It shares five of its bits with the RST register (BkD, FE, PE, OE, and RFIR). When this register is read, the RST register (BITS 1–7) and LSR register (BITS 1–4) are cleared. This register is provided for compatibility with the INS8250A.

TxSt—Transmit Machine Status Bit—Same as TxIR bit of GSR register. If high it indicates that the Transmit Machine is in Idle State. (Note: Idle may indicate that the TxM is either empty or disabled.

TFSt—Transmit FIFO Status—Same as TFIR bit of GSR. It indicates that the Transmit FIFO level is equal to or below the Transmit FIFO Threshold. There are two ways to disable the transmit FIFO status from being reflected in GIR:

1. Writing a "0" to the TFIE bit of the GER register
2. Dynamically by using the Tx FIFO HOLD INTERRUPT logic. When the Tx FIFO is in the Hold State, no interrupts are generated regardless of the TFIR and TFIE bits.

The Transmit FIFO enters the Hold State when the CPU reads the GIR register and the source of the interrupt is Tx FIFO. To Exit, the CPU must drop the TFIR bit of GSR by writing a character to Tx FIFO, or drop TFIE bit of GER (Disable Tx FIFO).

Bkd—Break Detected—See Bkd bit in RST register for full explanation. The BkD bit in RST register is the same as this bit.

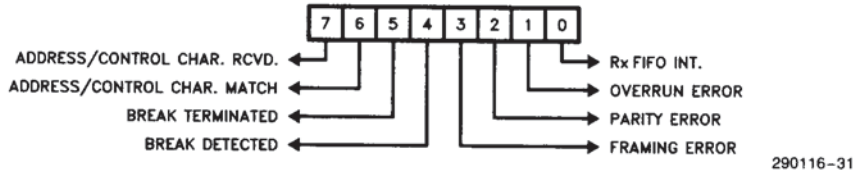
FE—Framing Error Detected—See FE bit in RST register for a full explanation. The FE bit in RST register is the same as this bit.

PE—Parity Error Detected—See PE bit in RST register for full explanation. The PE bit in RST register is the same as this bit.

OE—Overrun Error—See OE bit in RST register for full explanation. The OE bit in RST register is the same as this bit.

RFIR—Receive FIFO Interrupt Request—This bit is identical to RFIR bit of GSR. It indicates that the RX FIFO level is above the Rx FIFO Threshold. This bit is forced LOW during any READ from the Rx FIFO. A zero written to this bit will acknowledge an Rx FIFO interrupt.

23. RST—RECEIVE MACHINE STATUS REGISTER



RST—Receive Machine Status Register

This register displays the status of the Receive Machine. It reports events that have occurred since the RST was cleared. This register is cleared when it is read except for BIT0, Rx FIFO interrupt. Each bit in this register, when set, can cause an interrupt. Five bits of this register are shared with the LSR register.

CRF—Control/Address Character Received—When enabled, this bit can cause an interrupt if a control character or address character is received.

In uLAN Mode: indicates that an address character has been received.
In normal Mode: indicates that a standard control character (either ASCII or EBCDIC) has been received.

PCRF—Programmed Control/Address Character Received—This bit, when enabled, will cause an interrupt when an address or control character match occurs.

In uLAN Mode: indicates that an address character equal to one of the registers ACR0 or ACR1 has been received.
In normal Mode: indicates that a character which matches the registers ACR0 or ACR1 has been received.

BkT—Break Terminated—This bit indicates that a break condition has been terminated.

BkD—Break Detected—This bit indicates that a Break Condition has been detected, i.e., RxD input was held low for one character frame plus a stop BIT.

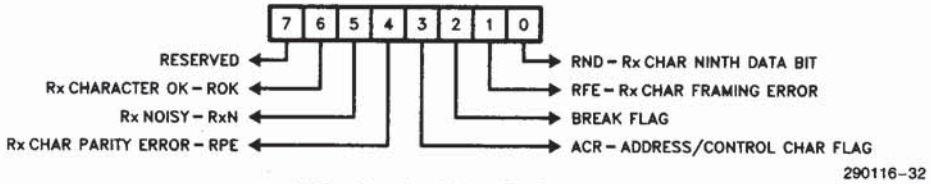
FE—Framing Error—This bit indicates that a received character did not have a valid stop bit.

PE—Parity Error—Indicates that a received character had a parity error.

OE—Overrun Error—Indicates that a received character was lost because the Rx FIFO was full.

RFIR—Receive FIFO Interrupt Request—Same as the RFIR bit of LSR register.

24. RXF—RECEIVED CHARACTER FLAGS



RxF—Receive Flags Register

This register contains additional information about the character in the RXD register. It is loaded by the Rx Machine simultaneously with the RXD register.

ROK—Received Character OK—This bit indicates that the character in RXD no parity or framing error. The parity error is not included in the s/w parity mode.

RxN—Received Character Noisy—The character in RXD was noisy. This bit, valid only in 16X sampling mode, indicates that the received character had non-identical samples for at least one of its bits.

RPE—Receive Character Parity Error—This bit indicates that the RxD character had a Parity Error. However, in S/W Parity mode it holds the received parity bit as is.

ACR—Address/Control Character Marker—This bit indicates that the character in RXD is either:

A control Character—in normal Mode.
An Address Character in uLAN Mode.

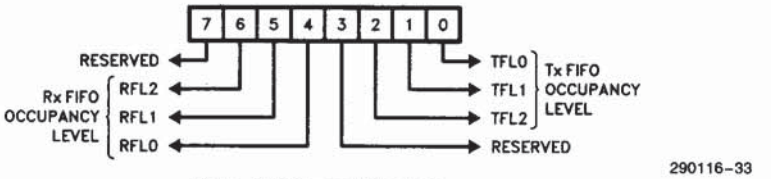
RFE—Receive Character Framing Error—Indicates that no Stop bit was found for the character in RXD.

NOTE:
A Framing Error will be generated for the first character of the Break sequence.

RND—Ninth Bit of Received Character—The most significant bit of the character in RXD is written into this bit. This bit is zero for characters with less than nine bits.

BKF—Break Flag—Indicates that the character is part of a "break" sequence.

25. FLR—FIFO LEVEL REGISTER



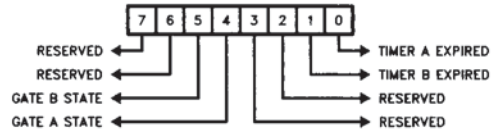
FLR—FIFO Level Register

This register holds the current Receive and Transmit FIFO occupancy levels.

RFL2, RFL1, RFL0—Receive FIFO Level of Occupancy—These three bits indicate the level of Occupancy of the Rx FIFO. The valid range is zero (000) to four (100).

TFL2, TFL1, TFL0—Transmit FIFO Level of Occupancy—These three bits indicate the level of occupancy in the transmit FIFO. The valid range is zero (000) to four (100).

26. TMST—TIMER STATUS REGISTER



TMST—Timer Status Register

This register holds the status of the timers. Bits TBEx and TAEx generate interrupts which are reflected in bit TIR of GSR. Bits GBS and GAS just display the counting status, they do not generate interrupts.

GBS—Gate B State—This bit does not generate an interrupt. It indicates the counting state of the software gate of Timer B, as written through the TMCR register.

0—counting disabled
1—counting enabled

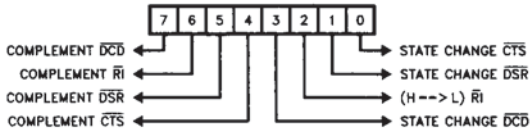
GAS—Gate—A State—This bit does not generate an interrupt. It reflects the state of the software gate of Timer A, as written through the TMCR register.

0—counting disabled
1—counting enabled

TBEx—Timer B Expired—When Set generates an interrupt through TIR bit of GSR. Indicates that Timer B count has expired. This bit is set via the terminal count pulse generated by the timer when it terminates counting.

TAEx—Timer A Expired—Same as TBEx except it refers to Timer A.

27. MSR—MODEM/I/O PINS REGISTER



MSR—Modem/I/O Pins Status Register

This register holds the status of the Modem input pins (CTS, DCD, DSR, RI). It is the source of interrupts (MSR 0–3) for the MIR bit of GSR. If any of the above inputs change levels the appropriate bit in MODEM STATUS is set. Reading MODEM STATUS will clear the status bits.

DCDC—$\overline{\text{DCD}}$ Complement—Holds the complement of the $\overline{\text{DCD}}$ input pin if programmed as an input in PMD.

DRIC—Holds the complement of the $\overline{\text{RI}}$ input pin if programmed as an input in PMD.

DSRC—$\overline{\text{DSR}}$ Complement—Holds the complement of the $\overline{\text{DSR}}$ input pin if configured as an input in PMD.

CTSC—$\overline{\text{CTS}}$ Complement—Holds the complement of the $\overline{\text{CTS}}$ pin.

DDCD—Delta $\overline{\text{DCD}}$—Indicates that the $\overline{\text{DCD}}$ input pin has changed state since this register was last read.

DRI—Delta $\overline{\text{RI}}$—Indicates that there was a high-to-low transition on the $\overline{\text{RI}}$ input pin since the register was last read.

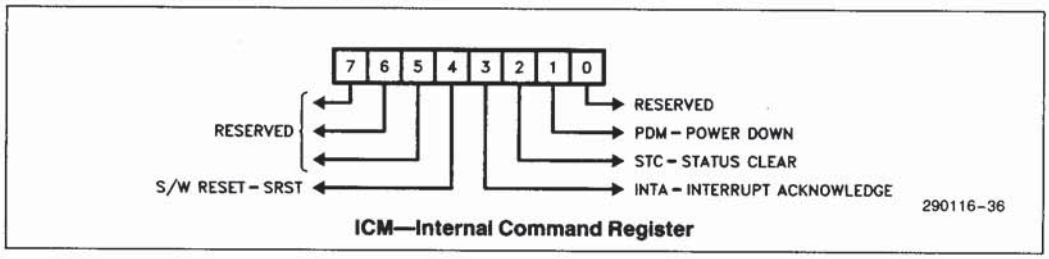
DDSR—Delta $\overline{\text{DSR}}$—Indicates that the $\overline{\text{DSR}}$ input pin has changed state since this register was last read.

DCTS—Delta $\overline{\text{CTS}}$—Indicates that the $\overline{\text{CTS}}$ input pin has changed state since this register was last read.

COMMAND REGISTERS

The command registers are write only; they are used to trigger an operation by the device. Once the operation is started the register is automatically reset. There is a device level register as well as four block command registers. It is recommended that only one command be issued during a write cycle.

28. ICM—INTERNAL COMMAND REGISTER



ICM—Internal Command Register

This register activates the device's general functions.

SRST—Device Software RESET—Causes a total device reset; the effect is identical to the hardware reset (except for strapping options). The reset lasts four clocks and puts the device into the Default Wake-up Mode.

INTA—Interrupt Acknowledge—This command is an explicit acknowledgement of the 82510's interrupt request. It forces the INT pin inactive for two clocks; afterwards, the INT pin may again go active if other enabled interrupts are pending. This command is provided for the Manual Acknowledge mode of the 82510.

StC—Status Clear—Clears the following status registers: RST, MSR, and TMST.

PDM—Power Down—This command forces the device into the power-down mode. Refer to the functional description for details.

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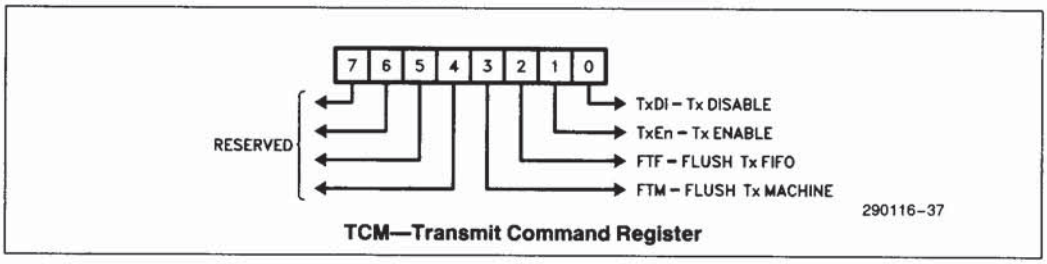
29. TCM—TRANSMIT COMMAND REGISTER



TCM—Transmit Command Register

This register controls the operation of the Transmit Machine.

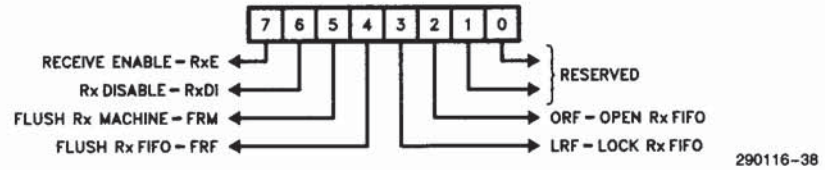
FTM—Flush Transmit Machine—Resets the Transmit Machine logic (but not the registers or FIFO) and enables transmission.

FTF—Flush Transmit FIFO—Clears the Tx FIFO.

TxEN—Transmit Enable—Enables Transmission by the Transmit Machine.

TxDi—Transmit Disable—Disables transmission. If transmission is occurring when this command is issued the Tx Machine will complete transmission of the current character before disabling transmission.

30. RCM—RECEIVE COMMAND REGISTER



RCM—Receive Command Register

This register controls the operation of the Rx machine.

RxE—Receive Enable—Enables the reception of characters.

RxDI—Receive Disable—Disables reception of data on RXD pin.

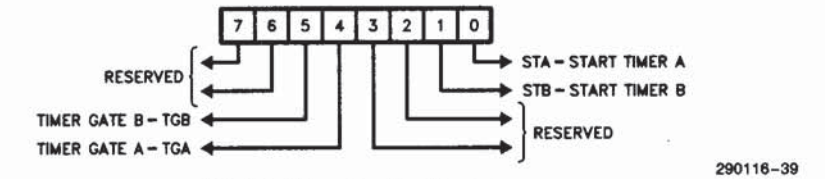
FRM—Flush Receive Machine—Resets the Rx Machine logic (but not registers and FIFOs), enables reception, and unlocks the receive FIFO.

FRF—Flush Receive FIFO—Clears the Rx FIFO.

LRF—Locks Rx FIFO—Disables the write mechanism of the Rx FIFO so that characters subsequently received are not written to the Rx FIFO but are lost. However, reception is not disabled and complete status/event reporting continues. (This command may be used in the uLAN mode to disable loading of characters into the Rx FIFO until an address match is detected.)

ORF—Open (Unlock) Rx FIFO—This command enables or unlocks the write mechanism of the Rx FIFO.

31. TMCR—TIMER CONTROL REGISTER



TMCR—Timer Control Register

This register controls the operation of the two 82510 timers. It has no effect when the timers are configured as baud—rate generators. TGA and TGB are not reset after command execution.

TGB—Timer-B Gate—This bit serves as a gate for Timer B operation:

1—enables counting
0—disables counting

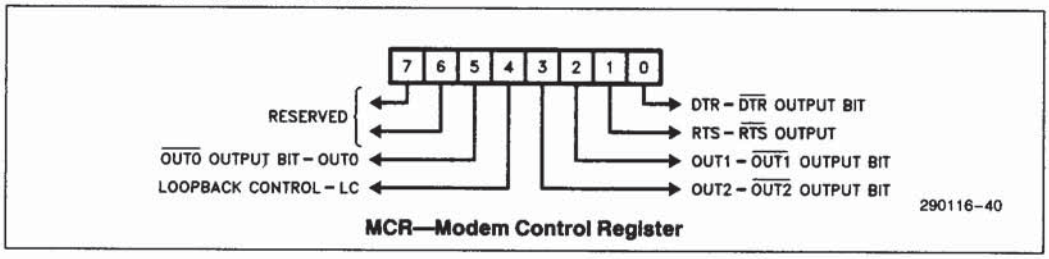
TGA—Timer-A Gate—This bit serves as a gate for Timer-A operation:

1—enables counting
0—disables counting

STB—Start Timer B—This command triggers timer B. At terminal count a status bit is set in TMST (TBEx).

STA—Start Timer A—This command triggers timer A. At terminal count a status bit is set in TMST (TAEx).

32. MCR—MODEM CONTROL REGISTER



MCR—Modem Control Register

This register controls the modem output pins. With multi—function pins it affects only the pins configured as general purpose output pins. All the output pins invert the data, i.e. their output will be the complement of the data written into this register.

OUT0—$\overline{OUT0}$ Output Bit—This bit controls the $\overline{OUT0}$ pin. The output signal is the complement of this bit.

LCB Loopback Control Bit—This bit puts the 82510 into loopback mode. The particular type of loopback is selected via the IMD register.

OUT2—$\overline{OUT2}$ Output Bit—This bit controls the $\overline{OUT2}$ pin. The output signal is the complement of this bit.

OUT1—$\overline{OUT1}$ Output Bit—This bit controls the $\overline{OUT1}$ pin. The output signal is the complement of this bit.

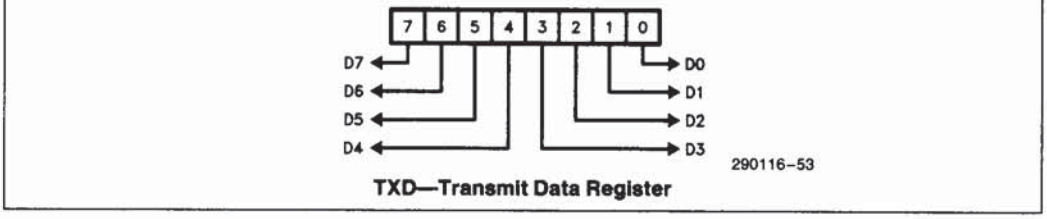
RTS—$\overline{RTS}$ Output Bit—This bit controls the $\overline{RTS}$ pin. The output signal is the complement of this bit.

DTR—$\overline{DTR}$ Output Bit—This bit controls the $\overline{DTR}$ pin. The output signal is the complement of this bit.

DATA REGISTERS

The data registers hold data or other information and may be accessed at any time.

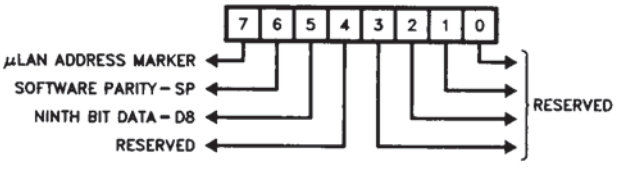
33. TXD—TRANSMIT DATA REGISTER



TXD—Transmit Data Register

This register holds the next data byte to be pushed into the Transmit FIFO. For character formats with more than eight bits of data, or with additional components (S/W Parity, Address Marker Bit) the additional data bits should be written into the TxF register. When a byte is written to this register its contents, along with the contents of the TxF register, are pushed to the top of the Transmit FIFO. This register is write only.

34. TXF—TRANSMIT FLAGS REGISTER



TxF—Transmit Flags Register

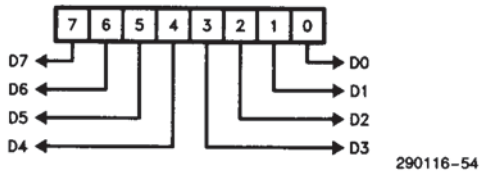
This register holds some additional components of the next character to be pushed into the Tx FIFO. The contents of this register are pushed into the Tx FIFO with the Transmit Data register whenever the TxD register is written to by the CPU.

uLAN—uLAN Address Marker Bit—This bit is transmitted in uLAN mode as the address marker bit.

SP—Software Parity Bit—This bit is transmitted in S/W parity mode as the character's parity bit.

D8—Ninth Bit of Data—In nine-bit character length mode this bit is transmitted as the MSB (D8) bit.

35. RXD—RECEIVE DATA REGISTER



RXD—Receive Data Register

This register holds the earliest received character in the Rx FIFO. The character is right justified and leading bits are zeroed. This register is loaded by the Rx Machine with the first received character. Reading the register causes the next register from the Rx FIFO to be loaded into RxD and RxF registers.

SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Ambient Temperature under Bias .....0°C to 70°C
Storage Temperature .....−65° to +150°C
Voltage on any Pin (w.r.t. V_{SS}) −0.5V to V_{CC} +0.5V
Voltage on V_{CC} Pin (w.r.t. V_{SS}).....−0.5V to +7V
Power Dissipation .....300 mW

D.C. SPECIFICATIONS

D.C. CHARACTERISTICS (T_A = 0° to 70°C, V_{CC} = 5V ±10%)

Symbol	Parameter	Notes	Min	Max	Units
V_{IL}	Input Low Voltage	(1)	−0.5	0.8	V
V_{IH}	Input High Voltage	(1)	2.0	V_{CC}−0.5	V
V_{OL}	Output Low Voltage	(2), (9)		0.45	V
V_{OH}	Output High Voltage	(3), (9)	2.4		V
I_{LI}	Input Leakage Current	(4)		±10	μA
I_{LO}	3-State Leakage Current	(5)		±10	μA
I_{cc}	Power Supply Current	(6)		3.8	mA/MHz
I_{pd}	Power Down Supply	(7)		2	mA
I_{STBY}	Standby Supply Current	(10)		500	μA
I_{OHR}	$\overline{RTS}$, $\overline{DTR}$ Strapping Current	(11)		0.4	mA
I_{OLR}	$\overline{RTS}$, $\overline{DTR}$ Strapping Current	(12)	11		mA
C_{in}	Input Capacitance	(8)		10	pF
C_{io}	I/O Capacitance	(8)		10	pF
C_{XTAL}	X1, X2 Load			10	pF

NOTES:
1. Does not apply to CLK/X1 pin, when configured as crystal oscillator input (X1).
2. @ I_{OL} = 2 mA.
3. @ I_{OH} = −0.4 mA.
4. $0 < V_{IN} < V_{CC}$.
5. $0.45V < V_{OUT} < (V_{CC} - 0.45)$.
6. V_{CC} = 5.5V; V_{IL} = 0.5V (max); V_{IH} = V_{CC} − 0.5V (min); 35 mA (max); Typical value = 2.5 mA/MHz (Not Tested); Ext 1X CLK (9 MHz max); I_{OL} = I_{OH} = 0.
7. V_{CC} = 5.5V; V_{IL} = GND; V_{IH} = V_{CC}; I_{OL} = I_{OH} = 0; device at power down mode, clock running.
8. Freq = 1 MHz.
9. Does not apply to OUT2/X2 pin, when configured as crystal oscillator output (X2).
10. Same as 7, but input clock not running.
11. Applies only during hardware reset for clock configuration options. Strapping current for logic HIGH.
12. Applies only during hardware reset for clock configuration. Strapping current for logic LOW.

A.C. SPECIFICATIONS

Testing Conditions:

- All AC output parameters are under output load of 20 to 100 pF, unless otherwise specified.
- AC testing inputs are driven at 2.4 for logic '1', and 0.45V for logic '0'. Output timing measurements are made at 1.5V for both a logical '0' and '1'.
- In the following tables, the units are ns, unless otherwise specified.

System Interface Specification—System Clock Specification:

The 82510 system clock is supplied via the CLK pin or generated by an on-chip crystal oscillator. The clock is optionally divided by two. The CLK parameters are given separately for internal divide-by-two option ACTIVE and INACTIVE.

The system clock (after division by two, if active) must be at least 16X the Tx or Rx baud rate (the faster of the two).

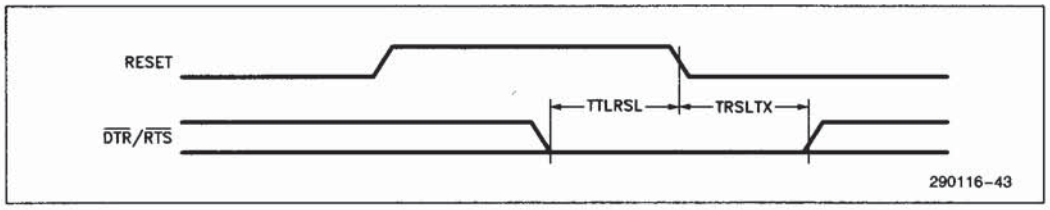
SYSTEM CLOCK SPECIFICATIONS

Symbol	Parameter	Min	Max	Notes
DIVIDE BY TWO OPTION—ACTIVE				
Tcy/2	CLK Period	54	250	(2)
TCLCH	CLK Low Time	25		
TCHCL	CLK High Time	25		
TCH1CH2	CLK Rise Time		10	(1)
TCL2CL1	CLK Fall Time		10	(1)
FXTAL	External Crystal Frequency Rating	4.0	18.432 MHz	
DIVIDE BY TWO OPTION—INACTIVE				
Tcy	CLK Period	108		
TCLCH	CLK Low Tme	54		
TCHCL	CLK High Time	44	250	
TCH1CH2	CLK Rise Time		15	(1)
TCL2CL1	CLK Fall Time		15	(1)

NOTES:
1. Rise/fall times are measured between 0.8 and 2.0V.
2. Tcy in ACTIVE divide by two option is TWICE the input clock period.

RESET SPECIFICATION

Symbol	Parameter	Min	Max	Notes
TRSHL	Reset Width—CLK/X1 Configured to CLK	8 Tcy		(1)
TTLRSL	RTS/DTR LOW Setup to Reset Inactive	6 Tcy		(2)
TRSLTX	RTS/DTR Low Hold after Reset Inactive	0	Tcy − 20	(2)

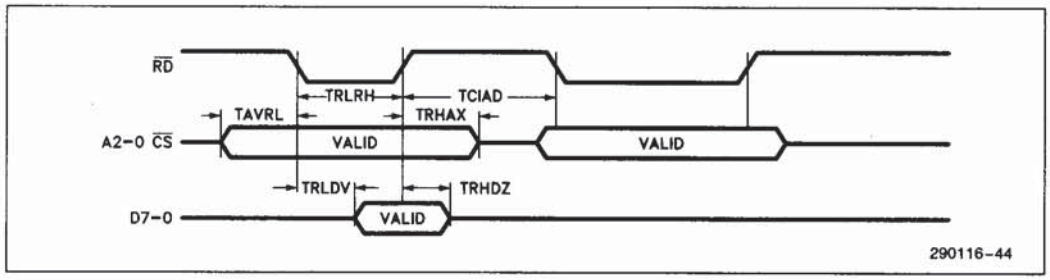


NOTES:
1. In case of CLK/X1 configured as X1, 1 Ms is required to guarantee crystal oscillator wake-up.
2. RTS/DTR are internally driven HIGH during RESET active time. The pin should be either left OPEN or externally driven LOW during RESET according to the required configuration of the system clock. These parameters specify the timing requirements on these pins, in case they are externally driven LOW during RESET.
The maximum spec on TRSLTX requires that the RTS/DTR pins not be forced later than TRSLTX maximum.

READ CYCLE SPECIFICATIONS

Symbol	Parameter	Min	Max	Notes
TRLRH	$\overline{RD}$ Active Width	2 Tcy + 65		
TAVRL	Address/$\overline{CS}$ Setup Time to $\overline{RD}$ Active	7		
TRHAX	Address/$\overline{CS}$ Hold Time after $\overline{RD}$ Inactive	0		
TRLDV	Data Out Valid Delay after $\overline{RD}$ Active		2Tcy + 65	
TCIAD	Command Inactive to Active Delay	Tcy + 15		(1)
TRHDZ	Data Out Float Delay after $\overline{RD}$ Inactive		40	

NOTE:
1. Command refers to either Read or Write signals.



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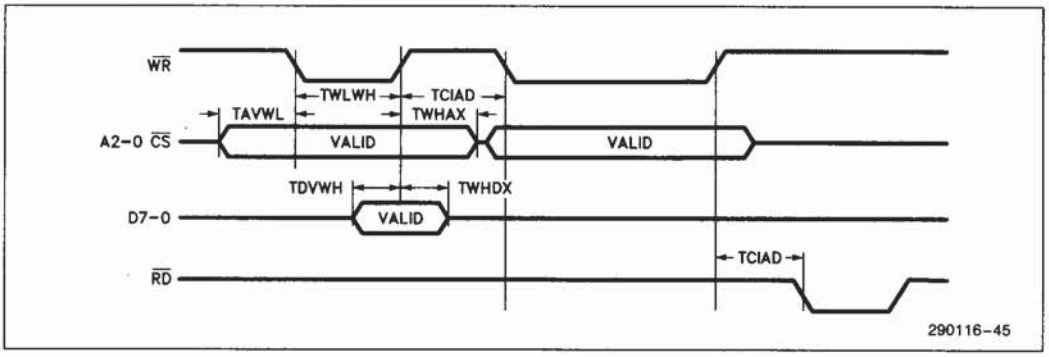
WRITE CYCLE SPECIFICATION

Symbol	Parameter	Min	Max	Notes
TWLWH	$\overline{WR}$ Active Width	2Tcy + 15		
TAVWL	Address $\overline{CS}$ Setup Time to $\overline{WR}$ Active	7		
TWHAX	Address and $\overline{CS}$ Hold Time after $\overline{WR}$	0		
TDVWH	Data in Setup Time to $\overline{WR}$ Inactive	90		
TWHDX	Data in Hold Time after $\overline{WR}$ Inactive	12		



NOTE:
Many of the serial interface pins have more than one function; sometimes the different functions have different timings. In such a case, the timing of each function of a pin is given separately.

SCLK PIN SPECIFICATION—16x CLOCKING MODE

Symbol	Parameter	Min	Max	Notes
Txcy	SCLK Period	216		
TXLXH	SCLK Low Time	93		
TXHXL	SCLK High Time	93		
TXH1XH2	SCLK Rise Time		15	(1)
TXL2XL1	SCLK Fall Time		15	(1)

NOTE:
1. Rise/fall times are measured between 0.8V and 2.0V.

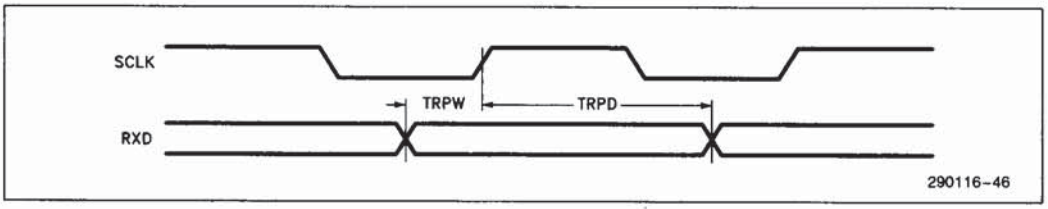
SCLK PIN SPECIFICATION—1x CLOCK MODE

Symbol	Parameter	Min	Max	Notes
Txcy	SCLK Period	3500		
TXLXH	SCLK Low Time	1650		
TXHXL	SCLK High Time	1650		
TXH1XH2	SCLK Rise Time		15	(1)
TXL2XL1	SCLK Fall Time		15	(1)

NOTE:
1. Rise/fall times are measured between 0.8V and 2.0V.

RXD SPECIFICATION (1x MODE)

Symbol	Parameter	Min	Max	Notes
TRPW	RXD Setup Time to SCLK High	250		
TRPD	RXD Hold Time After SCLK High	250		

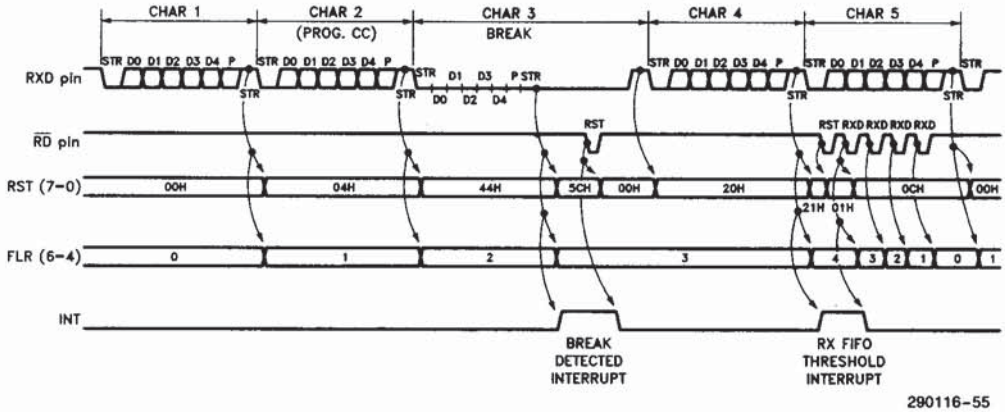


TXD SPECIFICATION (1x MODE)

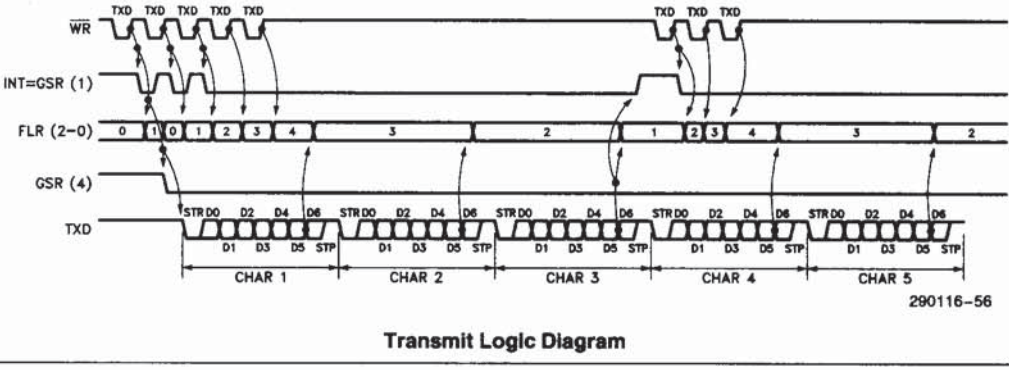
Symbol	Parameter	Min	Max	Notes
TSCLKTXD	TXD Valid Delay after SCLK Low	—	170	

REMOTE LOOPBACK SPECIFICATION

Symbol	Parameter	Min	Max	Notes
TRXDTXD	TXD Delay after RXD	—	170	



Receive Logic Diagram



Transmit Logic Diagram

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