CY7C194BN

256 Kb (64K x 4) Static RAM

Features

- **Fast access time: 15 ns and 25 ns**
- **Wide voltage range: 5.0V ± 10% (4.5V to 5.5V)**
- **CMOS for optimum speed/power**
- **TTL-compatible inputs and outputs**
- **CY7C194BN is available in 24 DIP, 24 SOJ packages.**

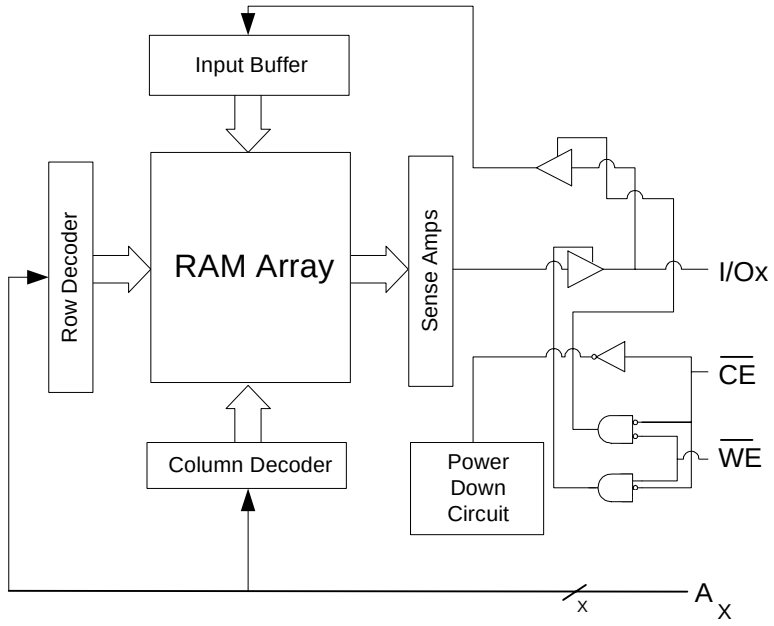
General Description [1]

The CY7C194BN is a high-performance CMOS Asynchronous SRAM organized as 64K × 4 bits that supports an asynchronous memory interface. The device features an automatic power-down feature that significantly reduces power consumption when deselected.

See the Truth Table in this data sheet for a complete description of read and write modes.

The CY7C194BN is available in 24 DIP, 24 SOJ package(s).

Logic Block Diagram



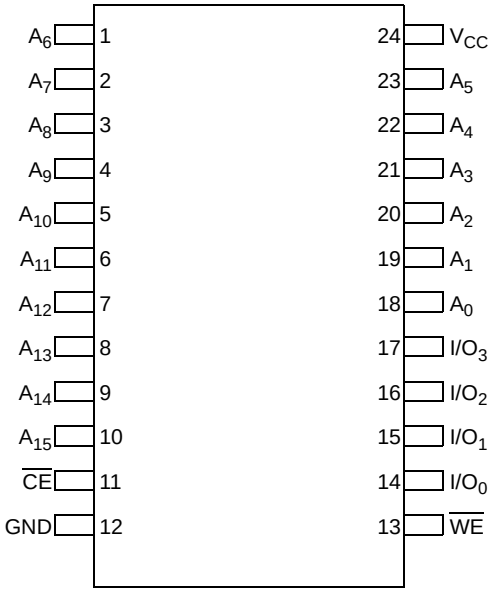
Product Portfolio

	-15	-25	Unit
Maximum Access Time	15	25	ns
Maximum Operating Current	80	80	mA
Maximum CMOS Standby Current	10	10	mA

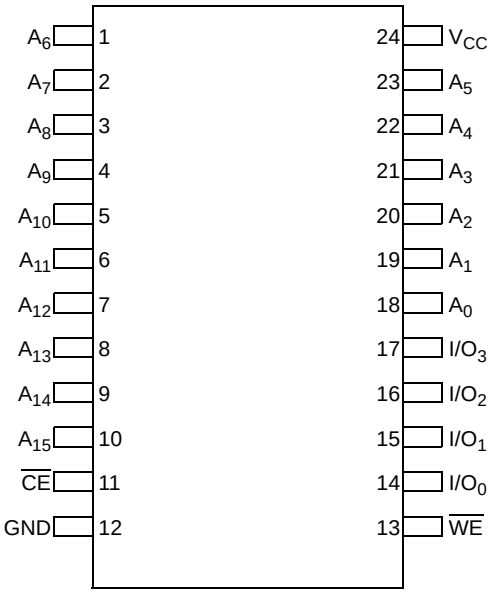
Notes:
1. For best-practice recommendations, please refer to the Cypress application note *System Design Guidelines* on www.cypress.com.

Pin Layout and Specification

CY7C194BN 24 SOJ (8 × 15 × 3.5 mm)



CY7C194BN 24 DIP (6.6 × 31.8 × 3.5 mm)



Pin Description

Pin	Type	Description	CY7C194BN	
			24 DIP	24 SOJ
A_X	Input	**Address Inputs**.	1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 18, 19, 20, 21, 22, 23	1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 18, 19, 20, 21, 22, 23
$\overline{CE}$	Control	**Chip Enable**.	11	11
I/O_X	Input or Output	**Data Input/Outputs**.	14, 15, 16, 17	14, 15, 16, 17
NC	–	**No Connect**. Pins are not internally connected to the die.	–	–
V_{CC}	Supply	**Power (5.0V)**.	24	24
$\overline{WE}$	Control	**Write Enable**.	13	13

CY7C194BN Truth Table

$\overline{CE}$	$\overline{WE}$	I/Ox	Mode	Power
H	X	High Z	Power-Down	Standby (I_{SB})
L	H	Data Out	Read	Active (I_{CC})
L	L	Data In	Write	Active (I_{CC})

Maximum Ratings (Above which the useful life may be impaired. For user guidelines, not tested.)

Parameter	Description	Value	Unit
T_{STG}	Storage Temperature	–65 to +150	°C
T_{AMB}	Ambient Temperature with Power Applied (i.e. case temperature)	–55 to +125	°C
V_{CC}	Core Supply Voltage Relative to V_{SS}	–0.5 to +7.0	V
V_{IN}, V_{OUT}	DC Voltage Applied to any Pin Relative to V_{SS}	–0.5 to V_{CC} + 0.5	V
I_{OUT}	Output Short-Circuit Current	20	mA
V_{ESD}	Static Discharge Voltage (per MIL-STD-883, Method 3015)	> 2001	V
I_{LU}	Latch-up Current	> 200	mA

Operating Range

Range	Ambient Temperature (T_A)	Voltage Range (V_{CC})
Commercial	0°C to 70°C	5.0V ± 10%

DC Electrical Characteristics[3]

Parameter	Description	Condition	15 ns		25 ns		Unit
			Min.	Max.	Min.	Max.	
V_{IH}	Input HIGH Voltage		2.2	V_{CC} + 0.3	2.2	V_{CC} + 0.3	V
V_{IL}	Input LOW Voltage		–0.3	0.8	–0.5	0.8	V
V_{OH}	Output HIGH Voltage	V_{CC} = Min., Ioh = –4.0 ma	2.4	–	2.4	–	V
V_{OL}	Output LOW Voltage	V_{CC} = Min., Iol = 8.0 ma	–	0.4	–	0.4	V
I_{CC}	V_{CC} Operating Supply Current	V_{CC} = Max., I_{OUT} = 0 mA, f = F_{MAX} = 1 / t_{RC}	–	80	–	80	mA
I_{SB1}	Automatic $\overline{CE}$ Power-down Current TTL Inputs	V_{CC} = Max., $\overline{CE} \geq V_{IH}$, $V_{IN} \geq V_{IH}$ or $V_{IN} \leq V_{IL}$, f = F_{MAX}	–	30	–	30	mA
I_{SB2}	Automatic $\overline{CE}$ Power-down Current CMOS Inputs	V_{CC} = Max., $\overline{CE} \geq V_{CC}$ - 0.3v, $V_{IN} > V_{CC}$ - 0.3v or $V_{IN} \leq 0.3$, f = 0, Commercial	–	10	–	10	mA
I_{OZ}	Output Leakage Current	GND ≤ Vi ≤ V_{CC}, Output Disabled	–5	+5	–5	+5	µA
I_{IX}	Input Load Current	GND ≤ Vi ≤ V_{CC}	–5	+5	–5	+5	µA

Capacitance[2]

Parameter	Description	Conditions	Max	Unit
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 5.0V	7	pF
C_{OUT}	Output Capacitance		10	

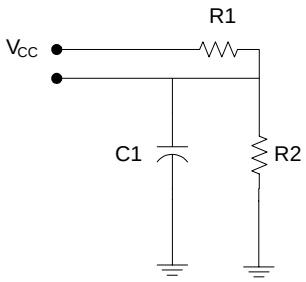
Thermal Resistance[4]

Parameter	Description	Conditions	CY7C194BN		Unit
			24 DIP	24 SOJ	
Θ_{JA}	Thermal Resistance (Junction to Ambient)	Still Air, soldered on a 3 x 4.5 square inches, two-layer printed circuit board	75.69	84.15	°C/W
Θ_{JC}	Thermal Resistance (Junction to Case)		33.80	37.56	

Note:
2. Tested initially and after any design or process change that may affect these parameters
3. V_{IL}(min) = –2.0V for pulse durations of less than 20 ns.
4. Test Conditions assume a transition time of 3ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V

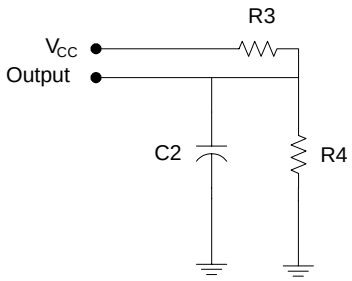
AC Test Loads

Output Loads



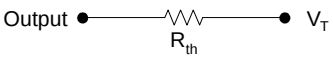
(A)*

Output Loads for t_{HZCE} & t_{HZWE}

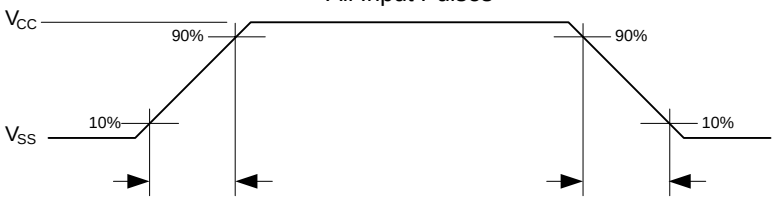


(B)*

Thevenin Equivalent



All Input Pulses



* including scope and jig capacitance

AC Test Conditions

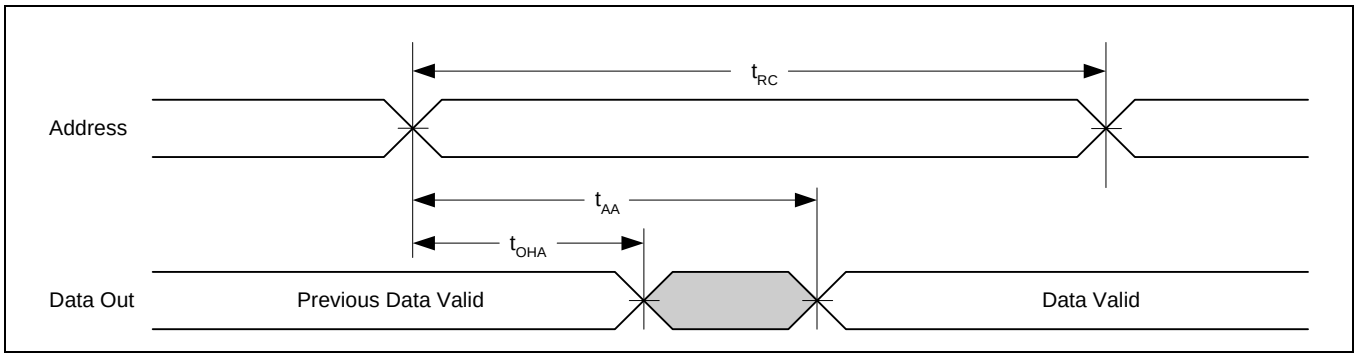
Parameter	Description	Nom.	Unit
C1	Capacitor 1	30	pF
C2	Capacitor 2	5	
R1	Resistor 1	480	Ω
R2	Resistor 2	255	
R3	Resistor 3	480	
R4	Resistor 4	255	
R_{TH}	Resistor Thevenin	167	
V_{TH}	Voltage Thevenin	1.73	V

AC Electrical Characteristics[2, 5, 6, 7]

Parameter	Description	15 ns		25 ns		Unit
		Min	Max	Min	Max	
t_{RC}	Read Cycle Time	15	–	25	–	ns
t_{AA}	Address to Data Valid	–	15	–	25	ns
t_{OHA}	Data Hold from Address Change	3	–	3	–	ns
t_{ACE}	$\overline{CE}$ to Data Valid	–	15	–	25	ns
t_{LZCE}	$\overline{CE}$ to Low Z	3	–	3	–	ns
t_{HZCE}	$\overline{CE}$ to High Z	–	7	–	10	ns
t_{PU}	$\overline{CE}$ to Power-up	0	–	0	–	ns
t_{PD}	$\overline{CE}$ to Power-down	–	15	–	25	ns
t_{WC}	Write Cycle Time	15	–	25	–	ns
t_{SCE}	$\overline{CE}$ to Write End	10	–	18	–	ns
t_{AW}	Address Set-up to Write End	10	–	20	–	ns
t_{HA}	Address Hold from Write End	0	–	0	–	ns
t_{SA}	Address Set-up to Write Start	0	–	0	–	ns
t_{PWE}	$\overline{WE}$ Pulse Width	9	–	18	–	ns
t_{SD}	Data Set-Up to Write End	8	–	10	–	ns
t_{HD}	Data Hold from Write End	0	–	0	–	ns
t_{HZWE}	$\overline{WE}$ LOW to High Z	–	7	-	10	ns
t_{LZWE}	$\overline{WE}$ HIGH to Low Z	3	–	3	–	ns

Timing Waveforms

Read Cycle No. 1[8, 9]

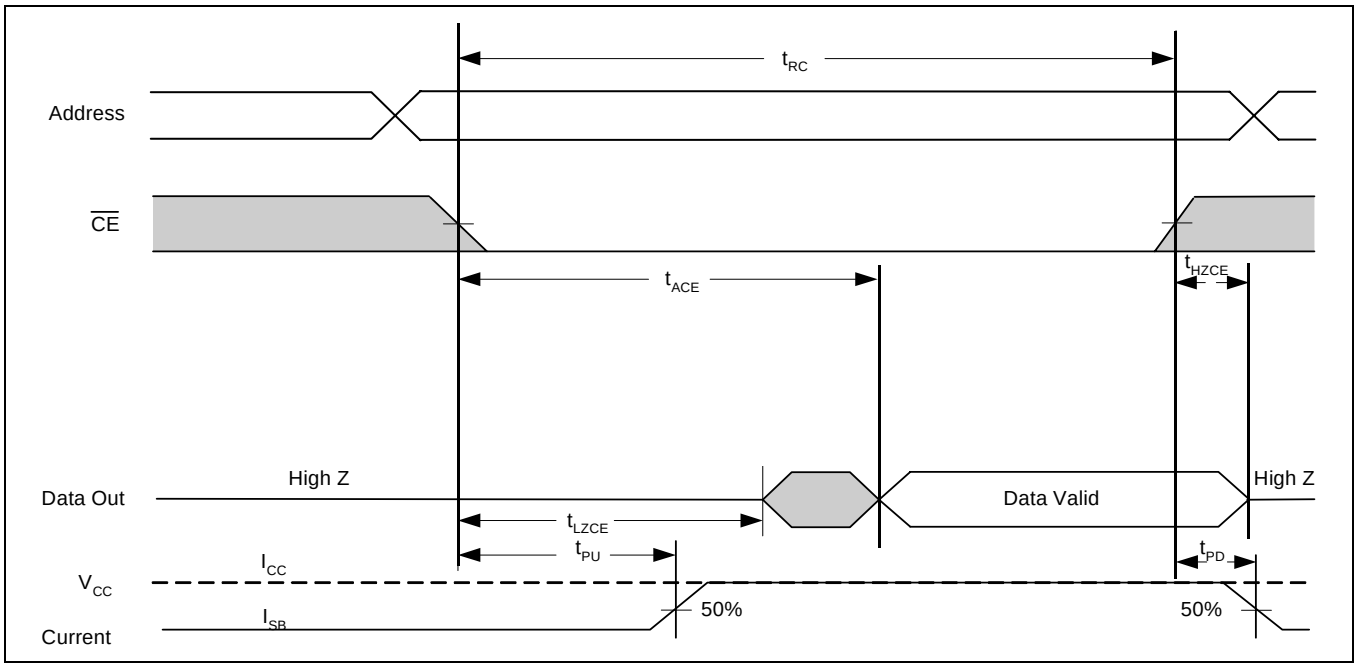


Notes:

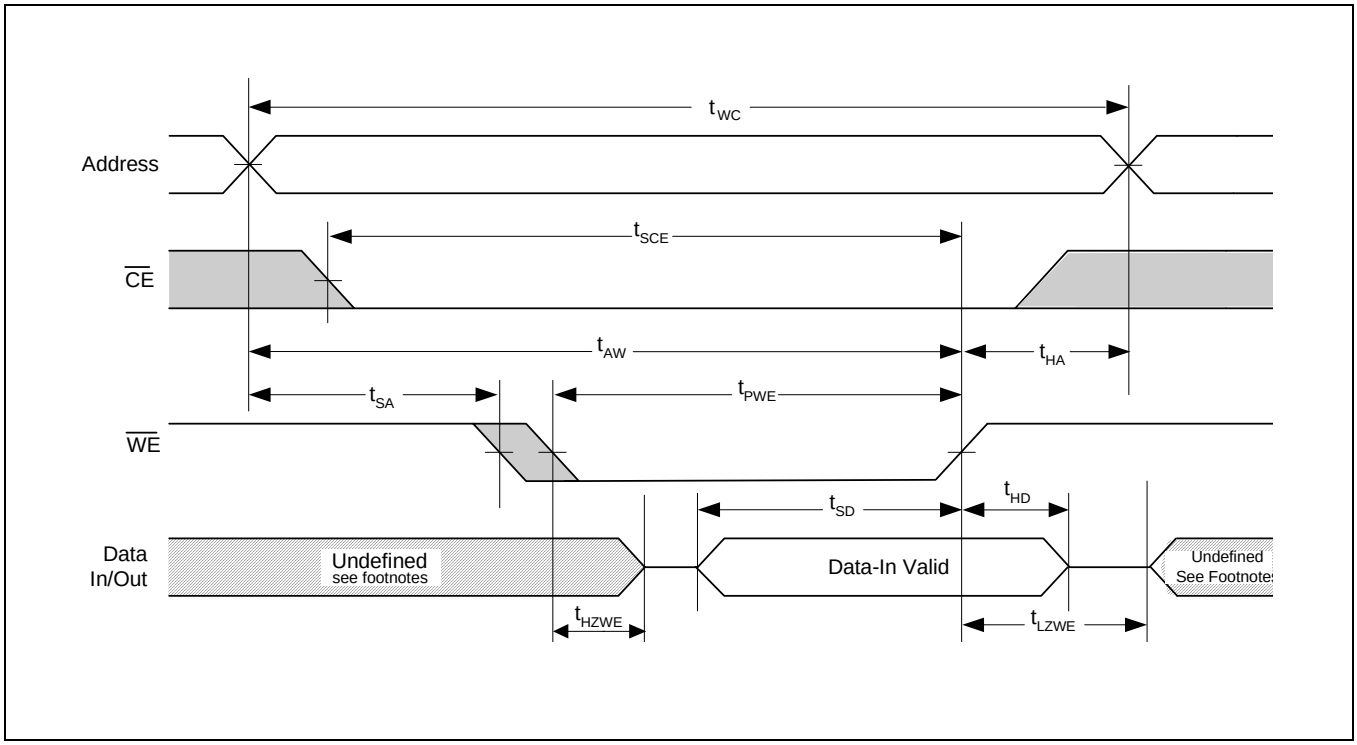
5. At any given temperature and voltage condition, t_{HZCE} is less than t_{LZCE}, and t_{HZWE} is less than t_{LZWE} for any given device.
6. The internal write time of the memory is defined by the overlap of $\overline{CE}$ LOW and $\overline{WE}$ LOW. $\overline{CE}$ and $\overline{WE}$ must be LOW to initiate a write, and the transition of any of these signals can terminate the write. The input data set-up and hold timing should be referenced to the leading edge of the signal that terminates the write.
7. t_{HZCE}, t_{HZWE} are specified as in part (b) of the A/C Test Loads. Transitions are measured ± 200 mV from steady state voltage.
8. Device is continuously selected. $\overline{CE} = V_{IL}$.
9. $\overline{WE}$ is HIGH for Read Cycle.

Timing Waveforms (continued)

Read Cycle No. 2[2, 10, 11]



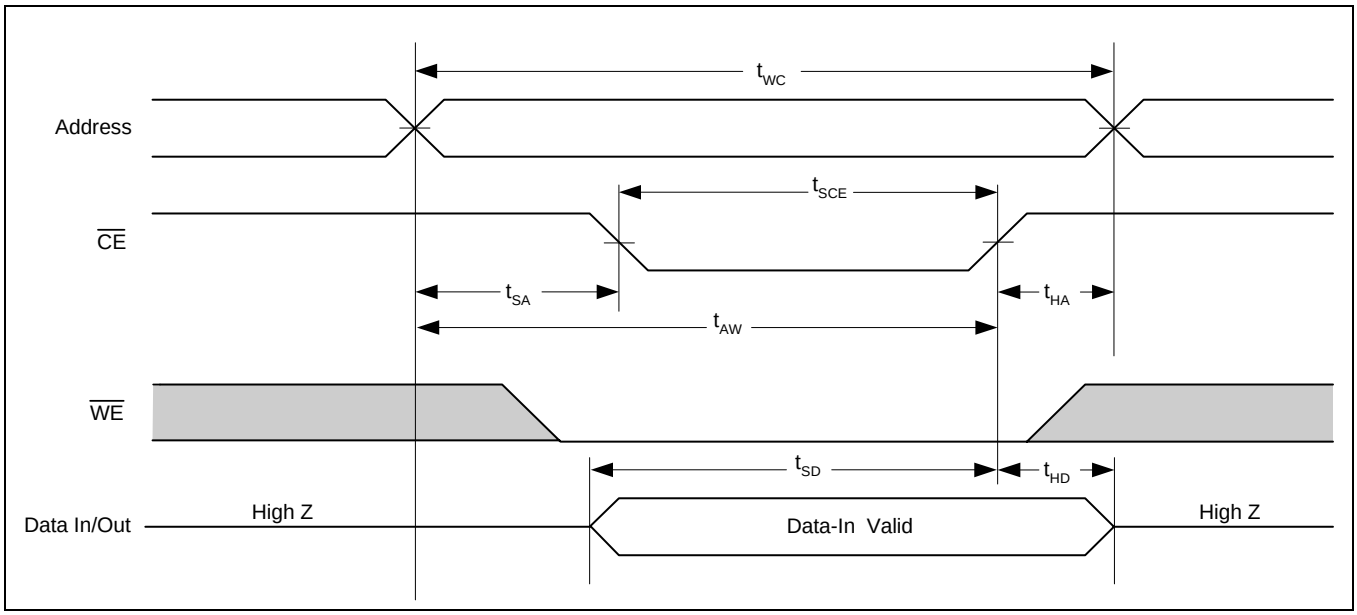
Write Cycle No. 1 (WE Controlled)[2, 12]



Notes:
10. WE is HIGH in read cycle.
11. Address valid prior to or coincident with CE transition LOW.
12. The minimum write cycle time is the sum of t_{HZWE} and t_{SD}.

Timing Waveforms (continued)

Write Cycle No. 2 ($\overline{CE}$ Controlled)[13, 14]



Notes:
13. This cycle is $\overline{CE}$ controlled.
14. If $\overline{CE}$ goes HIGH simultaneously with $\overline{WE}$ going HIGH, the output remains in a high-impedance state.

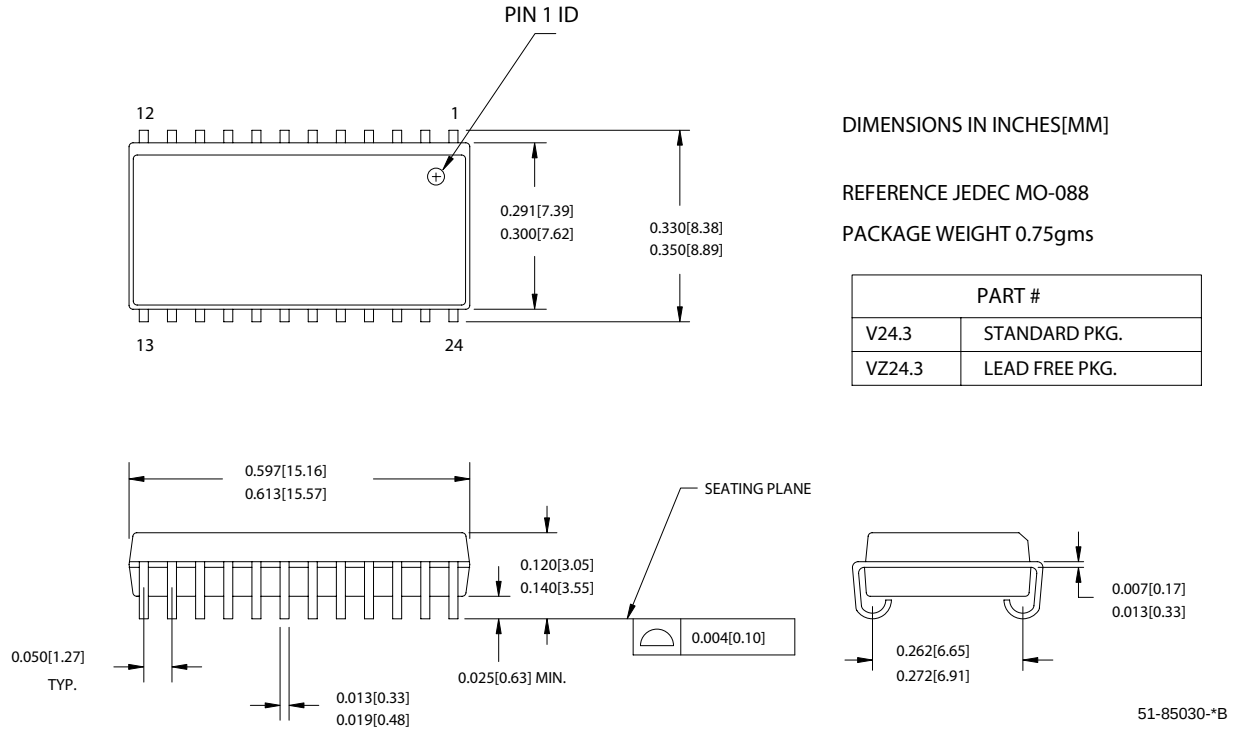
Ordering Information

Speed (ns)	Ordering Code	Package Diagram	Package Type	Power Option	Operating Range
15	CY7C194BN-15PC	51-85013	24 DIP (6.6 x 31.8 x 3.5 mm)	Standard	Commercial
	CY7C194BN-15VC	51-85030	24 SOJ (8 x 15 x 3.5 mm)	Standard	Commercial
25	CY7C194BN-25VC	51-85030	24 SOJ (8 x 15 x 3.5 mm)	Standard	Commercial

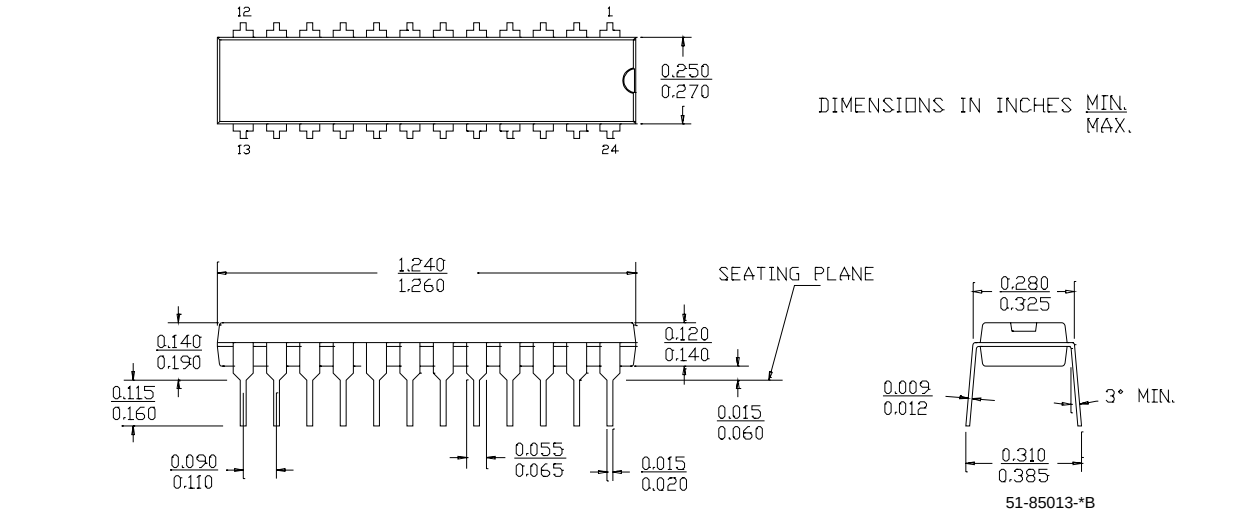
Please contact local sales representative regarding availability of these parts.

Package Diagrams

24-lead (300-mil) SOJ (51-85030)



24 DIP (6.6 x 31.8 x 3.5 mm) (51-85013)



Document History Page

Document Title: CY7C194BN 256 Kb (64K x 4) Static RAM Document Number: 001-06446				
REV.	**ECN No.**	**Issue Date**	**Orig. of Change**	**Description of Change**
**	424111	See ECN	NXR	New Data Sheet