ANALOG DEVICES

LC²MOS Voltage Output 12-Bit MDAC

1.1 Scope.

This specification covers the detail requirements for a monolithic voltage output 12-bit multiplying digital-to-analog converter with a parallel loading structure.

1.2 Part Number.

The complete part number per Table 1 of this specification is as follows:

Device	Part Number[1]
−1	AD7845S(X)/883B
−2	AD7845T(X)/883B

NOTE
[1]To complete the part number substitute the package identifier as shown in paragraph 1.2.3.

1.2.3 Case Outline.

See Appendix 1 of General Specification ADI-M-1000: package outline:

(X)	Package	Description
Q	Q-24	24-Pin Cerdip, 0.3″ Width
E	E-28	28-Contact LCC

1.3 Absolute Maximum Ratings. (T_A=+25°C unless otherwise noted)

V_{DD} to DGND ..... −0.3 V, +17 V
V_{SS} to DGND ..... +0.3 V, −17 V
V_{REF} to AGND ..... ±25 V
V_{RFB} to AGND ..... ±25 V
V_{RA} to AGND ..... ±25 V
V_{RB} to AGND ..... ±25 V
V_{RC} to AGND ..... ±25 V
V_{OUT} to AGND[1] ..... V_{DD} +0.3, V_{SS} −0.3 V
AGND to DGND ..... −0.3 V, V_{DD}
Digital Input Voltage to DGND ..... −0.3 V to V_{DD} +0.3 V
Power Dissipation (Any Package)
Up to +75°C ..... 650 mW
Derates above +75°C ..... 10 mW/°C
Operating Temperature Range ..... −55°C to +125°C

NOTE
[1]V_{OUT} may be shorted to AGND provided that the power dissipation of the package is not exceeded.

1.3.1 Recommended Operating Conditions.

V_{DD} = +15 V ±5%, V_{SS} = −15 V ±5%, V_{REF} = +10 V, AGND = DGND = 0 V, V_{OUT} connected to R_{FB}, V_{OUT} load = 2 kΩ, and 100 pF.

AD7845—SPECIFICATIONS

Table 1.

Test	Symbol	Device	Limits Min	Limits Max	Sub Group	Test Condition[1]	Units
Resolution	RES	−1, 2		12	1, 2, 3		Bits
Relative Accuracy	RA	−1, 2	−1	+1	1	1 LSB = V_{REF} = 2.4 mV	LSB
		−1	−2	+2	2, 3		
		−2	−1	+1	2, 3		
		−2	−0.5	+0.5	4		
Differential Nonlinearity	DNL	−1, 2	−1	+1	1, 2, 3	All Devices Type Are Guaranteed Monotonic over Temperature	LSB
Zero Code Offset Error	Z_E	−1, 2	−2	+2	1		mV
		−1	−5	+5	2, 3		
		−2	−4	+4	2, 3		
		−2	−1	+1	4		
Gain Error	A_E	−1	−6	+6	1, 2, 3	R_{FB}, V_{OUT} Connected	LSB
		−2	−3	+3	1, 2, 3		
		−1	−9	+9	1, 2, 3	R_C, V_{OUT} Connected	
		−2	−6	+6	1, 2, 3	V_{REF} = +5 V	
		−1	−9	+9	1, 2, 3	R_B, V_{OUT} Connected	
		−2	−6	+6	1, 2, 3	V_{REF} = +5 V	
		−1	−10	+10	1, 2, 3	R_A, V_{OUT} Connected	
		−2	−8	+8	1, 2, 3	V_{REF} = 2.5 V	
Reference Input Resistance	R_{REFIN}	−1, 2	8	16	1, 2, 3		kΩ
Application Resistor Matching	$R_{MATCH\ RATIO}$	−1, 2		0.5	1, 2, 3	Matching Between R_A, R_B, R_C	%
Digital Input High Voltage	V_{INH}	−1, 2	2.4		1, 2, 3		V
Digital Input Low Voltage	V_{INL}	−1, 2		0.8	1, 2, 3		V
Digital Input Current	I_{IN}	−1, 2	−1	+1	1, 2, 3	Digital Inputs at 0 V and V_{DD}	μA
Digital Input Capacitance	C_{IN}	−1, 2		7	13[3], 14[3], 15[3]		pF
Power Supply Current	I_{DD}	−1, 2		10	1, 2, 3	V_{OUT} Unloaded	mA
	I_{SS}	−1, 2		4	1, 2, 3		
Power Supply Rejection Gain/ΔV_{DD}	$A/\Delta V_{DD}$	−1, 2	−0.2	+0.2	1, 2, 3	V_{DD} = 15 V ±5%, V_{REF} = −10 V	%/%
Gain/ΔV_{SS}	$A/\Delta V_{SS}$	−1, 2	−0.2	+0.2	1, 2, 3	V_{SS} = −15 V ±5%	%/%
Output Voltage Settling Time	t_{SL}	−1, 2		5	13, 14, 15	To 0.01% of FSR	μs
Open Loop Gain[2]		−1, 2	85		13, 14, 15		dB
Output Voltage Swing		±1, 2	−10	+10	13, 14, 15	R_L = 2 kΩ, C_L = 100 pF	V
Chip Select to Write Setup Time	t_{CS}	−1, 2	100		9	See Timing Diagram	ns
			140		10[3], 11[3]		
Chip Select to Write Hold Time	t_{CH}	−1, 2	0		9, 10, 11		ns
Write Pulse Width	t_{WR}	−1, 2	100		9		ns
			140		10, 11		
Data Setup Time	t_{DS}	−1, 2	100		9		ns
			120		10, 11		
Data Hold Time	t_{DH}	−1, 2	20		9, 10, 11		ns

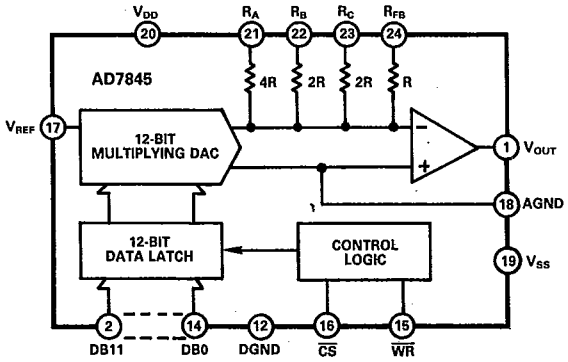
NOTES

[1]−55°C to +125°C.

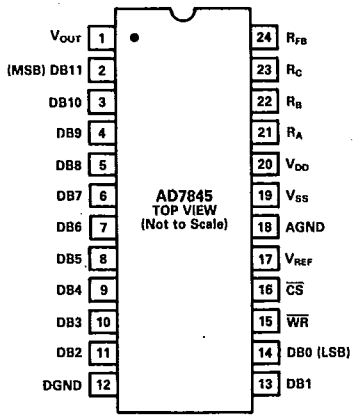
[2]V_{OUT}, R_{RB} not connect. V_{OUT} = ±10 V, R_L = 2 kΩ. Parameters in subgroups 13, 14, 15 are characterized at initial design and after any subsequent redesigns.

[3]Subgroups 10, 11, 13, 14, 15 are characterized at initial design and after subsequent design changes and are not production tested.

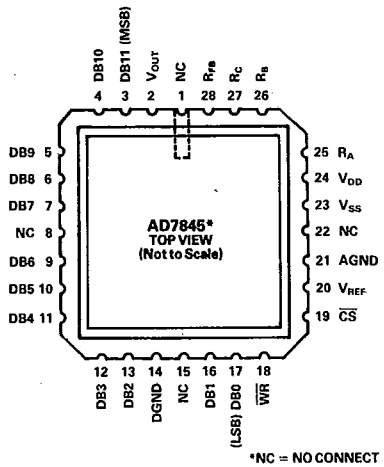
3.2.1 Functional Block Diagram and Terminal Assignments.



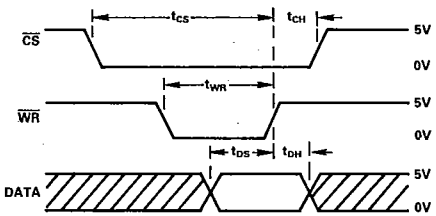
DIP



LCC



*NC = NO CONNECT



NOTES
1. All INPUT SIGNAL RISE AND FALL TIMES MEASURED FROM 10% to 90% of +5V. $t_R = t_F = 20ns$.
2. TIMING MEASUREMENT REFERENCE LEVEL IS $\frac{V_{IH} + V_{IL}}{2}$

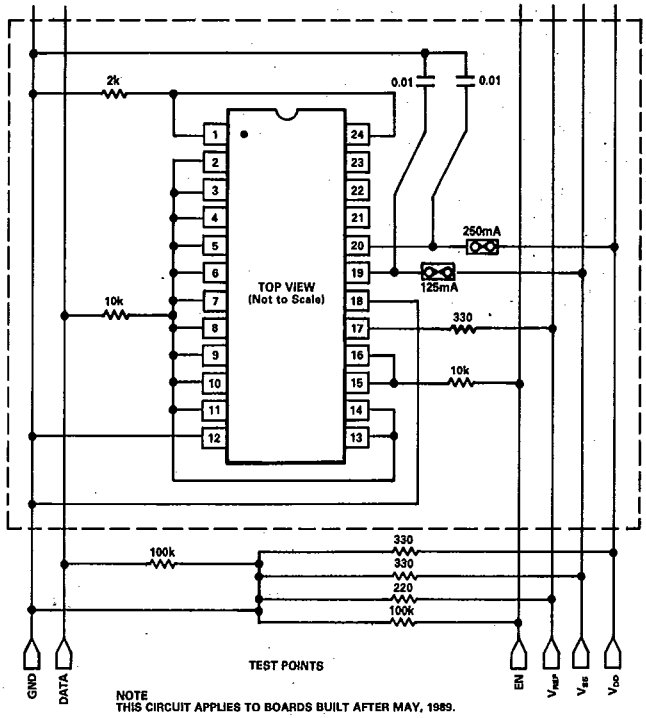
Timing Diagram

3.2.4 Microcircuit Technology Group.

This microcircuit is covered by technology group (80).

4.2.1 Life Test/Burn-In Circuit.

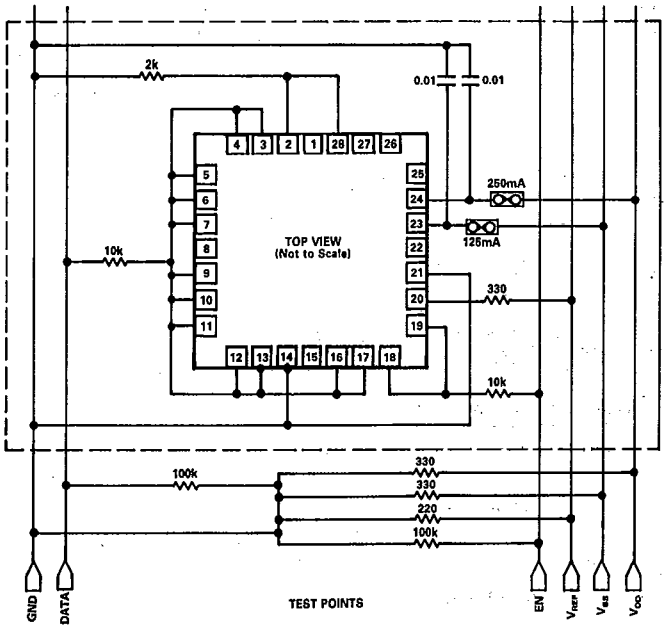
Steady state life test is per MIL-STD-883 Method 1005. Burn-in is per MIL-STD-883 Method 1015 test condition (B).



AD7845 Edge Connections

STATIC BURN-IN CONDITIONS
APPLY VOLTAGES IN THE FOLLOWING SEQUENCE:

1. V_{SS}	−15V	(V2)
2. V_{DD}	+15V	(V5)
3. V_{REF}	−10 V	(V4)
4. ENABLE	GND	(V1)
5. DATA	+15 V	



AD7845 Edge Connections

DYNAMIC BURN-IN CONDITIONS
APPLY VOLTAGES IN THE FOLLOWING SEQUENCE:

1. V_{SS}	−15V	(V2)
2. V_{DD}	+15V	(V5)
3. V_{REF}	−10 V	(V4)
4. ENABLE	GND	(V1)
5. DATA	0 To +15 V @ 1kHz, CONTINUOUS	