

# MOS FIELD EFFECT TRANSISTOR $\mu$ PA2727T1A

## SWITCHING N-CHANNEL POWER MOSFET

#### **DESCRIPTION**

The  $\mu$ PA2727T1A is N-channel MOSFET designed for DC/DC converter applications.

#### **FEATURES**

• Low on-state resistance

 $R_{DS(on)1}$  = 9.6 m $\Omega$  MAX. (Vgs = 10 V, ID = 8 A)

 $R_{\text{DS(on)2}}$  = 15  $m\Omega$  MAX. (Vgs = 4.5 V, Ip = 8 A)

• Low QgD

 $Q_{GD} = 3.5 \text{ nC TYP.}$  ( $V_{DD} = 15 \text{ V}$ ,  $I_{D} = 16 \text{ A}$ )

- Built-in gate protection diode
- Thin type surface mount package with heat spreader (8-pin HVSON)
- RoHS Compliant

#### ABSOLUTE MAXIMUM RATINGS (TA = 25°C, All terminals are connected.)

Drain to Source Voltage (V <sub>GS</sub> = 0 V)	VDSS	30	V
Gate to Source Voltage (VDS = 0 V)	Vgss	±20	V
Drain Current (DC)	ID(DC)	±16	Α
Drain Current (pulse) Note1	I <sub>D(pulse)</sub>	±96	Α
Total Power Dissipation Note2	P <sub>T1</sub>	1.5	W
Total Power Dissipation (PW =10 sec) Note2	P <sub>T2</sub>	4.6	W
Channel Temperature	Tch	150	°C
Storage Temperature	Tstg	-55 to +150	°C
Single Avalanche Current Note3	las	16	Α
Single Avalanche Energy Note3	Eas	26	mJ

#### THERMAL RESISTANCE

Channel to Ambient Thermal Resistance Note2	Rth(ch-A)	83.3	°C/W
Channel to Case (Drain) Thermal Resistance	Rth(ch-C)	2.0	°C/W

**Notes 1.** PW  $\leq$  10  $\mu$ s, Duty Cycle  $\leq$  1%

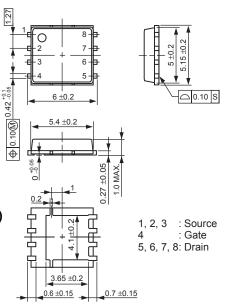
- 2. Mounted on a glass epoxy board of 25.4 mm x 25.4 mm x 0.8 mm
- 3. Starting T<sub>ch</sub> = 25°C, V<sub>DD</sub> = 15 V, R<sub>G</sub> = 25  $\Omega$ , V<sub>GS</sub> = 20  $\rightarrow$  0 V, L = 100  $\mu$ H

## **Remark** The diode connected between the gate and source of the transistor serves as a protector against ESD. When this device actually used, an additional protection circuit is externally required if a voltage exceeding the rated voltage may be applied to this device.

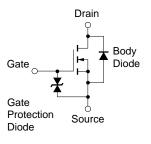
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#### PACKAGE DRAWING (Unit: mm)



#### **EQUIVALENT CIRCUIT**



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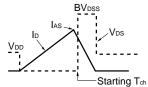
#### <R> ELECTRICAL CHARACTERISTICS (Ta = 25°C, All terminals are connected.)

CHARACTERISTICS	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Zero Gate Voltage Drain Current	IDSS	V <sub>DS</sub> = 30 V, V <sub>GS</sub> = 0 V			10	μΑ
Gate Leakage Current	Igss	V <sub>GS</sub> = ±16 V, V <sub>DS</sub> = 0 V			±10	μΑ
Gate to Source Cut-off Voltage	V <sub>GS(off)</sub>	V <sub>DS</sub> = 10 V, I <sub>D</sub> = 1 mA	1.5		2.5	V
Forward Transfer Admittance Note	yfs	V <sub>DS</sub> = 10 V, I <sub>D</sub> = 8 A	6			S
Drain to Source On-state Resistance Note	R <sub>DS(on)1</sub>	V <sub>GS</sub> = 10 V, I <sub>D</sub> = 8 A		7.6	9.6	mΩ
	R <sub>DS(on)2</sub>	V <sub>GS</sub> = 4.5 V, I <sub>D</sub> = 8 A		11	15	mΩ
Input Capacitance	Ciss	V <sub>DS</sub> = 15 V,		1170		pF
Output Capacitance	Coss	V <sub>GS</sub> = 0 V,		250		pF
Reverse Transfer Capacitance	Crss	f = 1 MHz		90		pF
Turn-on Delay Time	<b>t</b> d(on)	V <sub>DD</sub> = 15 V, I <sub>D</sub> = 8 A,		13		ns
Rise Time	tr	V <sub>GS</sub> = 10 V,		3.6		ns
Turn-off Delay Time	t <sub>d(off)</sub>	R <sub>G</sub> = 10 Ω		41		ns
Fall Time	t <sub>f</sub>			8		ns
Total Gate Charge	Q <sub>G</sub>	V <sub>DD</sub> = 15 V,		11		nC
Gate to Source Charge	Qgs	V <sub>GS</sub> = 5 V,		3.8		nC
Gate to Drain Charge	Q <sub>GD</sub>	I <sub>D</sub> = 16 A		3.5		nC
Body Diode Forward Voltage Note	V <sub>F(S-D)</sub>	I <sub>F</sub> = 16 A, V <sub>GS</sub> = 0 V		0.83		V
Reverse Recovery Time	trr	IF = 16 A, VGS = 0 V,		27		ns
Reverse Recovery Charge	Qrr	di/dt = 100 A/μs		23		nC
Gate Resistance	R <sub>G</sub>	f = 1 MHz		2.2		Ω

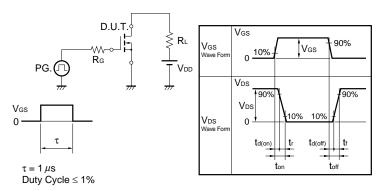
Note Pulsed

#### **TEST CIRCUIT 1 AVALANCHE CAPABILITY**

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#### **TEST CIRCUIT 2 SWITCHING TIME**



#### **TEST CIRCUIT 3 GATE CHARGE**

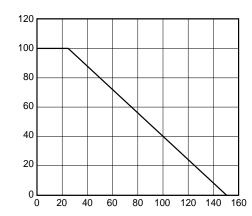
$$\begin{array}{c|c} D.U.T. \\ \hline \\ I_G = 2 \text{ mA} \\ \hline \\ \hline \\ \hline \\ \hline \\ \end{array} \begin{array}{c} R_L \\ \hline \\ V_{DD} \end{array}$$

dT - Percentage of Rated Power - %

lo - Drain Current - A

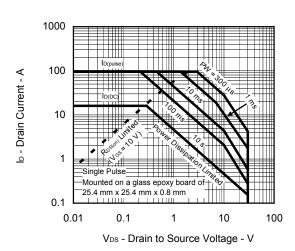
#### <R> TYPICAL CHARACTERISTICS (TA = 25°C)

### DERATING FACTOR OF FORWARD BIAS SAFE OPERATING AREA

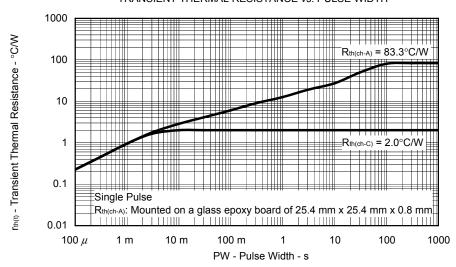


T<sub>A</sub> - Ambient Temperature - °C

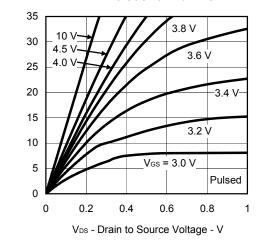
#### FORWARD BIAS SAFE OPERATING AREA



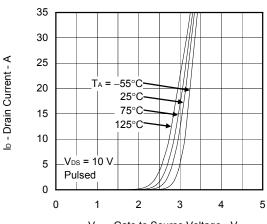
TRANSIENT THERMAL RESISTANCE vs. PULSE WIDTH



DRAIN CURRENT vs.
DRAIN TO SOURCE VOLTAGE

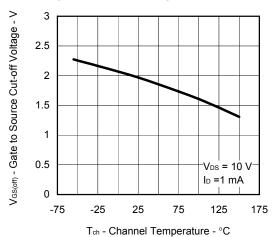


FORWARD TRANSFER CHARACTERISTICS

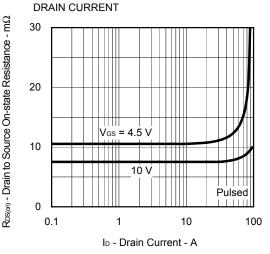


V<sub>GS</sub> - Gate to Source Voltage - V

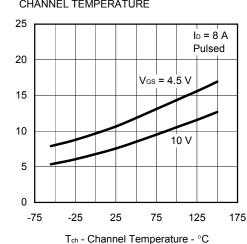
## GATE TO SOURCE CUT-OFF VOLTAGE vs. CHANNEL TEMPERATURE



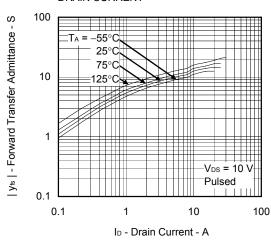
#### DRAIN TO SOURCE ON-STATE RESISTANCE vs.



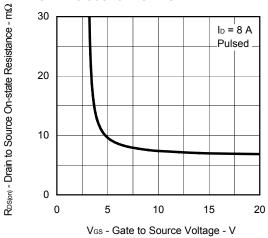
## DRAIN TO SOURCE ON-STATE RESISTANCE vs. CHANNEL TEMPERATURE



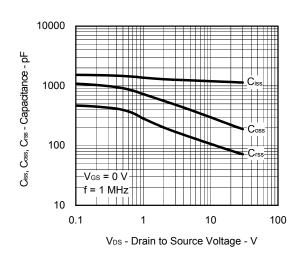
## FORWARD TRANSFER ADMITTANCE vs. DRAIN CURRENT



## DRAIN TO SOURCE ON-STATE RESISTANCE vs. GATE TO SOURCE VOLTAGE

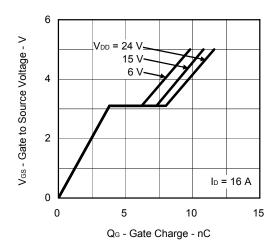


#### CAPACITANCE vs. DRAIN TO SOURCE VOLTAGE

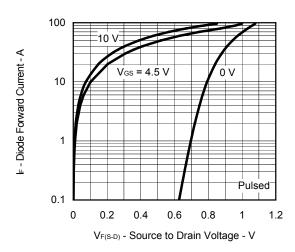


R<sub>DS(on)</sub> - Drain to Source On-state Resistance - mΩ

#### DYNAMIC INPUT/OUTPUT CHARACTERISTICS



#### SOURCE TO DRAIN DIODE FORWARD VOLTAGE



#### **ORDERING INFORMATION**

PART NUMBER	LEAD PLATING	PACKING	PACKAGE	
μPA2727T1A-E1-AZ <sup>Note</sup>	Co. Di			
μPA2727T1A-E2-AZ <sup>Note</sup>	Sn-Bi	T 2000/	8-pin HVSON	
μPA2727T1A-E1-AY Note	D Ca	Tape 3000 p/reel	0.10 g TYP.	
μPA2727T1A-E2-AY Note	Pure Sn			

Note Pb-free (This product does not contain Pb in the external electrode.)

NEC  $\mu$ PA2727T1A

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