

### Features

- $\pm 15V$  Wide Analog Signal Range
- Low "ON" Resistance  $25\Omega$  (Typical)
- High Current Capability 80mA (Typical)
- Break-Before-Make Switching
  - Turn-On Time 370ns (Typical)
  - Turn-Off Time 280ns (Typical)
- No Latch-Up
- Input MOS Gates are Protected from Electrostatic Discharge
- DTL, TTL, CMOS, PMOS Compatible

### Applications

- High Frequency Switching
- Sample and Hold
- Digital Filters
- Operational Amplifier Gain Switching

### Description

This family of CMOS analog switches offers low resistance switching performance for analog voltages up to the supply rails and for signal currents up to 80mA. "ON" resistance is low and stays reasonably constant over the full range of operating signal voltage and current.  $R_{ON}$  remains exceptionally constant for input voltages between +5V and -5V and currents up to 50mA. Switch impedance also changes very little over temperature, particularly between  $0^{\circ}C$  and  $+75^{\circ}C$ .  $R_{ON}$  is nominally  $25\Omega$  for HI-5048 through HI-5051 and HI-5046A and HI-5047A and  $50\Omega$  for HI-5040 through HI-5047.

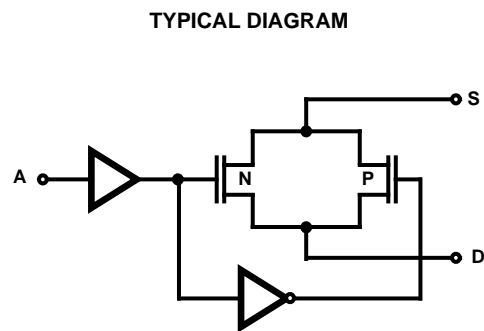
All devices provide break-before-make switching and are TTL and CMOS compatible for maximum application versatility. Performance is further enhanced by Dielectric Isolation processing which insures latch-free operation with very low input and output leakage currents ( $0.8nA$  at  $+25^{\circ}C$ ). This family of switches also features very low power operation ( $1.5mW$  at  $+25^{\circ}C$ ).

There are 14 devices in this switch series which are differentiated by type of switch action and value of  $R_{ON}$  (see Functional Description). All devices are available in 16 lead DIP packages. The HI-5040 and HI-5050 switches can directly replace IH-5040 series devices except IH5048, and are functionally compatible with the DG180 and DG190 family. Each switch type is available in the  $-55^{\circ}C$  to  $+125^{\circ}C$  and  $0^{\circ}C$  to  $+75^{\circ}C$  performance grades.

### Functional Description

PART NUMBER	TYPE	$R_{ON}$
HI-5040	SPST	$50\Omega$
HI-5041	Dual SPST	$50\Omega$
HI-5042	SPDT	$50\Omega$
HI-5043	Dual SPDT	$50\Omega$
HI-5044	DPST	$50\Omega$
HI-5045	Dual DPST	$50\Omega$
HI-5046	DPDT	$50\Omega$
HI-5046A	DPDT	$25\Omega$
HI-5047	4PST	$50\Omega$
HI-5047A	4PST	$25\Omega$
HI-5048	Dual SPST	$25\Omega$
HI-5049	Dual DPST	$25\Omega$
HI-5050	SPDT	$25\Omega$
HI-5051	Dual SPDT	$25\Omega$

### Functional Block Diagram



## HI-5040 Series

### Ordering Information

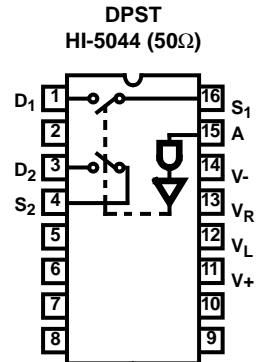
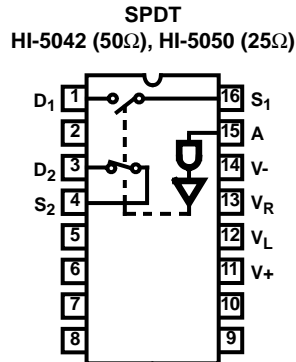
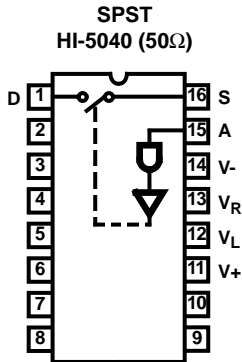
PART NUMBER	TEMPERATURE RANGE	PACKAGE
HI1-5040-7	0°C to +75°C + 96 Hr. Burn-In	16 Lead Ceramic DIP
HI3-5040-5	0°C to +75°C	16 Lead Plastic DIP
HI1-5040-2	-55°C to +125°C	16 Lead Ceramic DIP
HI1-5040-5	0°C to +75°C	16 Lead Ceramic DIP
HI3-5041-5	0°C to +75°C	16 Lead Plastic DIP
HI1-5041-5	0°C to +75°C	16 Lead Ceramic DIP
HI1-5041-2	-55°C to +125°C	16 Lead Ceramic DIP
HI1-5041-7	0°C to +75°C + 96 Hr. Burn-In	16 Lead Ceramic DIP
HI3-5042-5	0°C to +75°C	16 Lead Plastic DIP
HI1-5042-5	0°C to +75°C	16 Lead Ceramic DIP
HI1-5042-7	0°C to +75°C + 96 Hr. Burn-In	16 Lead Ceramic DIP
HI1-5042-2	-55°C to +125°C	16 Lead Ceramic DIP
HI1-5043-7	0°C to +75°C + 96 Hr. Burn-In	16 Lead Ceramic DIP
HI1-5043-2	-55°C to +125°C	16 Lead Ceramic DIP
HI3-5043-5	0°C to +75°C	16 Lead Plastic DIP
HI1-5043-5	0°C to +75°C	16 Lead Ceramic DIP
HI1-5044-7	0°C to +75°C + 96 Hr. Burn-In	16 Lead Ceramic DIP
HI1-5044-5	0°C to +75°C	16 Lead Ceramic DIP
HI3-5044-5	0°C to +75°C	16 Lead Plastic DIP
HI1-5044-2	-55°C to +125°C	16 Lead Ceramic DIP
HI1-5045-5	0°C to +75°C	16 Lead Ceramic DIP
HI1-5045-7	0°C to +75°C + 96 Hr. Burn-In	16 Lead Ceramic DIP
HI1-5045-2	-55°C to +125°C	16 Lead Ceramic DIP
HI3-5045-5	0°C to +75°C	16 Lead Plastic DIP
HI1-5046-2	-55°C to +125°C	16 Lead Ceramic DIP
HI1-5046-5	0°C to +75°C	16 Lead Ceramic DIP
HI1-5046-7	0°C to +75°C + 96 Hr. Burn-In	16 Lead Ceramic DIP
HI3-5046-5	0°C to +75°C	16 Lead Plastic DIP
HI1-5046A-7	0°C to +75°C + 96 Hr. Burn-In	16 Lead Ceramic DIP
HI3-5046A-5	0°C to +75°C	16 Lead Plastic DIP
HI1-5046A-2	-55°C to +125°C	16 Lead Ceramic DIP
HI1-5046A-5	0°C to +75°C	16 Lead Ceramic DIP
HI1-5047-5	0°C to +75°C	16 Lead Ceramic DIP
HI1-5047-7	0°C to +75°C + 96 Hr. Burn-In	16 Lead Ceramic DIP
HI1-5047-2	-55°C to +125°C	16 Lead Ceramic DIP
HI3-5047-5	0°C to +75°C	16 Lead Plastic DIP
HI1-5047A-5	0°C to +75°C	16 Lead Ceramic DIP
HI1-5047A-2	-55°C to +125°C	16 Lead Ceramic DIP
HI3-5047A-5	0°C to +75°C	16 Lead Plastic DIP
HI1-5047A-7	0°C to +75°C + 96 Hr. Burn-In	16 Lead Ceramic DIP

PART NUMBER	TEMPERATURE RANGE	PACKAGE
HI1-5048-5	0°C to +75°C	16 Lead Ceramic DIP
HI1-5048-7	0°C to +75°C + 96 Hr. Burn-In	16 Lead Ceramic DIP
HI3-5048-5	0°C to +75°C	16 Lead Plastic DIP
HI1-5048-2	-55°C to +125°C	16 Lead Ceramic DIP
HI1-5049-5	0°C to +75°C	16 Lead Ceramic DIP
HI1-5049-2	-55°C to +125°C	16 Lead Ceramic DIP
HI3-5049-5	0°C to +75°C	16 Lead Plastic DIP
HI1-5049-7	0°C to +75°C + 96 Hr. Burn-In	16 Lead Ceramic DIP
HI1-5050-5	0°C to +75°C	16 Lead Ceramic DIP
HI1-5050-2	-55°C to +125°C	16 Lead Ceramic DIP
HI3-5050-5	0°C to +75°C	16 Lead Plastic DIP
HI1-5050-7	0°C to +75°C + 96 Hr. Burn-In	16 Lead Ceramic DIP
HI1-5051-5	0°C to +75°C	16 Lead Ceramic DIP
HI1-5051-2	-55°C to +125°C	16 Lead Ceramic DIP
HI1-5051-7	0°C to +75°C + 96 Hr. Burn-In	16 Lead Ceramic DIP
HI4P5051-5	0°C to +75°C	20 Lead PLCC
HI3-5051-5	0°C to +75°C	16 Lead Plastic DIP
HI1-5040/883	-55°C to +125°C	16 Lead Ceramic DIP
HI1-5041/883	-55°C to +125°C	16 Lead Ceramic DIP
HI1-5042/883	-55°C to +125°C	16 Lead Ceramic DIP
HI1-5043/883	-55°C to +125°C	16 Lead Ceramic DIP
HI1-5044/883	-55°C to +125°C	16 Lead Ceramic DIP
HI1-5045/883	-55°C to +125°C	16 Lead Ceramic DIP
HI1-5046/883	-55°C to +125°C	16 Lead Ceramic DIP
HI1-5046A/883	-55°C to +125°C	16 Lead Ceramic DIP
HI1-5047/883	-55°C to +125°C	16 Lead Ceramic DIP
HI1-5047A/883	-55°C to +125°C	16 Lead Ceramic DIP
HI1-5048/883	-55°C to +125°C	16 Lead Ceramic DIP
HI1-5049/883	-55°C to +125°C	16 Lead Ceramic DIP
HI1-5050/883	-55°C to +125°C	16 Lead Ceramic DIP
HI1-5051/883	-55°C to +125°C	16 Lead Ceramic DIP
HI4-5043/883	-55°C to +125°C	20 Lead CLCC
HI4-5045/883	-55°C to +125°C	16 Lead Ceramic DIP
HI4-5051/883	-55°C to +125°C	16 Lead Ceramic DIP
HI9P5043-5	0°C to +75°C	16 SOIC (N)
HI9P5045-5	0°C to +75°C	16 SOIC (N)
HI9P5049-5	0°C to +75°C	16 SOIC (N)
HI9P5051-5	0°C to +75°C	16 SOIC (N)
HI9P5043-9	-40°C to +85°C	16 SOIC (N)
HI9P5045-9	-40°C to +85°C	16 SOIC (N)
HI9P5049-9	-40°C to +85°C	16 SOIC (N)
HI9P5051-9	-40°C to +85°C	16 SOIC (N)

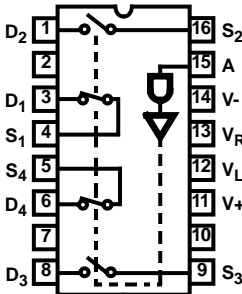
# HI-5040 Series

## Pin Configurations Switch States are Logic "0" Input

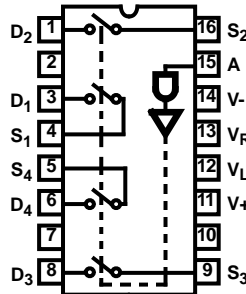
### SINGLE CONTROL



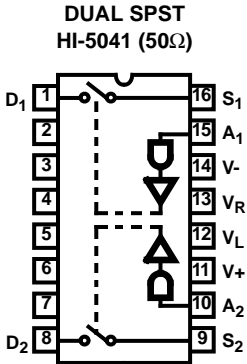
**DPDT**  
HI-5046 (50Ω), HI-5046A (25Ω)



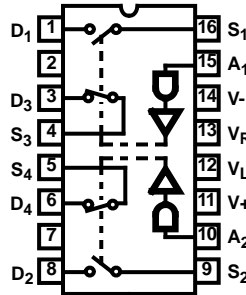
**4PST**  
HI-5047 (50Ω), HI-5047A (25Ω)



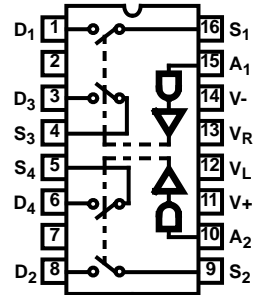
### DUAL CONTROL



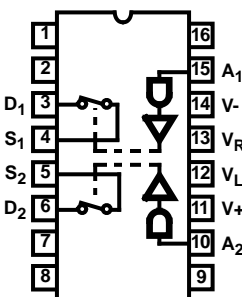
**DUAL SPDT**  
HI-5043 (50Ω), HI-5051 (25Ω)



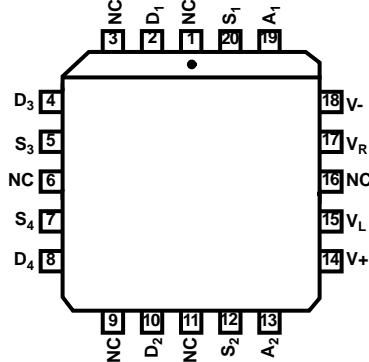
**DUAL DPST**  
HI-5045 (50Ω), HI-5049 (25Ω)



**DUAL SPST**  
HI-5048 (25Ω)



**DUAL SPDT**  
HI-5043 (50Ω), HI-5051 (25Ω)

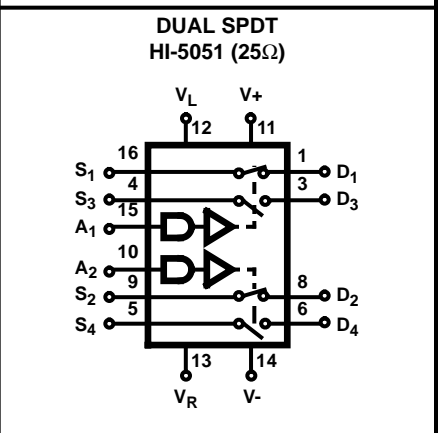
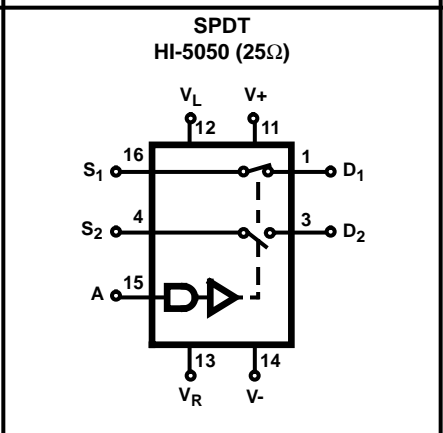
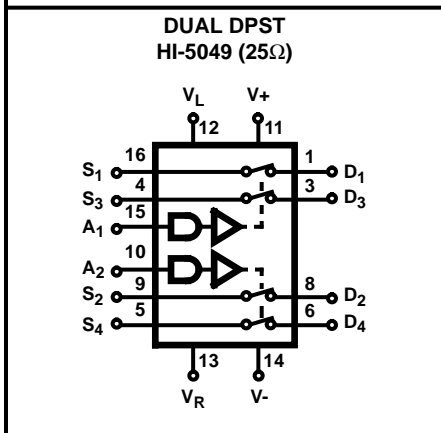
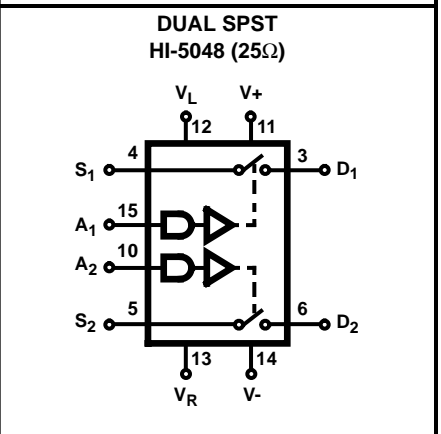
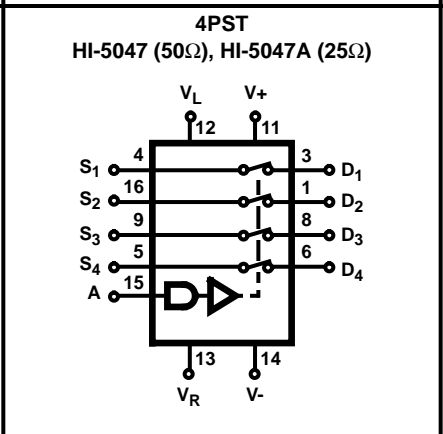
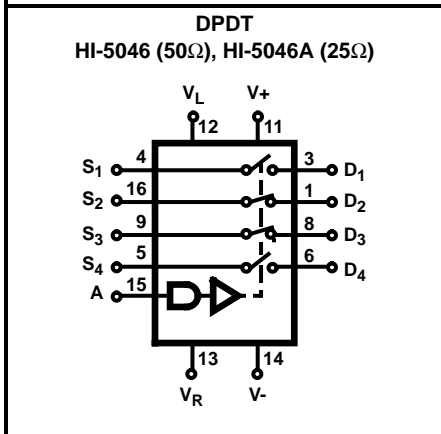
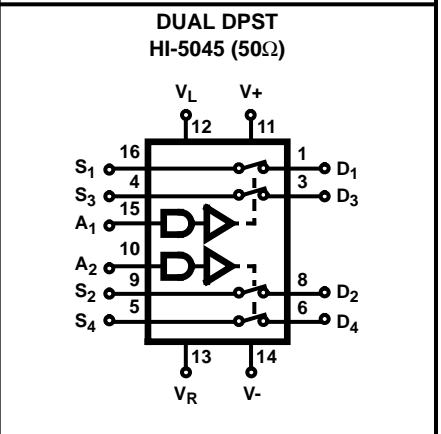
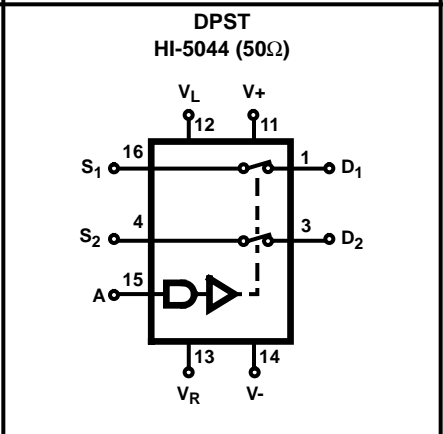
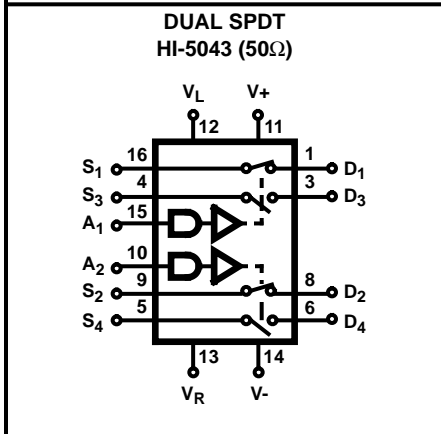
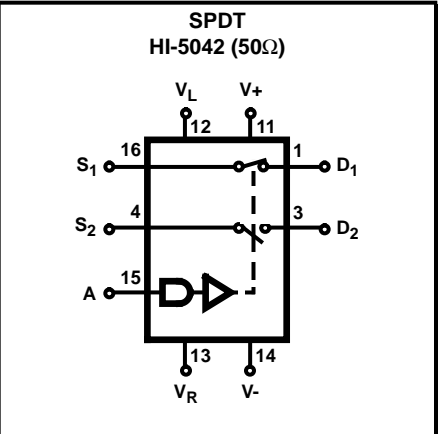
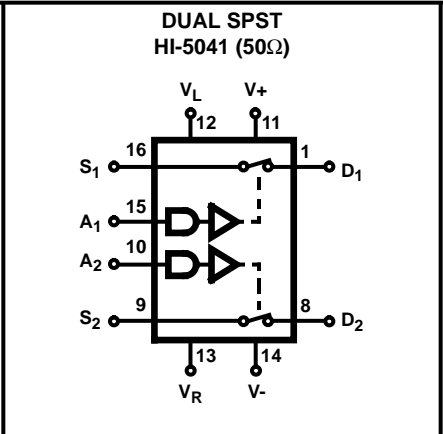
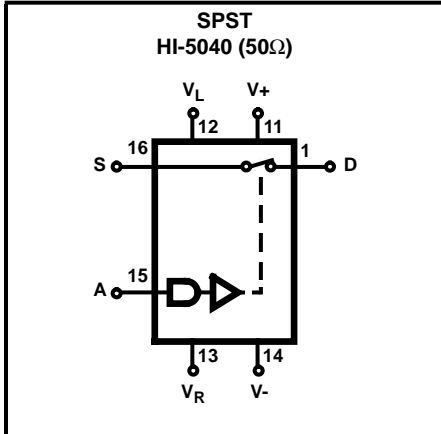


NOTE: Unused pins may be internally connected. Ground all unused pins.

# HI-5040 Series

## Switch Functions

Switch States are Logic "1" Input



## Specifications HI-5040 Series

### Absolute Maximum Ratings

Supply Voltage (V+, V-) . . . . .	36V
V <sub>R</sub> to Ground . . . . .	V+, V-
Digital and Analog Input Voltage . . . . .	+V <sub>SUPPLY</sub> +4V, -V <sub>SUPPLY</sub> -4V
Analog Current (S to D) Continuous . . . . .	30mA
Analog Current (S to D) Peak . . . . .	80mA
Storage Temperature . . . . .	-65°C to +150°C
Lead Temperature (Soldering 10s) . . . . .	+300°C

### Thermal Information

Thermal Resistance	$\theta_{JA}$	$\theta_{JC}$
Ceramic DIP Package . . . . .	80°C/W	24°C/W
SOIC Package . . . . .	120°C/W	-
Plastic DIP Package . . . . .	100°C/W	-
PLCC Package . . . . .	80°C/W	-
CLCC Package . . . . .	75°C/W	20°C/W
Junction Temperature		
Plastic Packages . . . . .	+150°C	
Ceramic Packages . . . . .	+175°C	
Operating Temperature Range		
HI-50XX-2 . . . . .	-55°C to +125°C	
HI-50XX-5, -7 . . . . .	0°C to +75°C	
HI-50XX-9 . . . . .	-40°C to +85°C	

**CAUTION:** Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

### Electrical Specifications

Supplies = +15V, -15V; V<sub>R</sub> = 0V; V<sub>AH</sub> (Logic Level High) = 2.4V, V<sub>AL</sub> (Logic Level Low) = +0.8V, V<sub>L</sub> = +5V, Unless Otherwise Specified. For Test Conditions, Consult Performance Characteristics, Unused Pins are Grounded.

PARAMETER	TEST CONDITIONS	TEMP	-55°C To +125°C			0°C To +75°C			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
<b>SWITCHING CHARACTERISTICS</b>									
t <sub>ON</sub> , Switch On Time	(Note 4)	+25°C	-	370	500	-	370	500	ns
t <sub>OFF</sub> , Switch Off Time	(Note 4)	+25°C	-	280	500	-	280	500	ns
Charge Injection	(Note 2)	+25°C	-	5	20	-	5	-	mV
"Off Isolation"	(Note 3)	+25°C	75	80	-	-	80	-	dB
"Crosstalk"	(Note 3)	+25°C	80	88	-	-	88	-	dB
C <sub>S(OFF)</sub> , Input Switch Capacitance		+25°C	-	11	-	-	11	-	pF
C <sub>D(OFF)</sub> , Output Switch Capacitance		+25°C	-	11	-	-	11	-	pF
C <sub>D(ON)</sub> , Output Switch Capacitance		+25°C	-	22	-	-	22	-	pF
C <sub>A</sub> , Digital Input Capacitance		+25°C	-	5	-	-	5	-	pF
C <sub>DS(OFF)</sub> , Drain-To-Source Capacitance		+25°C	-	0.5	-	-	0.5	-	pF
<b>DIGITAL INPUT CHARACTERISTICS</b>									
V <sub>AL</sub> , Input Low Threshold		Full	-	-	0.8	-	-	0.8	V
V <sub>AH</sub> , Input High Threshold		Full	2.4	-	-	2.4	-	-	V
I <sub>A</sub> , Input Leakage Current (High or Low)		Full	-	0.01	1.0	-	0.01	1.0	μA
<b>ANALOG SWITCH CHARACTERISTICS</b>									
Analog Signal Range		Full	-15	-	+15	-15	-	+15	V
R <sub>ON</sub> , On Resistance	(Note 1A)	+25°C	-	50	75	-	50	75	Ω
R <sub>ON</sub> , On Resistance	(Note 1B)	+25°C	-	-	150	-	-	150	Ω
		Full	-	-	50	-	-	50	Ω
R <sub>ON</sub> , Channel-to-Channel Match	(Note 1A)	+25°C	-	2	10	-	2	10	Ω
R <sub>ON</sub> , Channel-to-Channel Match	(Note 1B)	+25°C	-	1	5	-	1	5	Ω
I <sub>S(OFF)</sub> = I <sub>D(OFF)</sub> , Off Input or Output Leakage Current		+25°C	-	0.8	2	-	0.8	2	nA
		Full	-	100	200	-	100	200	nA

## Specifications HI-5040 Series

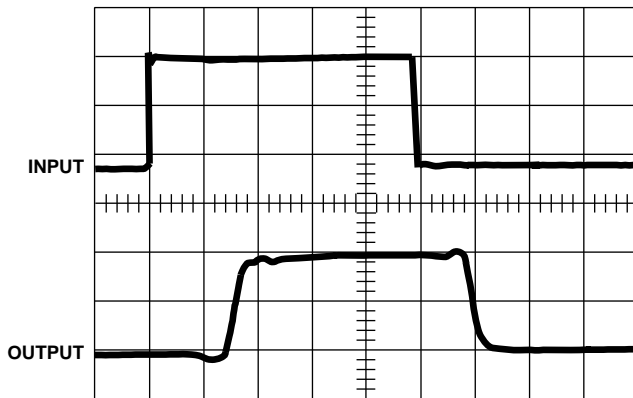
**Electrical Specifications** Supplies = +15V, -15V;  $V_R = 0V$ ;  $V_{AH}$  (Logic Level High) = 2.4V,  $V_{AL}$  (Logic Level Low) = +0.8V,  $V_L = +5V$ , Unless Otherwise Specified. For Test Conditions, Consult Performance Characteristics, Unused Pins are Grounded. (Continued)

PARAMETER	TEST CONDITIONS	TEMP	-55°C To +125°C			0°C To +75°C			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
$I_{D(ON)}$ , On Leakage Current		+25°C	-	0.01	2	-	0.01	2	nA
		Full	-	2	200	-	2	200	nA
<b>POWER REQUIREMENTS</b>									
$P_D$ , Quiescent Power Dissipation		+25°C	-	1.5	-	-	1.5	-	mW
$I_+$ , $I_-$ , $I_L$ , $I_R$		+25°C	-	-	0.2	-	-	0.3	mA
$I_+$ , +15V Quiescent Current	(Note 4)	Full	-	-	0.3	-	-	0.5	mA
$I_-$ , -15V Quiescent Current	(Note 4)	Full	-	-	0.3	-	-	0.5	mA
$I_L$ , +5V Quiescent Current	(Note 4)	Full	-	-	0.3	-	-	0.5	mA
$I_R$ , Ground Quiescent Current	(Note 4)	Full	-	-	0.3	-	-	0.5	mA

**NOTES:**

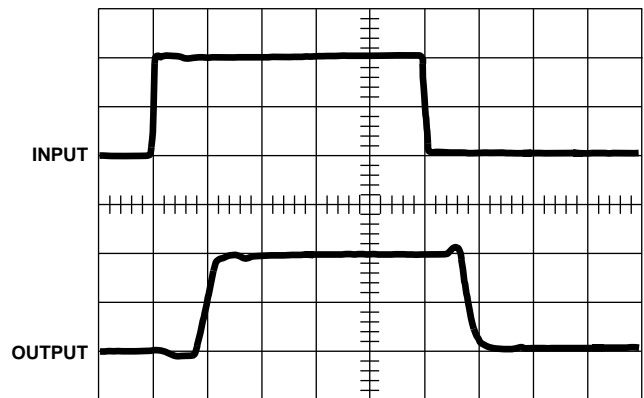
1.  $V_{OUT} = \pm 10V$ ,  $I_{OUT} = \mp 1mA$   
 A). For HI-5040 thru HI-5047  
 B). For HI-5048 thru HI-5051, HI-5046A/5047A.
2.  $V_{IN} = 0V$ ,  $C_L = 10,000pF$ .
3.  $R_L = 100\Omega$ ,  $f = 100kHz$ ,  $V_{IN} = 2.0V_{P-P}$ ,  $C_L = 5pF$ .
4.  $V_{AL} = 0V$ ,  $V_{AH} = 5V$ .

### Switching Waveforms



Top: TTL Input (1V/Div.)  
 $V_{AH} = 5V$ ,  $V_{AL} = 0V$   
 Bottom: Output (2V/Div.)  
 Horizontal: 200ns/Div.

**FIGURE 1.**



Top: CMOS Input (5V/Div.)  
 $V_{AH} = 10V$ ,  $V_{AL} = 0V$   
 Bottom: Output (5V/Div.)  
 Horizontal: 200ns/Div.

**FIGURE 2.**

**Typical Performance Curves and Test Circuits**  $T_A = +25^\circ\text{C}$ ,  $V_+ = +15\text{V}$ ,  $V_- = -15\text{V}$ ,  $V_L = +5\text{V}$ ,  $V_R = 0\text{V}$ ,  $V_{AH} = 3.0\text{V}$  and  $V_{AL} = 0.8\text{V}$ , Unless Otherwise Specified

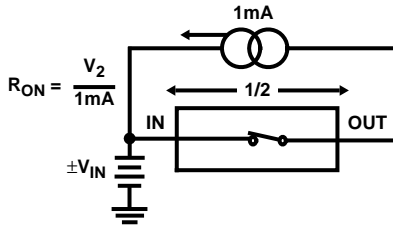


FIGURE 3. "ON" RESISTANCE vs ANALOG SIGNAL LEVEL, SUPPLY VOLTAGE AND TEMPERATURE

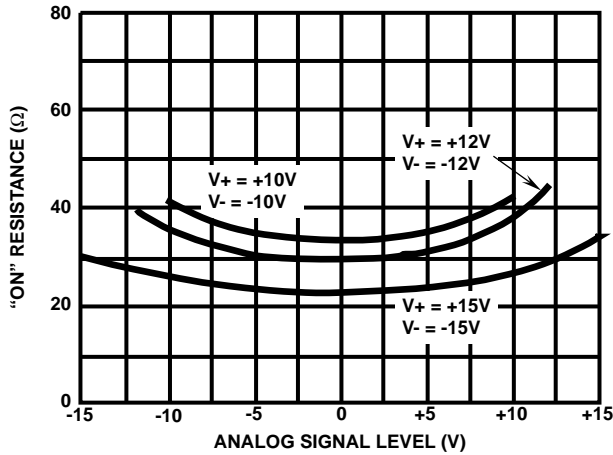


FIGURE 4. "ON" RESISTANCE vs ANALOG SIGNAL LEVEL AND POWER SUPPLY VOLTAGE

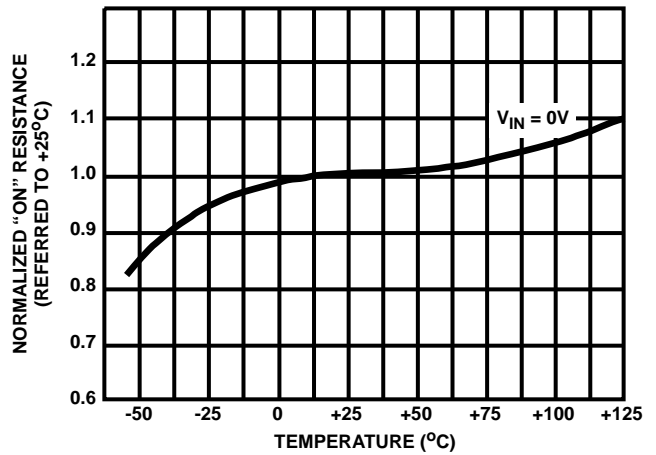


FIGURE 5. NORMALIZED "ON" RESISTANCE vs TEMPERATURE

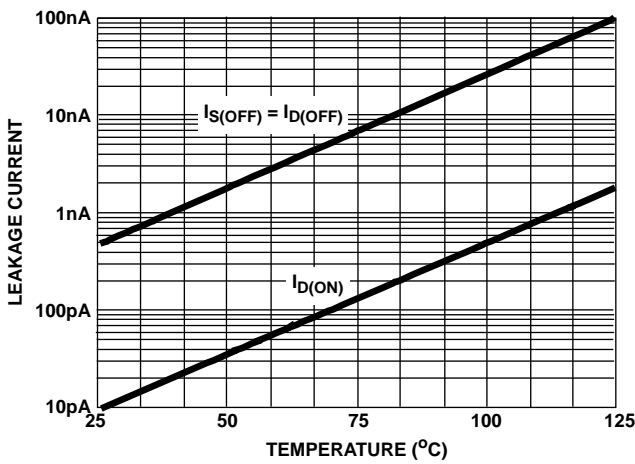
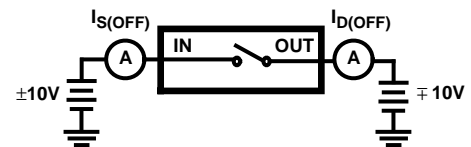
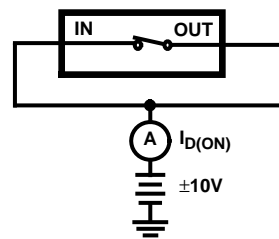


FIGURE 6. ON/OFF LEAKAGE CURRENT vs TEMPERATURE

OFF LEAKAGE CURRENT vs TEMPERATURE



ON LEAKAGE CURRENT vs TEMPERATURE



Typical Performance Curves and Test Circuits

$T_A = +25^\circ\text{C}$ ,  $V_+ = +15\text{V}$ ,  $V_- = -15\text{V}$ ,  $V_L = +5\text{V}$ ,  $V_R = 0\text{V}$ ,  $V_{AH} = 3.0\text{V}$  and  $V_{AL} = 0.8\text{V}$ , Unless Otherwise Specified (Continued)

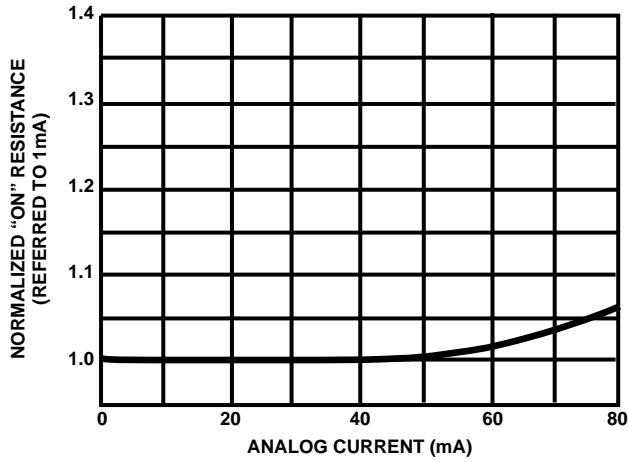


FIGURE 7. NORMALIZED "ON" RESISTANCE vs ANALOG CURRENT

"ON" RESISTANCE vs ANALOG CURRENT

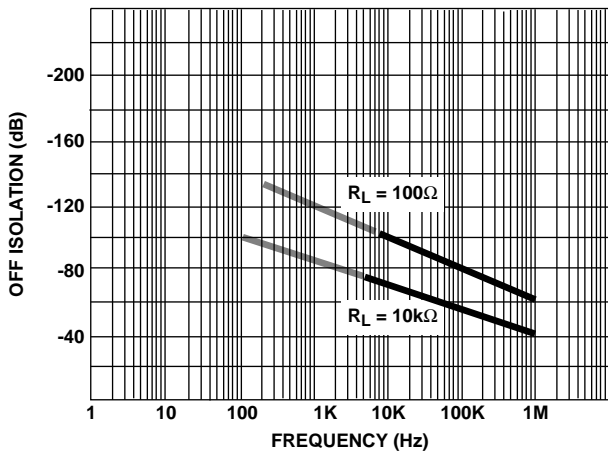
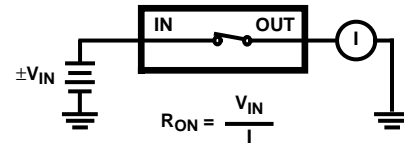


FIGURE 8. "OFF" ISOLATION vs FREQUENCY

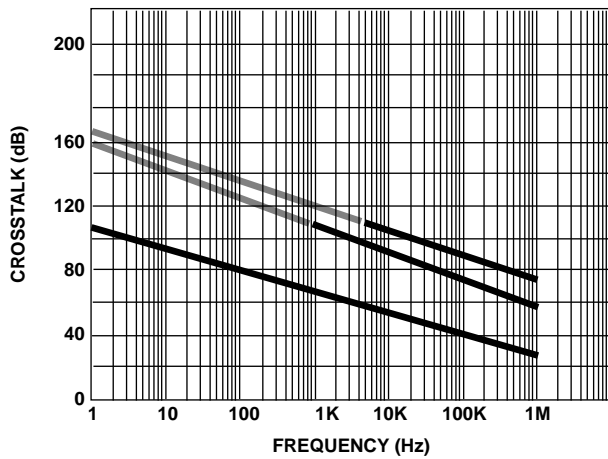
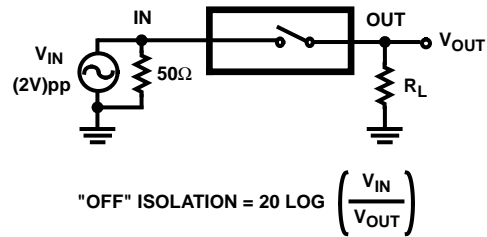
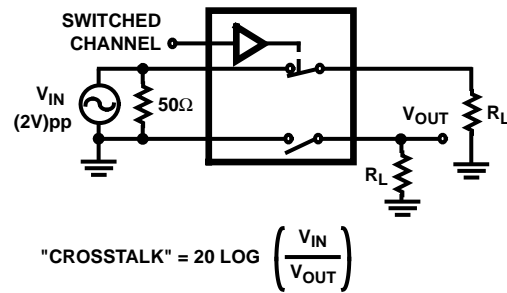


FIGURE 9. CROSSTALK vs FREQUENCY





**Typical Performance Curves and Test Circuits**  $T_A = +25^\circ\text{C}$ ,  $V_+ = +15\text{V}$ ,  $V_- = -15\text{V}$ ,  $V_L = +5\text{V}$ ,  $V_R = 0\text{V}$ ,  $V_{AH} = 3.0\text{V}$  and  $V_{AL} = 0.8\text{V}$ , Unless Otherwise Specified (Continued)

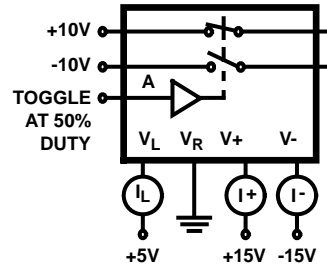
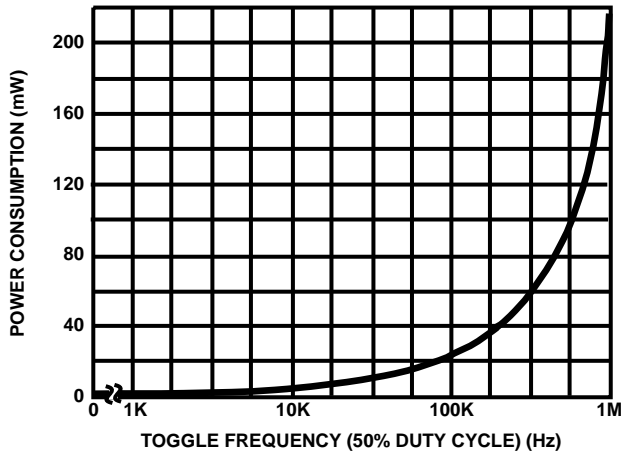


FIGURE 10. POWER CONSUMPTION vs FREQUENCY

**Switching Characteristics**

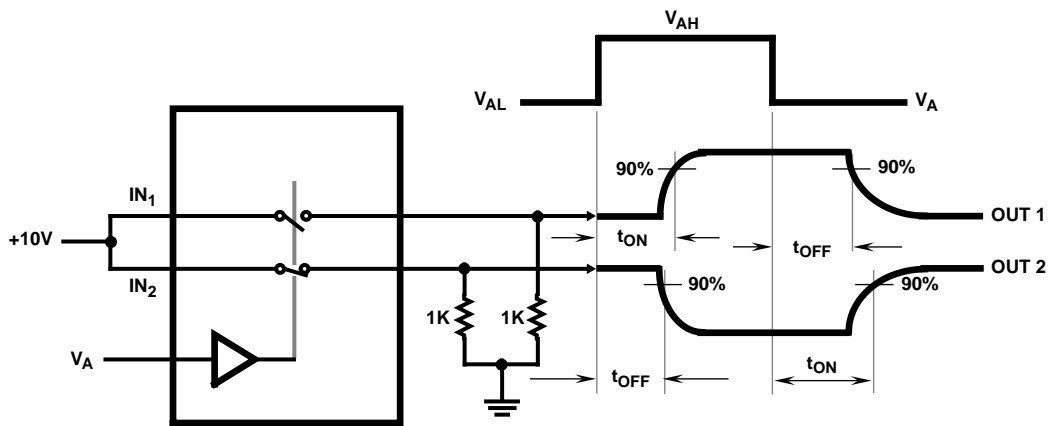


FIGURE 11. ON/OFF SWITCH TIME vs LOGIC LEVEL

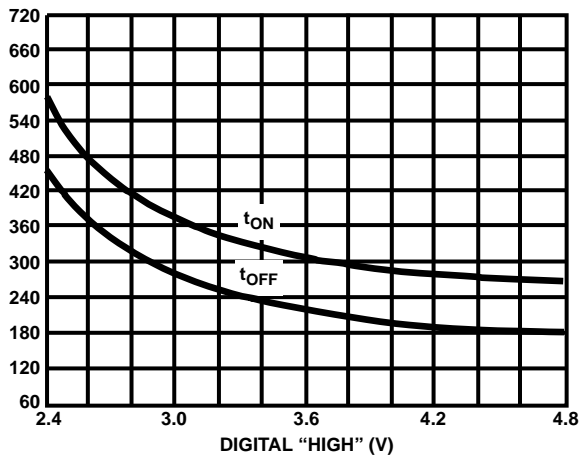


FIGURE 12. SWITCHING TIMES FOR POSITIVE DIGITAL TRANSITION

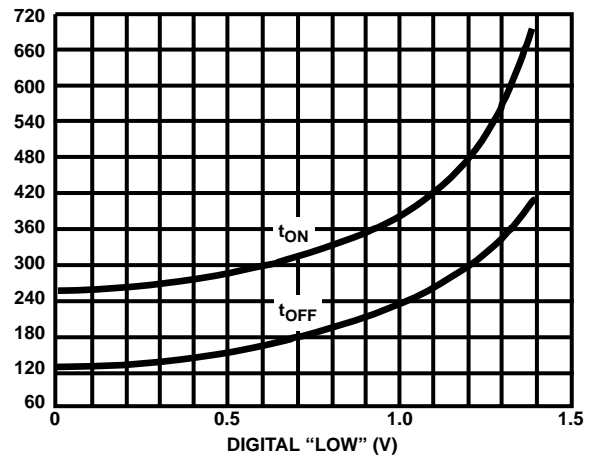


FIGURE 13. SWITCHING TIMES FOR NEGATIVE DIGITAL TRANSITION

Switching Characteristics (Continued)

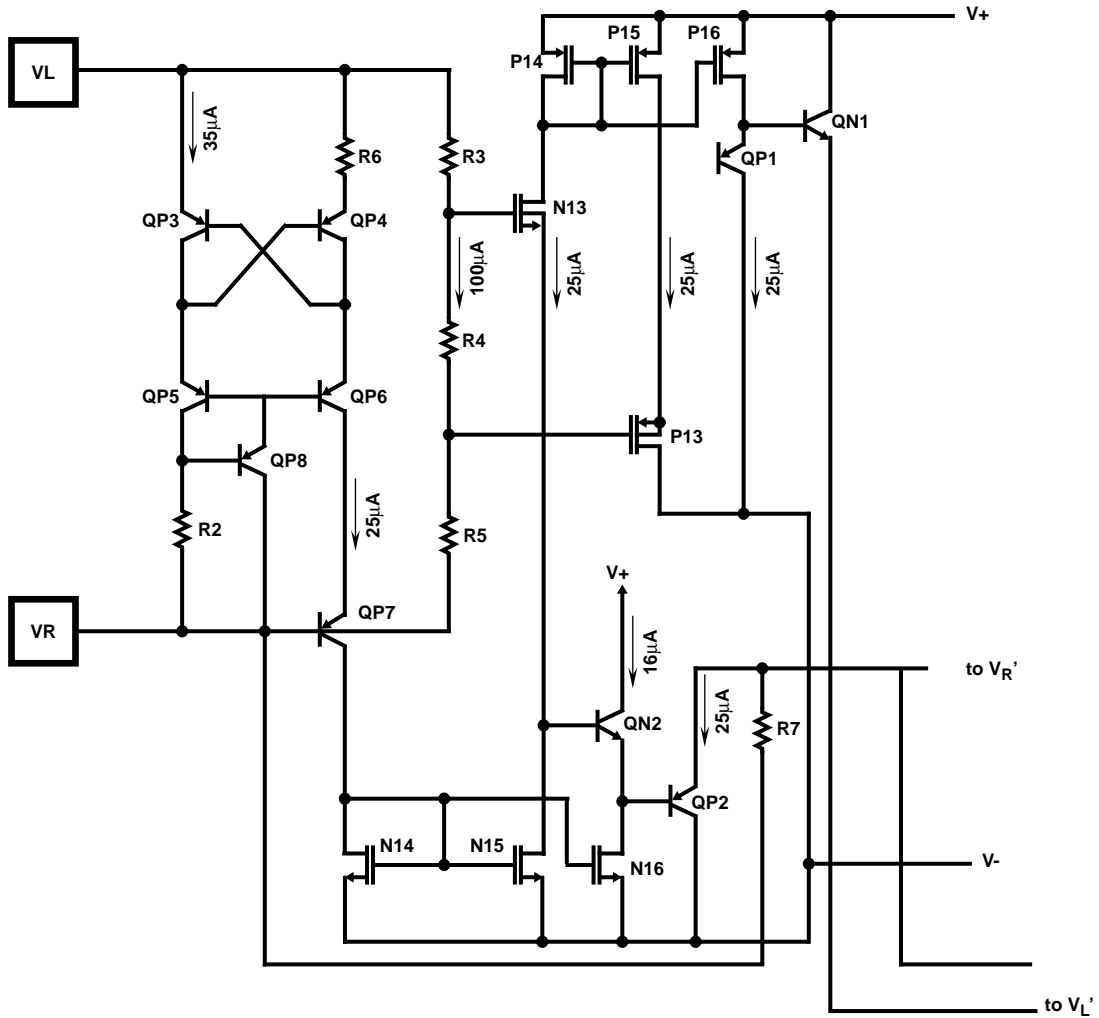


FIGURE 14. TTL/CMOS REFERENCE CIRCUIT (Note 1)

NOTE:

1. Connect V+ to VL for minimizing power consumption when driving from CMOS circuits.

Switching Characteristics (Continued)

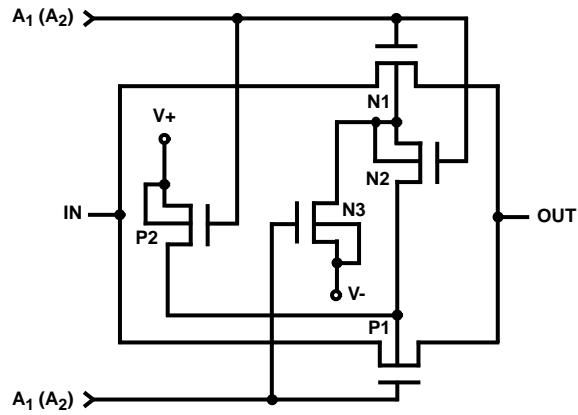
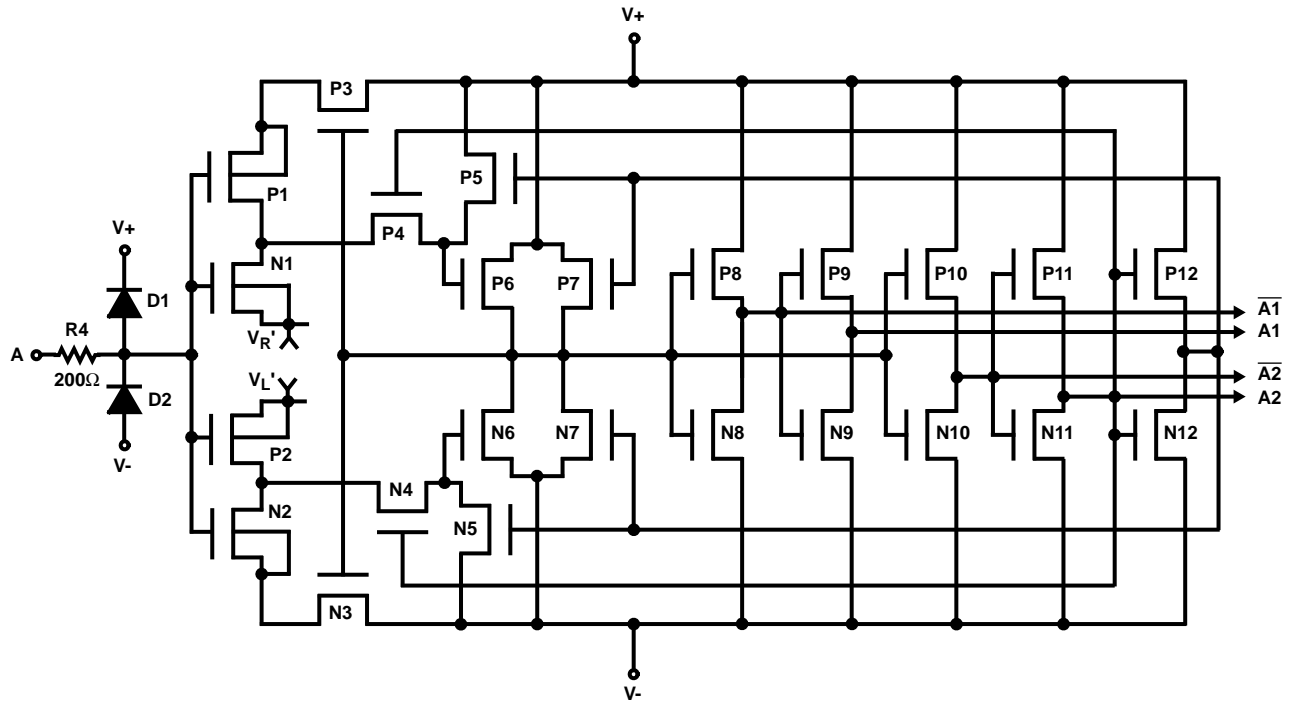


FIGURE 15. SWITCH CELL



NOTES:

1. All n-channel bodies to V-, all p-channel bodies to V+ except as shown.
2. For further information refer to Application Notes 520, 521, 531, 532 and 557.

FIGURE 16. DIGITAL INPUT BUFFER AND LEVEL SHIFTER