

MM54HC165/MM74HC165 Parallel-in/Serial-out 8-Bit Shift Register

General Description

The MM54HC165/MM74HC165 high speed PARALLEL-IN/SERIAL-OUT SHIFT REGISTER utilizes advanced silicon-gate CMOS technology. It has the low power consumption and high noise immunity of standard CMOS integrated circuits, along with the ability to drive 10 LS-TTL loads.

This 8-bit serial shift register shifts data from Q_A to Q_H when clocked. Parallel inputs to each stage are enabled by a low level at the SHIFT/LOAD input. Also included is a gated CLOCK input and a complementary output from the eighth bit.

Clocking is accomplished through a 2-input NOR gate permitting one input to be used as a CLOCK INHIBIT function. Holding either of the CLOCK inputs high inhibits clocking, and holding either CLOCK input low with the SHIFT/LOAD input high enables the other CLOCK input. Data transfer occurs on the positive going edge of the clock. Parallel load-

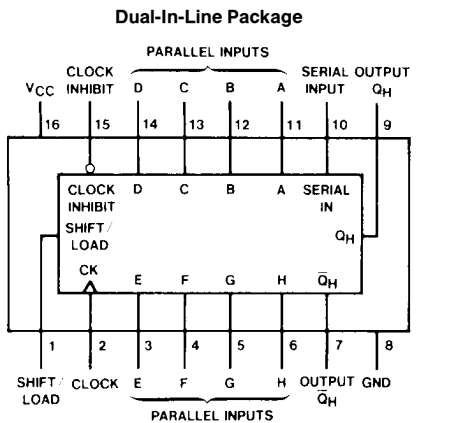
ing is inhibited as long as the SHIFT/LOAD input is high. When taken low, data at the parallel inputs is loaded directly into the register independent of the state of the clock.

The 54HC/74HC logic family is functionally as well as pin-out compatible with the standard 54LS/74LS logic family. All inputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

Features

- Typical propagation delay: 20 ns (clock to Q)
- Wide operating supply voltage range: 2–6V
- Low input current: 1 μ A maximum
- Low quiescent supply current: 80 μ A maximum (74HC Series)
- Fanout of 10 LS-TTL loads

Connection Diagram



TL/F/5316-1

Top View

Order Number MM54HC165 or MM74HC165

Function Table

Shift/Load	Clock Inhibit	Clock	Serial	Internal Outputs		Output Q_H
				Q_A	Q_B	
L	X	X	X	a . . . h	a b	h
H	L	L	X	X	Q_{A0} Q_{B0}	Q_{H0}
H	L	\uparrow	H	X	H Q_{AN}	Q_{GN}
H	L	\uparrow	L	X	L Q_{AN}	Q_{GN}
H	H	X	X	X	Q_{A0} Q_{B0}	Q_{H0}

H = High Level (steady state), L = Low Level (steady state)

X = Irrelevant (any input, including transitions)

\uparrow = Transition from low to high level

Q_{A0} , Q_{B0} , Q_{H0} = The level of Q_A , Q_B , or Q_H , respectively, before the indicated steady-state input conditions were established.

Q_{AN} , Q_{GN} = The level of Q_A or Q_G before the most recent \uparrow transition of the clock; indicates a one-bit shift.

Absolute Maximum Ratings (Notes 1 & 2)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC})	-0.5 to +7.0V
DC Input Voltage (V_{IN})	-1.5 to $V_{CC} + 1.5V$
DC Output Voltage (V_{OUT})	-0.5 to $V_{CC} + 0.5V$
Clamp Diode Current (I_{IK}, I_{OK})	± 20 mA
DC Output Current, per pin (I_{OUT})	± 25 mA
DC V_{CC} or GND Current, per pin (I_{CC})	± 50 mA
Storage Temperature Range (T_{STG})	-65°C to +150°C
Power Dissipation (P_D) (Note 3)	600 mW
S.O. Package only	500 mW
Lead Temperature (T_L) (Soldering 10 seconds)	260°C

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})	2	6	V
DC Input or Output Voltage (V_{IN}, V_{OUT})	0	V_{CC}	V
Operating Temp. Range (T_A)			
MM74HC	-40	+85	°C
MM54HC	-55	+125	°C
Input Rise or Fall Times (t_r, t_f)			
$V_{CC} = 2.0V$		1000	ns
$V_{CC} = 4.5V$		500	ns
$V_{CC} = 6.0V$		400	ns

DC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions	V_{CC}	$T_A = 25^\circ C$			74HC	54HC	Units
							$T_A = -40$ to $85^\circ C$	$T_A = -55$ to $125^\circ C$	
				Typ	Guaranteed Limits				
V_{IH}	Minimum High Level Input Voltage		2.0V		1.5	1.5	1.5	V	
			4.5V		3.15	3.15	3.15	V	
			6.0V		4.2	4.2	4.2	V	
V_{IL}	Maximum Low Level Input Voltage**		2.0V		0.5	0.5	0.5	V	
			4.5V		1.35	1.35	1.35	V	
			6.0V		1.8	1.8	1.8	V	
V_{OH}	Minimum High Level Output Voltage	$V_{IN} = V_{IH}$ or V_{IL} $ I_{OUT} \leq 20 \mu A$	2.0V	2.0	1.9	1.9	1.9	V	
			4.5V	4.5	4.4	4.4	4.4	V	
			6.0V	6.0	5.9	5.9	5.9	V	
		$V_{IN} = V_{IH}$ or V_{IL} $ I_{OUT} \leq 4.0$ mA $ I_{OUT} \leq 5.2$ mA	4.5V	4.2	3.98	3.84	3.7	V	
			6.0V	5.7	5.48	5.34	5.2	V	
V_{OL}	Maximum Low Level Output Voltage	$V_{IN} = V_{IH}$ or V_{IL} $ I_{OUT} \leq 20 \mu A$	2.0V	0	0.1	0.1	0.1	V	
			4.5V	0	0.1	0.1	0.1	V	
			6.0V	0	0.1	0.1	0.1	V	
		$V_{IN} = V_{IH}$ or V_{IL} $ I_{OUT} \leq 4.0$ mA $ I_{OUT} \leq 5.2$ mA	4.5V	0.2	0.26	0.33	0.4	V	
			6.0V	0.2	0.26	0.33	0.4	V	
I_{IN}	Maximum Input Current	$V_{IN} = V_{CC}$ or GND $V_{CC} = 2-6V$	6.0V		± 0.1	± 1.0	± 1.0	μA	
I_{CC}	Maximum Quiescent Supply Current	$V_{IN} = V_{CC}$ or GND $I_{OUT} = 0 \mu A$ $V_{CC} = 2-6V$	6.0V		8.0	80	160	μA	

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: -12 mW/°C from 65°C to 85°C; ceramic "J" package: -12 mW/°C from 100°C to 125°C.

Note 4: For a power supply of $5V \pm 10\%$ the worst case output voltages (V_{OH} , and V_{OL}) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case V_{IH} and V_{IL} occur at $V_{CC} = 5.5V$ and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst case leakage current (I_{IN} , I_{CC} , and I_{OZ}) occur for CMOS at the higher voltage and so the 6.0V values should be used.

** V_{IL} limits are currently tested at 20% of V_{CC} . The above V_{IL} specification (30% of V_{CC}) will be implemented no later than Q1, CY'89.

AC Electrical Characteristics $V_{CC}=5V, T_A=25^{\circ}C, C_L=15\text{ pF}, t_r=t_f=6\text{ ns}$

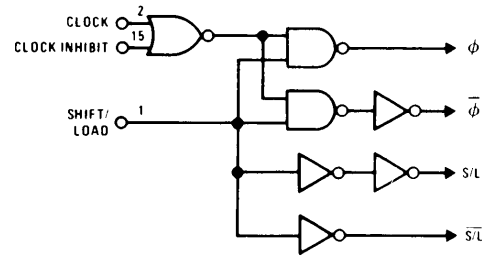
Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
f_{MAX}	Maximum Operating Frequency		50	30	MHz
t_{PHL}, t_{PLH}	Maximum Propagation Delay H to Q_H or \bar{Q}_H		15	25	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay Serial Shift/Parallel Load to Q_H		13	25	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay Clock to Output		15	25	ns
t_S	Minimum Setup Time Serial Input to Clock, Parallel or Data to Shift/Load		10	20	ns
t_S	Minimum Setup Time Shift/Load to Clock		11	20	ns
t_S	Minimum Setup Time Clock Inhibit to Clock		10	20	ns
t_H	Minimum Hold Time Serial Input to Clock or Parallel Data to Shift/Load			0	ns
t_W	Minimum Pulse Width Clock			16	ns

AC Electrical Characteristics $C_L=50\text{ pF}, t_r=t_f=6\text{ ns}$ (unless otherwise specified)

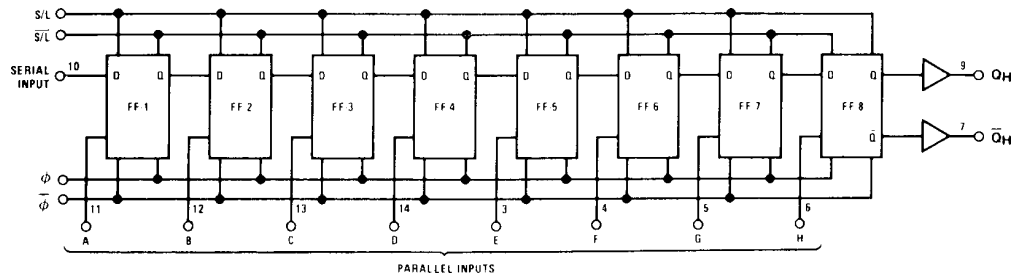
Symbol	Parameter	Conditions	V_{CC}	$T_A=25^{\circ}C$			74HC $T_A=-40\text{ to }85^{\circ}C$		54HC $T_A=-55\text{ to }125^{\circ}C$		Units
				Typ	Guaranteed Limits		Guaranteed Limits				
f_{MAX}	Maximum Operating Frequency		2.0V	10	5	4	4	MHz			
			4.5V	45	27	21	18	MHz			
			6.0V	50	32	25	21	MHz			
t_{PHL}, t_{PLH}	Maximum Propagation Delay H to Q_H or \bar{Q}_H		2.0V	70	150	189	225	ns			
			4.5V	21	30	38	45	ns			
			6.0V	18	26	33	39	ns			
t_{PHL}, t_{PLH}	Maximum Propagation Delay Serial Shift/Parallel Load to Q_H		2.0V	70	175	220	260	ns			
			4.5V	21	35	44	52	ns			
			6.0V	18	30	37	44	ns			
t_{PHL}, t_{PLH}	Maximum Propagation Delay Clock to Output		2.0V	70	150	189	225	ns			
			4.5V	21	30	38	45	ns			
			6.0V	18	26	33	39	ns			
t_S	Minimum Setup Time Serial Input to Clock, or Parallel Data to Shift/Load		2.0V	35	100	125	150	ns			
			4.5V	11	20	25	30	ns			
			6.0V	9	17	21	25	ns			
t_S	Minimum Setup Time Shift/Load to Clock		2.0V	38	100	125	150	ns			
			4.5V	12	20	25	30	ns			
			6.0V	9	17	21	25	ns			
t_S	Minimum Setup Time Clock Inhibit to Clock		2.0V	35	100	125	150	ns			
			4.5V	11	20	25	30	ns			
			6.0V	9	17	21	25	ns			
t_H	Minimum Hold Time Serial Input to Clock or Parallel Data to Shift/Load		2.0V		0	0	0	ns			
			4.5V		0	0	0	ns			
			6.0V		0	0	0	ns			
t_W	Minimum Pulse Width, Clock		2.0V	30	80	100	120	ns			
			4.5V	9	16	20	24	ns			
			6.0V	8	14	18	20	ns			
t_{THL}, t_{TLH}	Maximum Output Rise and Fall Time		2.0V	30	75	95	110	ns			
			4.5V	9	15	19	22	ns			
			6.0V	8	13	16	19	ns			
t_r, t_f	Maximum Input Rise and Fall Time		2.0V		1000	1000	1000	ns			
			4.5V		500	500	500	ns			
			6.0V		400	400	400	ns			
C_{PD}	Power Dissipation Capacitance (Note 5)	(per package)		100				pF			
C_{IN}	Maximum Input Capacitance			5	10	10	10	pF			

Note 5: C_{PD} determines the no load dynamic power consumption, $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$, and the no load dynamic current consumption, $I_S = C_{PD} V_{CC} f + I_{CC}$.

Logic Diagrams

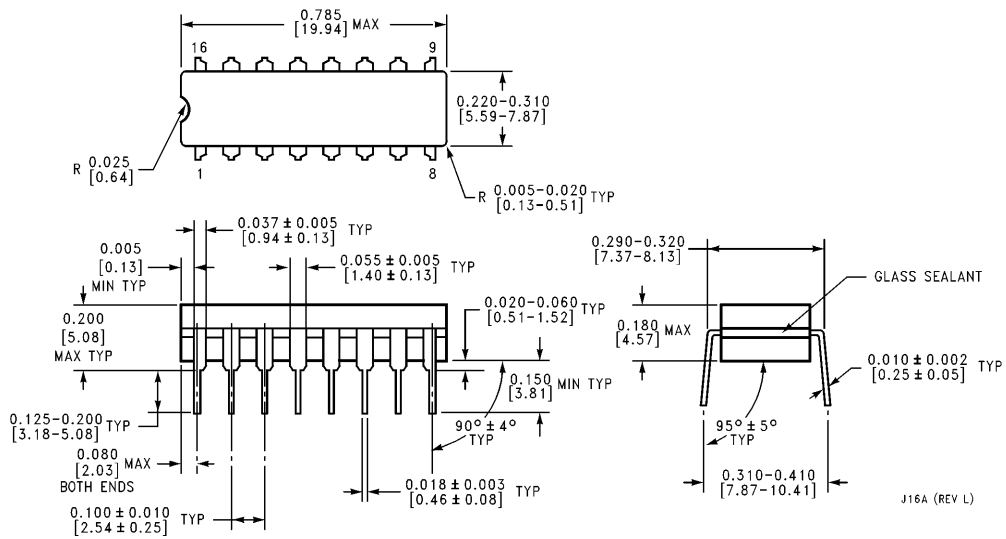


TL/F/5316-2



TL/F/5316-3

Physical Dimensions inches (millimeters)



J16A (REV L)

Dual-In-Line Package
Order Number MM54HC165J or MM74HC165J
NS Package J16A

