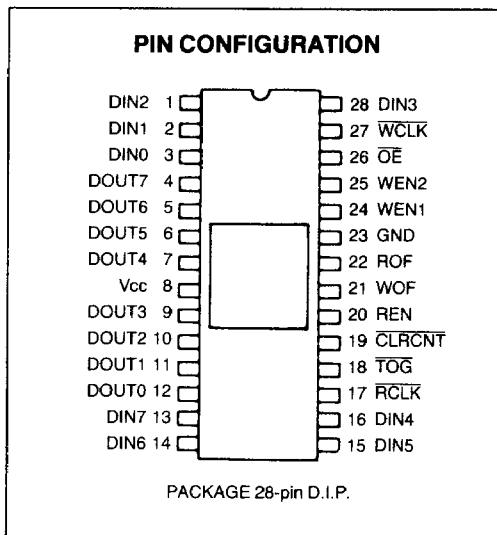


Double Row Buffer DRB

FEATURES

- Low Cost Solution to CRT Memory Contention Problem
- Provides Enhanced Processor Throughput for CRT Display Systems
- Replaces Shift Registers or Several RAM and Counter IC's in CRT Display System
- Permits Display of One Data Row While Next Data Row is Being Loaded
- Data May be Written into Buffer at Less Than the Video Painting Rate
- Double Data Row Buffer Permits Second Data Row to be Loaded Anytime during the Display of the Preceding Data Row
- Permits Active Video on All Scan Lines of Data Row
- Dynamically Variable Number of Characters per Data Row—...64, 80, 132,... up to a Maximum of 135
- Cascadable for Data Rows Greater than 135 Characters
- Stackable for "Invisible Attributes" or Character Widths of Greater than 8 Bits



- Three-State Outputs
- Up to 4 MHz Read/Write Data Rate
- Compatible with SMC CRT 5037, CRT 9007, and other CRT Controllers
- 28 Pin Dual-In-Line Package
- + 5 Volt Only Power Supply
- TTL Compatible

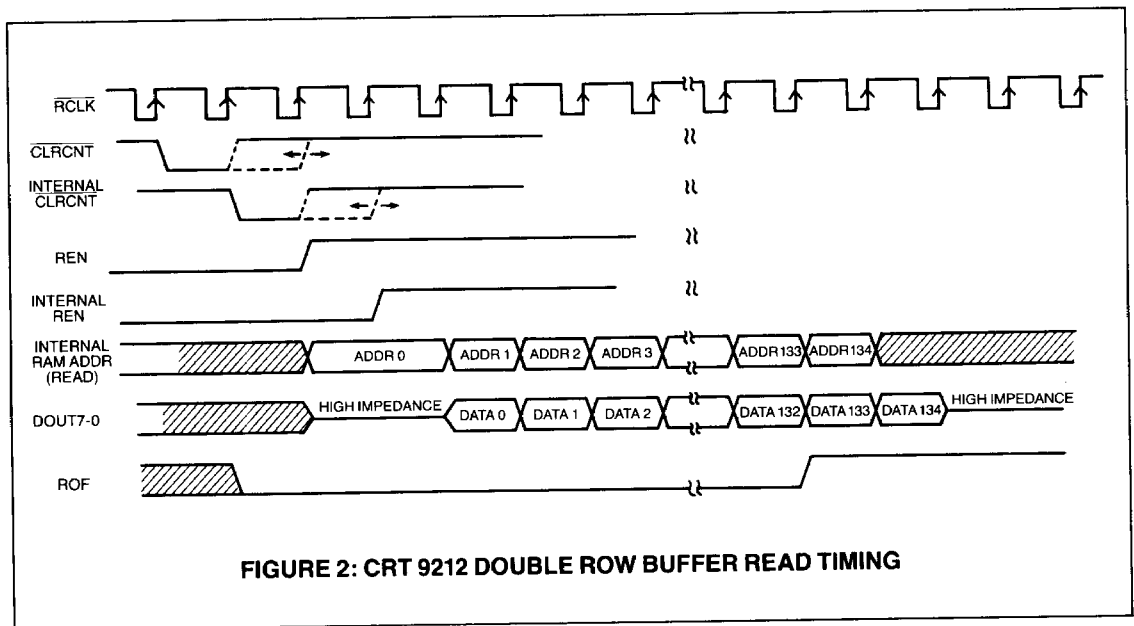
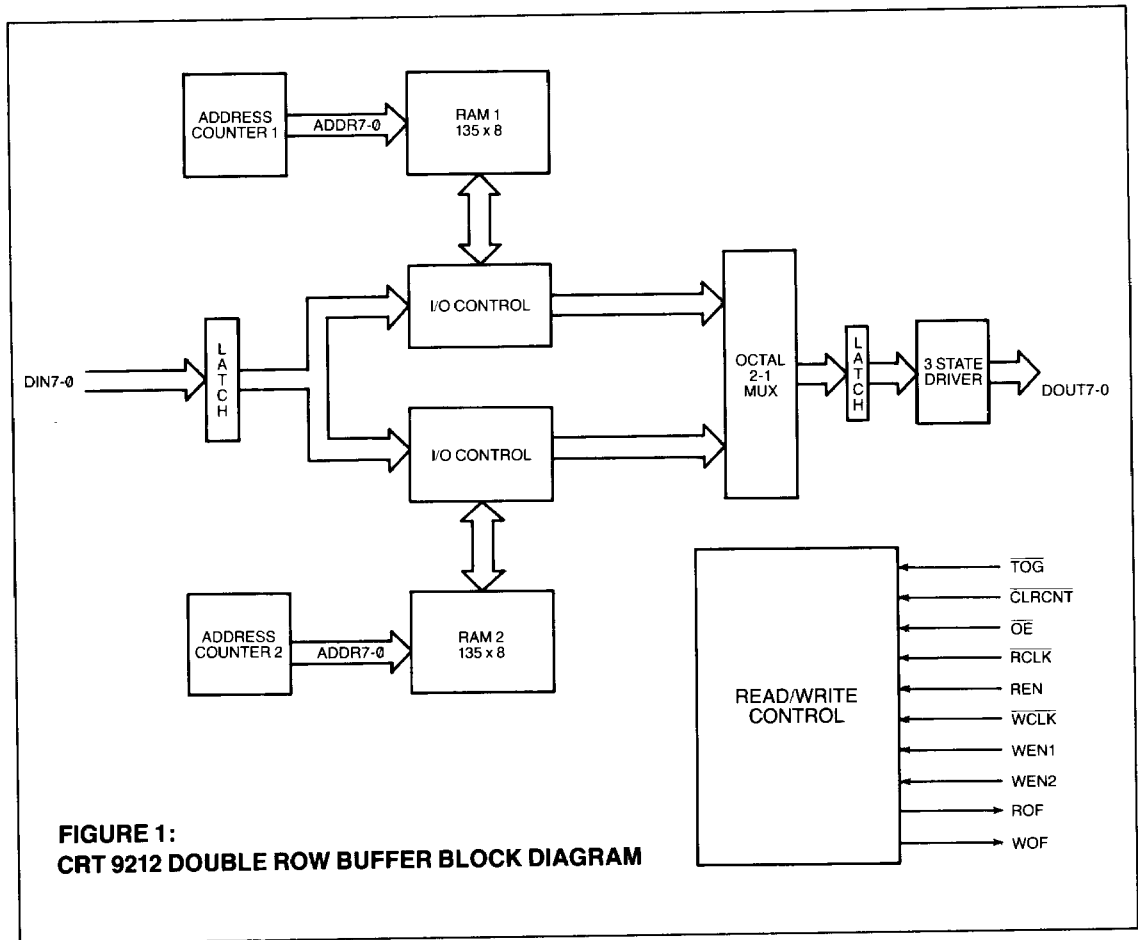
GENERAL DESCRIPTION

The CRT 9212 Double Row Buffer (DRB) provides a low cost solution to memory contention between the system processor and the CRT controller in video display systems.

The CRT 9212 DRB is a RAM-based buffer which provides two rows of buffering. It appears to the system as two octal shift registers of dynamically variable length (2-135 bytes) plus steering logic.

The CRT 9212 permits the loading of one data row

while the previous data row is being displayed. The loading of data may take place during any of the scan line times of the data row. This relaxed time-constraint allows the processor to perform additional processing on the data or service other high priority interrupt conditions (such as a Floppy Disk DMA request) which may occur during a single video scan line. The result is enhanced processor throughput and flicker-free display of data.



DESCRIPTION OF PIN FUNCTIONS

PIN NO.	NAME	SYMBOL	FUNCTION
3-0, 28, 16-13	Data inputs	DIN0-DIN7	DIN0-DIN7 are the data inputs from the system memory.
12-9, 7-4	Data outputs	DOUT0-DOUT7	DOUT0-DOUT7 are the data outputs from the CRT 9212 internal data output latch. Valid information will appear on DOUT0-DOUT7 two RCLK periods after the rising edge of REN. This introduces two pipeline delays when supplying data to the character generator.
17	Read Clock	RCLK	RCLK increments the current "read" address register, clocks data through the "read" buffer and moves data through the internal pipeline at the trailing edge.
18	Toggle Signal	TOG	TOG alternates the function of each buffer between read and write. TOG normally occurs at every data row boundary. Switching of the buffers occurs when both TOG and CLR CNT are low.
19	Clear Counter	CLR CNT	Clear Counter clears the current "read" address counter at the next RCLK positive edge. CLR CNT is normally asserted low at the beginning of each horizontal retrace interval. CLR CNT clears the current "write" address counter when the TOG is active.
20	Read Enable	REN	REN enables the loading of data from the selected "read" buffer into the output latch. Data is loaded when Read Clock is active.
21	Write Overflow	WOF	WOF high indicates that data is being written into the last memory position (position 135). When WOF is high, further writing into the selected "write" buffer is disabled. WOF may be connected to the WEN1 or WEN2 inputs of a second CRT 9212 for cascaded operation where data row lengths of greater than 135 characters are desired. See figure 4.
22	Read Overflow	ROF	The Read Overflow output is high when data is being read from the last memory position (position 135). ROF high disables further reading from the selected "read" buffer. ROF may be connected to the REN input of a second CRT 9212 for cascaded operation where data row lengths of greater than 135 characters are desired. DOUT0-7 will switch into a high impedance state at the second positive transition of RCLK after ROF goes high. See figure 4.
24, 25	Write Enable	WEN1, WEN 2	WEN allows input data to be written into the selected "write" buffer during WCLK active. Both WEN1 and WEN 2 must be high to enable writing. WEN1 has an internal pullup resistor allowing it to assume a high if pin 24 is left open.
26	Output Enable	OE	When the OE input is low, the data outputs DOUT0-DOUT7 are enabled. When OE is high, DOUT0-DOUT7 present a high impedance state. OE has an internal pulldown resistor allowing it to assume a low if pin 26 is left open.
27	Write Clock	WCLK	WCLK clocks input data into the selected "write" buffer and increments the current "write" address register when WEN1 and WEN2 are high.
8	Power Supply	V _{cc}	+ 5 Volt supply
23	Ground	GND	Ground

OPERATION

Figure 1 illustrates the internal architecture of the CRT 9212. It contains 135 bytes of RAM in each of its two buffers. In normal operation, data is written into the input latch on the positive-going edge of Write Clock (WCLK). When both Write Enable (WEN1, WEN 2) signals go high, the next WCLK causes data from the input latch to be written into the selected buffer (1 or 2) and the associated address counter to be incremented by one. Loading of the selected RAM buffer continues until WEN goes inactive or until the buffer has been fully loaded. At the next data row boundary, the Toggle Signal (TOG) will go low. When Clear Counter (CLR CNT) goes low, the next Read Clock (RCLK) will begin to reset both buffer address counters to zero, switching the buffer just loaded from a "write buffer" to a "read buffer", permitting the next row of data to be written into the other buffer. Data from the current "read" buffer is read out of the buffer and to the output latch whenever Read Enable (REN) is high during a Read Clock (RCLK). Each read-out from

the buffer RAM causes the "read" address counter to be incremented. REN is normally high during the entire visible line time of each scan line of the data row. CLR CNT resets the present "read" address counter. The negative edge of CLR CNT is detected by the CRT 9212 and the internal "read" address counter is cleared independent of the CLR CNT pulse width. The CLR CNT input may be tied to the REN input for proper operation.

Figures 2 and 3 illustrate the functional timing for reading and writing the CRT 9212. It is possible to cascade two or more CRT 9212's to allow for data storage greater than 135 bytes by employing the read overflow (ROF) and write overflow (WOF) outputs. Figure 4 illustrates two CRT 9212's cascaded together.

The CRT 9212 is compatible with the CRT 9007 video processor and controller (VPAC™) and the CRT 8002 video display attributes controller (VDAC™). A typical video configuration employing the three parts is illustrated in figure 5.

MAXIMUM GUARANTEED RATINGS*

Operating Temperature Range	0°C to +70°C
Storage Temperature Range	-55°C to +150°C
Lead Temperature (soldering, 10 sec.)	+325°C
Positive Voltage on any Pin, with respect to ground	+8.0V
Negative Voltage on any Pin, with respect to ground	-0.3V

*Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied.

ELECTRICAL CHARACTERISTICS (T_A = 0°C to 70°C, V_{CC} = +5V ± 5%)

PARAMETER	MIN	TYP	MAX	UNITS	COMMENTS
DC CHARACTERISTICS					
INPUT VOLTAGE LEVELS					
Low Level V _{IL}			0.8	V	excluding RCLK; WCLK RCLK, WCLK
High Level V _{HI1}	2.0			V	
High Level V _{HI2}	4.2			V	
OUTPUT VOLTAGE LEVELS					
Low Level V _{OL}			0.4	V	
High Level V _{OH}	2.4			V	
INPUT LEAKAGE CURRENT					
High Leakage I _{LH1}			10	μA	excluding OE excluding WEN1 WEN1 OE
Low Leakage I _{LL1}			10	μA	
High Leakage I _{LH2}			400	μA	
Low Leakage I _{LL2}			400	μA	
INPUT CAPACITANCE					
C _{IN1}		10		pF	excluding RCLK, WCLK RCLK, WCLK
C _{IN2}		15		pF	
POWER SUPPLY CURRENT					
I _{CC}		100		mA	

AC CHARACTERISTICS¹

t _{CYW}	300			ns	Write clock period Read clock period
t _{CYR}	300			ns	
t _{CKH}	247		DC	ns	measured from 10% to 90% points measured from 90% to 10% points referenced to WCLK referenced to WCLK
t _{CKL}	33			ns	
t _{CKR}			10	ns	
t _{CKF}			10	ns	
t _{DS}	50			ns	
t _{DH}	0			ns	
t _{EN1²}	0			ns	
t _{EN2²}	100			ns	
t _{ENH²}	0			ns	
t _{DV}			175	ns	
t _{DOFF}			175	ns	C _L = 30 pF
t _{DON}			175	ns	
t _{OF³}			175	ns	
t _{CS}	100			ns	
t _{CH}	0			ns	
t _{WT⁴}		1t _{CYW}			

1 - Reference points for all AC parameters are 2.4V high and 0.4V low.

2 - For REN, referenced from RCLK; for WEN1 or WEN2 referenced to WCLK.

3 - For ROF, referenced from RCLK; for WOF referenced from WCLK.

4 - At least 1 WCLK rising edge must occur between CLRcnt or TOG (whichever occurs last) and WEN (= WEN1-WEN2).

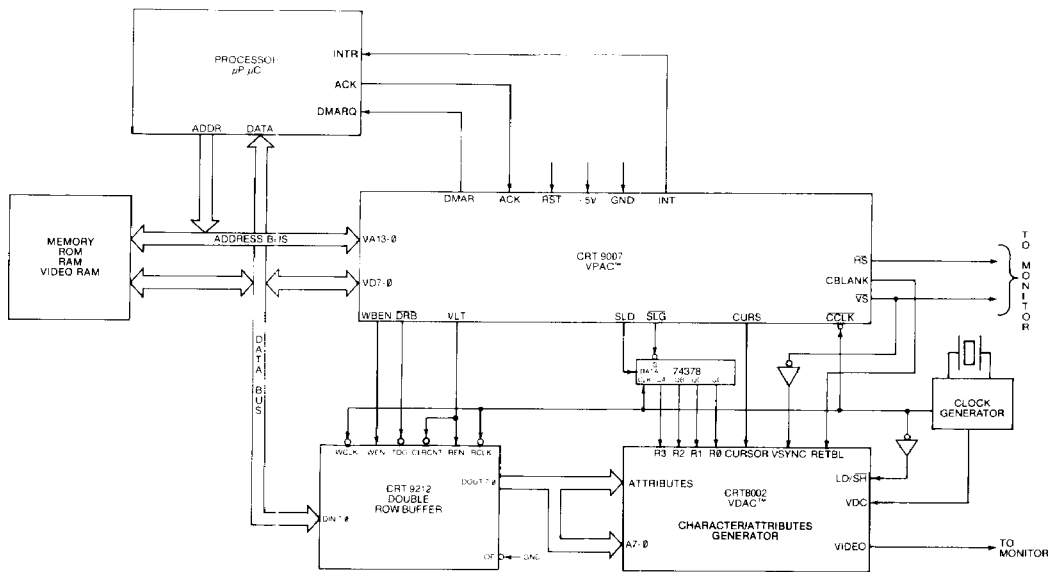


FIGURE 5: CRT 9212 CONFIGURED WITH THE CRT 9007 VPAC AND THE CRT 8002 VDAC™

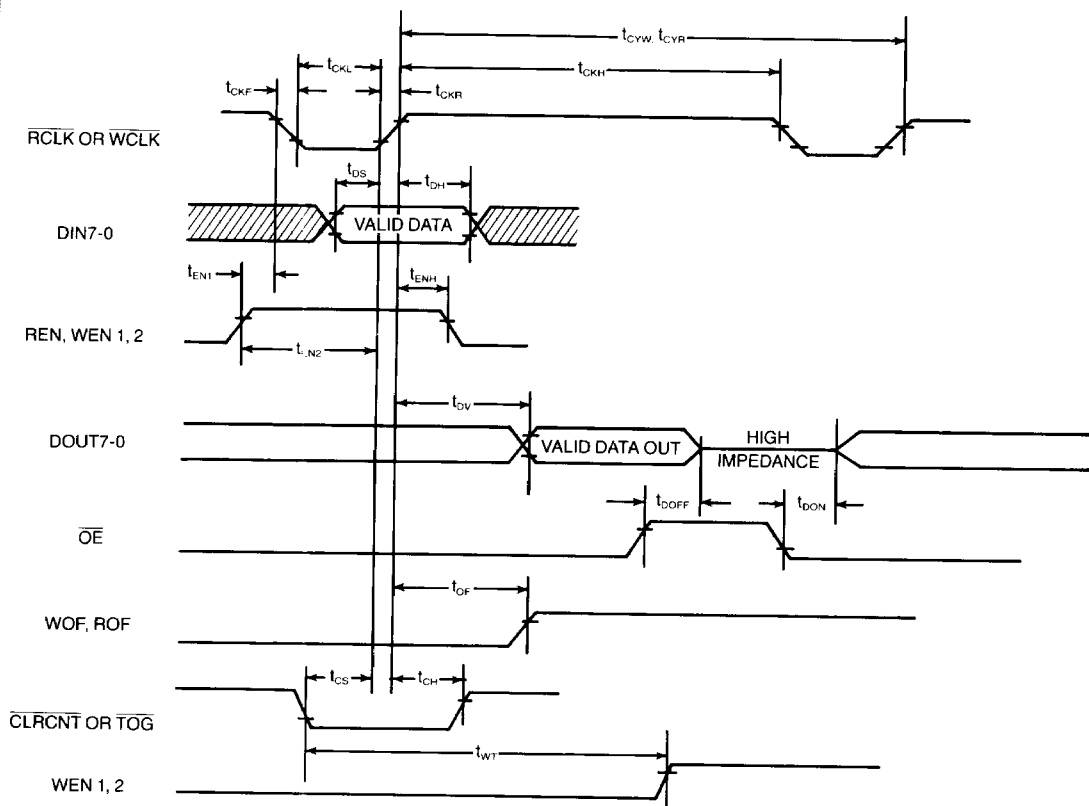


FIGURE 6: CRT 9212 I/O TIMING

