CMOS

LATCHES/FLIP-FLOPS

Item	Function	DEVICE NO.	Data Inputs	Common Clear	Enable/Clock Inputs (Level)	Required Enable/Clock Pulse Width-ns (Typ) V_{DD} = 10V	Enable/Clock to Q Delay-ns (Typ) V_{DD} = 10V	Logic/Connection Diagram	Package(s)
1	Dual JK Flip-Flop	**4027B**	JK	RS	H	35	45	C21	4L,6B,9B
2	Dual D Flip-Flop	**4013B**	D	RS	H	30	38	C22	3I,6A,9A
3	Quad D Flip-Flop	**40175B**	D	X	H	10	35	C23	4L,6B,9B
4	Quad D Flip-Flop w/3-State Ouptuts	**4076B**	D	MR	L	35	35	C110	4L,6B,9B
5	Hex D Flip-Flop	**40174B**	D	X	H	10	35	C24	4L,6B,9B
6	4-Bit Latch	**4042B**	D	—	H	16	66	C25	4L,6B,9B
7	4-Bit Latch	**4043B**	RS	RS	H	14	30	C26	4L,6B,9B
8	4-Bit Latch	**4044B**	RS	RS	H	14	30	C27	4L,6B,9B
9	Dual 4-Bit Address Latch	**4723B**	D	X	L	20	50	C28	4L,6B,9B
10	8-Bit Address Latch	**4724B**	D	X	L	20	40	C29	4L,6B,9B
11	BCD-to-7-Seg Latch/Decoder/Dvr	**4511B**	D	X	L	14	90	C111	4L,6B,9B
12	BCD-to-7-Seg Latch/Decoder/Dvr for Liquid Crystal	**4543B**	D	X	H	40	200	C112	4L,6B,9B
13	BCD-to-7-Seg Latch/Decoder Dvr w/Ripple Blanking	**4734B**	D	X	L	14	90	C114	7D,9M

MULTIPLEXERS

Item	Function	DEVICE NO.	Enable Inputs	True Output	Select Delay ns (Typ) V_{DD} = 10V	Enable Delay ns (Typ) V_{DD} = 10V	Data Delay ns (Typ) V_{DD} = 10V	Logic/Connection Diagram	Package(s)
14	Quad 2-Input	**4019B**	—	X	37	—	37	C30	4L,6B,9B
15	Quad 2-Input	**4519B**	—	X	50	—	50	C31	4L,6B,9B
16	Dual 4-Input	**4539B**	X	X	88	53	71	C32	4L,6B,9B
17	Single 8-Input	**4512B**	X	3-State	85	45	75	C33	4L,6B,9B

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CMOS

DECODERS/DEMULTIPLEXERS (Cont'd)

Item	Function	DEVICE NO.	Address Inputs	Active LOW Enable	Output Configuration	Select Delay ns (Typ) V_{DD} = 10V	Enable Delay ns (Typ) V_{DD} = 10V	Logic/Connection Diagram	Package(s)
1	8-Channel Demultiplexer	**4051B**	3	1	H	125	105	C65	4L,6B,9B
2	BCD-to-7-Segment Latch/Decoder/Dvr	**4511B**	4	1	H	90	98	C111	4L,6B,9B
3	BCD-to-7-Segment Latch/Decoder/ Dvr for Liquid Crystals	**4543B**	4	—	H or L	200	200	C112	4L,6B,9B
4	BCD-to-7-Segment Latch/Decoder/ Dvr w/Ripple Blanking	**4734B**	4	1	H	90	98	C114	7D,9M

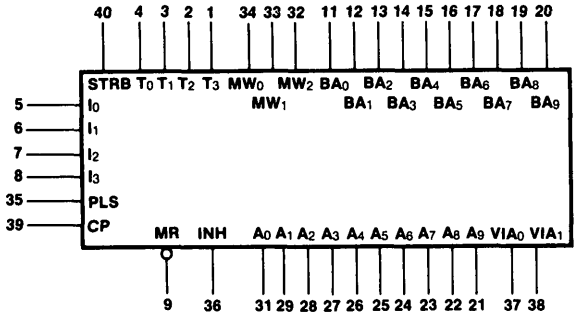
COUNTERS

Item	Function	DEVICE NO.	Modulo	Parallel Load[1]	Clock Transition	Max Clock Rate MHz (Typ) V_{DD} = 10V	Clock to Q Output Delay ns (Typ) V_{DD} = 10V	Logic/Connection Diagram	Package(s)
5	4-Bit Sync Count Up	**40160B**	Decade	S	L→H	12	55	C47	4L,6B,9B
6	4-Bit Sync Count Up	**40161B**	Binary	S	L→H	12	55	C47	4L,6B,9B
7	4-Bit Sync Count Up	**40162B**	Decade	S	L→H	12	55	C48	4L,6B,9B
8	4-Bit Sync Count Up	**40163B**	Binary	S	L→H	12	55	C48	4L,6B,9B
9	4-Bit Sync Count Down	**4522B**[2]	Decade	A	L→H or H→L	10	95	C49	4L,6B,9B
10	4-Bit Sync Count Down	**4526B**[2]	Binary	A	L→H or H→L	10	95	C49	4L,6B,9B
11	4-Bit Sync Count Up/Down	**4510B**	Decade	A	L→H	12	62	C50	4L,6B,9B
12	4-Bit Sync Count Up/Down	**4516B**	Binary	A	L→H	12	62	C50	4L,6B,9B
13	4-Bit Sync Count Up/Down	**40192B**	Decade	A	L→H	80	105	C51	4L,6B,9B

1 A = Asynchronous, S = Synchronous
2 To be announced

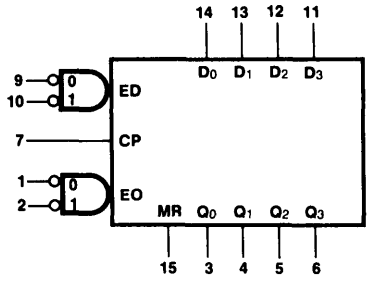
DIGITAL-CMOS

C109
4708B



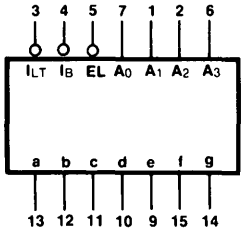
V_{DD} = Pin 10
V_{SS} = Pin 30

C110
4076B



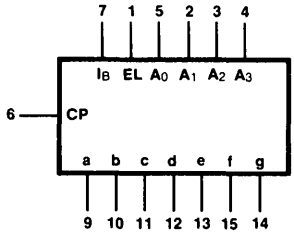
V_{DD} = Pin 16
V_{SS} = Pin 8

C111
4511B



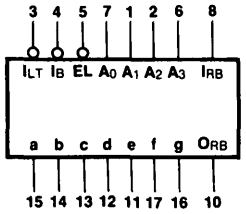
V_{DD} = Pin 16
V_{SS} = Pin 8

C112
4543B



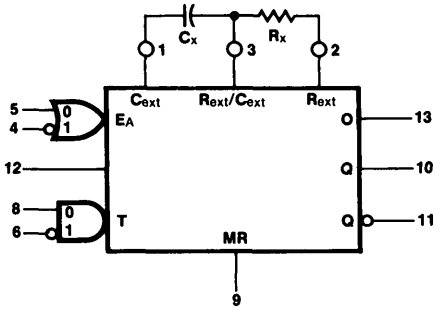
V_{DD} = Pin 18
V_{SS} = Pin 9

C114
4734B



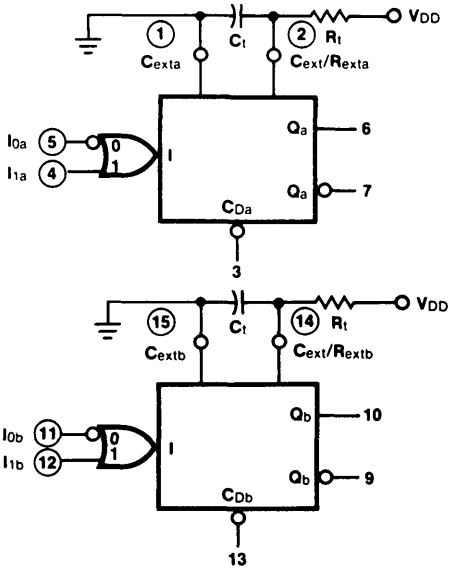
V_{DD} = Pin 16
V_{SS} = Pin 8

C115
4047B



V_{DD} = Pin 14
V_{SS} = Pin 7

C116
4538B



V_{DD} = Pin 16
V_{SS} = Pin 8

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LINE DRIVERS/RECEIVERS/TRANSCEIVERS

TRANCEIVERS (Cont'd)

Item	DEVICE NO.	Function[2]	Driver Output Current-mA	Receiver Output Current-mA	Hysteresis Capability	Receiver t_{pd}-ns	Driver t_{pd}-ns	Tranceivers per Package	Logic/Connection Diagram	Package(s)
1	**54LS/74LS242**	Quad Inverting 3S	40	40	0.4V	12	12	4	D75	3I,6A,9A
2	**54LS/74LS243**	Quad 3S	40	40	0.4V	12	12	4	D76	3I,6A,9A
3	**54LS[1]/74LS245**	Octal 3S	40	40	0.4V	12	12	8	D79	9Z
4	**100194[1]**	Duplex	—	—	—	2.0	1.1	5	E110	4Q,6Q

DISPLAY DRIVERS

DISPLAY DRIVERS

Item	DEVICE NO.	Function[2]	Input Compatibility	BCD Decoder	Ripple Blanking	Blanking Above BCD 9 Input	Output Current mA	Output Standoff Voltage-V (Max)	Active HIGH/LOW	Display Type	Standby Power Dissipation-mW	Logic/Connection Diagram	Package(s)
5	**4511B**	7-Seg Latch/ Decoder/Dvr	CMOS	Yes	No	Yes	25	—	H	LED	0.015	C111	4L,6B, 9B
6	**4734B**	7-Seg Latch/ Decoder/Dvr	CMOS	Yes	Yes	Yes	25	—	H	LED	0.015	C114	7D,9M
7	**4543B**	7-Seg Latch/ Decoder/Dvr	CMOS	Yes	No	Yes	—	—	H	LCD	0.015	C112	4L,6B, 9B
8	**54/7441**	1-of-10 Cold Cathode	TTL	Yes	No	No	7.0	55	L	Gas Discharge	145	D140	4L,6B, 9B
9	**54/7445**	1-of-10 OC Dvr	TTL	Yes	No	Yes	80	30	L	Common Anode	215	D135	4L,7B, 9B
10	**54/7446**	7-Seg Decoder/Dvr	TTL	Yes	Yes	No	40	30	L	Common Anode	320	D143	4L,7B 9B
11	**54/7447**	7-Seg Decoder/Dvr	TTL	Yes	Yes	No	40	15	L	Common Anode	320	D143	4L,7B, 9B
12	**54LS/ 74LS47**	7-Seg Decoder/Dvr	TTL	Yes	Yes	No	12	15	L	Common Anode	35	D143	4L,6B, 9B
13	**54/7448**	7-Seg Decoder	TTL	Yes	Yes	No	8.0	5.5	H	—	265	D141	4L,7B, 9B

1 To be announced
2 OC = open collector, 3S = 3-state