S3078

DEVICE SPECIFICATION

Multi-Rate Limiting Amplifier and Clock Recovery Unit

Features

- SiGe BiCMOS Technology
- +3.3 V Power Supply
- Integrated Limiting Amplifier
- No Degradation in Jitter Tolerance down to 5 mV Input
- Loss-of-Signal Detection
- Supports Clock Recovery for:
  OC-48 (2488.32 Mbps) with FEC
  OC-24 (1244.16 Mbps) with FEC
  OC-12 (622.08 Mbps) with FEC
  OC-3 (155.52 Mbps) with FEC NRZ data
  Gigabit Ethernet (GBE) (1250 Mbps) with FEC
  Fibre Channel (FC) (1062.5 Mbps) with FEC
  Fibre Channel (FC) (2125 Mbps) with FEC
- Lock Detect monitors frequency of incoming data
- Selectable reference frequencies
  155.52 MHz – 166.62 MHz or
  19.44 MHz – 20.83 MHz
- Typical power 730 mW
- 81 Pin PBGA package and Die

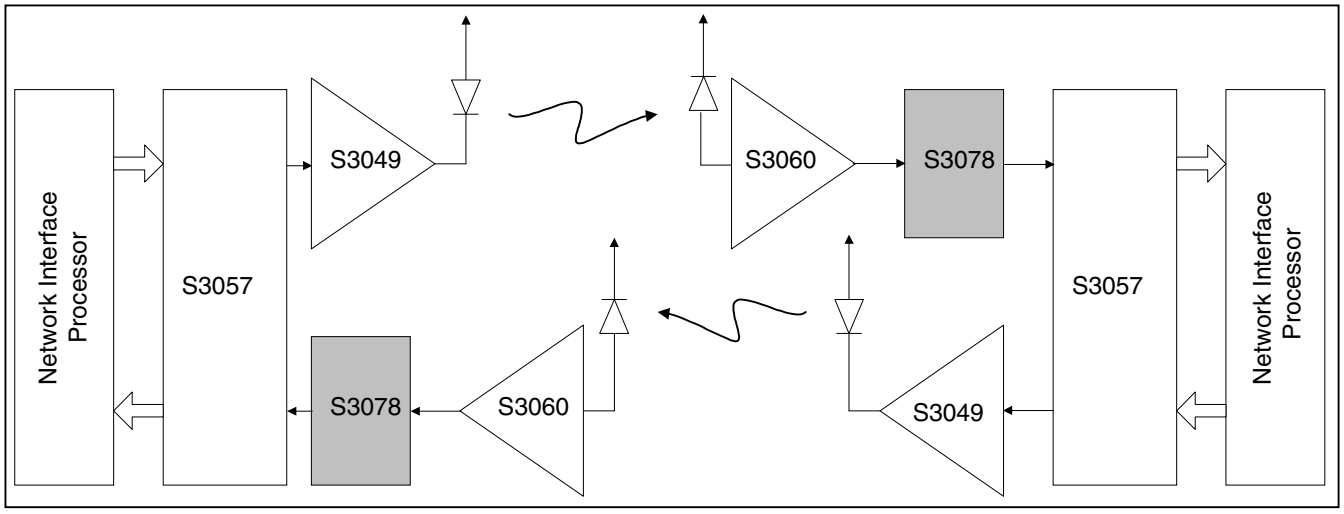
General Description

The S3078 is a 3.3 V combined limiting amplifier and Clock Recovery Unit (CRU) for multi-rate applications. Figure 1 shows a typical network application.

The internal limiting amplifier provides a voltage limited signal into the CRU for inputs down to 5 mV. It has a Loss-of-Signal (LOS) output, which can be programmed to assert with input levels between 25 mVp-p and 60 mVp-p. There is also an offset correction function that reduces pulse-width distortion.

The CRU is implemented using AMCC's proven on-chip Phase Locked Loop (PLL) technology, and it can lock onto OC-48, OC-24, OC-12, GBE, FC, or OC-3 scrambled NRZ signal with FEC capability up to 8 bytes per 255-byte block, and recovers the clock from the data. It consists of a phase detector, a loop filter, and a Voltage Controlled Oscillator (VCO). The phase detector compares the phase relationship between the VCO output and the serial data input. A loop filter converts the phase detector output into a smooth DC voltage, and the DC voltage is input into the VCO whose frequency is varied by this voltage.

Figure 1. System Block Diagram



FUNCTIONAL DESCRIPTION

The block diagram in Figure 2 shows the architecture of the S3078. It has a limiting amplifier integrated with a Clock Recovery Unit (CRU).

Limiting Amplifier

The limiting amplifier at the input of the device quantizes the signal, and outputs a voltage-limited waveform over a 62 dB input dynamic range. It provides 43 dB of linear gain (in three linear gain stages) followed by up to 15 dB of quantized gain (in the digital buffer), before it is presented into the phase detector of the PLL. This allows the device to operate with inputs down to 5 mV, differential, with no degradation in jitter tolerance.

The S3078 provides an input offset correction function that effectively reduces the offset voltage to negligible levels. An external capacitor, CAZ, should be added between CAZ1 and CAZ2 to compensate the offset correction loop.

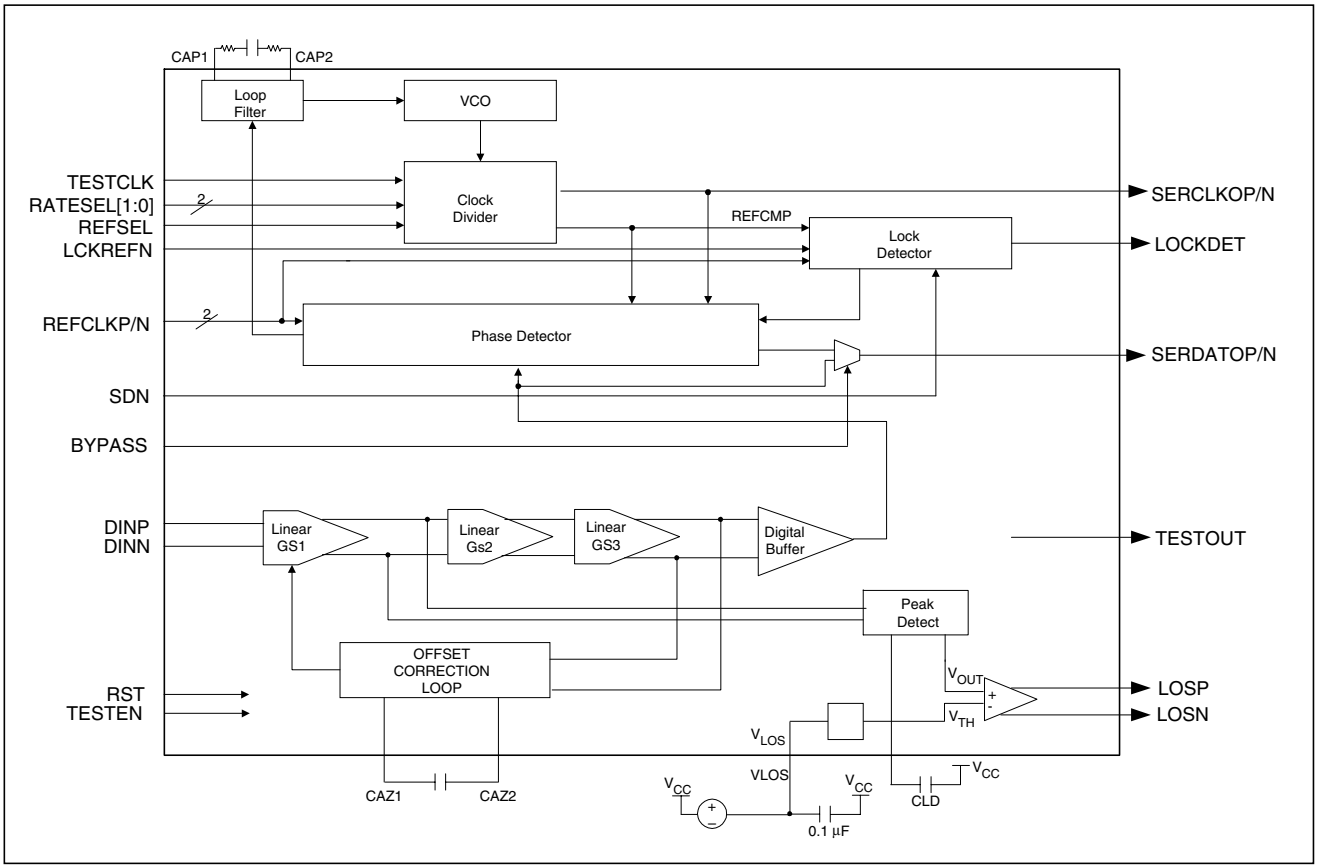
Loss-Of-Signal Function

The limiting amplifier incorporates a chatter-free loss-of-signal function, which is used to detect that the input signal has dropped below the level necessary for acceptable bit error rate performance. The loss-of-signal function is implemented with a rectifying peak detector, which samples the signal at the output of the first gain stage.

The peak detector has a filter to slow its response to the peaks. Nominal response time is 0.01 µs, but this can be increased by adding an external cap, CLD, to V_{CC}.

The output from the peak detector, V_{OUT}, is compared against a threshold level V_{TH}, which is externally controlled by the input voltage V_{LOS}, where V_{LOS} is referred to V_{CC}. LOS is asserted if V_{OUT} falls below V_{TH}. Figure 9 shows the V_{TH} as a function of V_{LOS}. Level-detect hysteresis ensures chatter-free LOS output when the input signal level is close to the LOS threshold. The hysteresis for any programmed loss-of-signal level is nominally 5 dB.

Figure 2. Functional Block Diagram



Clock Recovery Unit

The S3078 supports clock recovery for OC-48, OC-24, Gigabit Ethernet, Fibre Channel, OC-12, and OC-3 data rates with FEC capability up to 8 bytes per 255-byte block.

The clock recovery block generates a clock that is at the same frequency as the incoming data bit rate at the output of the limiting amplifier. The clock is phase aligned by a PLL so that it samples the data in the center of the data eye pattern.

A phase/frequency discriminator compares the phase relationship between the edge transitions of the data and those of the generated clock. Output pulses from the discriminator indicate the required direction of phase corrections. These pulses are smoothed by an integral loop filter. The output of the loop filter controls the frequency of the Voltage Controlled Oscillator (VCO), which generates the recovered clock.

Frequency stability without incoming data is guaranteed by an alternate reference clock input (REFCLK) that the PLL locks onto when data is lost. If the frequency of the incoming signal varies by greater than that stated in Table 5 with respect to REFCLKP/N, the PLL will be declared out of lock, and the PLL will lock to the reference clock. The assertion of SDN will also cause an out of lock condition.

The loop filter transfer function is optimized to enable the PLL to track the jitter, yet tolerate the minimum transition density expected in a received SONET data signal. The total loop dynamics of the clock recovery PLL yield a jitter tolerance which exceeds the minimum tolerance proposed for SONET equipment by the Bellcore TA-NWT-000253 standard, shown in Figure 6.

Lock Detect

The S3078 contains a lock detect circuit which monitors the integrity of the serial data inputs. If the recovered clock frequency deviates from the local reference clock frequency by more than that stated in Table 5, the PLL will be declared out of lock (the LOCKDET output will go inactive) and it will be forced to lock to the local reference clock. This will maintain the correct frequency of the recovered clock output under loss of signal or loss of lock conditions.

The lock detect circuit will poll the input data stream in an attempt to reacquire lock to data. If the recovered clock frequency is determined to be within that stated in Table 5, the PLL will be forced to lock to the data and the LOCKDET output will go active.

The assertion of SDN will also cause an out of lock condition.

Table 1. Pin Assignment and Descriptions

Pin Name	Level	I/O	Pin#	Description
DINP DINN	Analog	I	J4 J3	Positive/Negative data inputs.
CLD	Analog	I	J6	A capacitor to V_{CC} can be added here to set the LOS circuit response time. It can be left open for minimum response time. See Design Procedures to determine the desired capacitance.
VLOS	DC	I	G5	Power Detect/LOS level set. This input is to program the required threshold level for LOS assertion. If left open, the threshold will be set to the minimum level. The value of V_{LOS} can be determined using the plot in Figure 9. This pin should be bypassed to VCC through a 0.1 µF capacitor.
CAZ1 CAZ2	Analog		E1 D1	A 10 nF offset-correction loop compensation capacitor should be connected between these two pins. (See Design Procedures.)
LOSP	LVTTL	O	H7	Loss-of-Signal Detect. This pin is asserted High when the power drops below the LOS threshold, set by V_{LOS}.
LOSN	LVTTL	O	J7	Loss-of-Signal Detect. This pin is asserted Low when the power drops below the LOS threshold, set by V_{LOS}.
BYPASS	LVTTL	I	C3	Bypass. Active High. Used to bypass the PLL. It allows transmission of the data without clock recovery.
SDN	Single-Ended LVPECL	I	B2	Signal Detect. Active Low. A single-ended 10K PECL input to be driven by the external optical receiver module to indicate a loss of received optical power. When SDN is inactive, the input data will be internally forced to a constant zero, and the PLL will be forced to lock to the REFCLK inputs. When SDN is active, data on the DINP/N pins will be processed normally. If not used leave open.
REFCLKP REFCLKN	Internally Biased Diff. LVPECL	I	F9 G9	Reference Clock. 155.52/19.44 MHz input used to establish the initial operating frequency of the clock recovery PLL and also used as a standby clock in the absence of data, during reset or when SDN is inactive.
CAP1 CAP2	Analog		A5 B5	PLL Loop FIlter Capacitor. The loop filter capacitor and resistors are connected to these pins. See Figure 14.
LCKREFN	LVTTL	I	E7	Lock to Reference. Active Low. When active, the serial clock output will be forced to lock to the local reference clock input [REFCLK].
RATESEL0 RATESEL1	LVTTL	I	E6 D6	Rate Select. Selects the operating mode. See Table 16. If left open, they will default to a (Logic “1”) High state.
REFSEL	LVTTL	I	G8	Reference Clock Select. Selects the reference frequency. See Table 17.
SERDATOP SERDATON	Diff. CML	O	C9 D9	Serial Data Out. This signal is the data output updated on the falling edge of Serial Clock Out (SERCLKOP).
SERCLKOP SERCLKON	Diff. CML	O	A8 A9	Serial Clock Out. This signal is phase aligned with Serial Data Out (SERDATOP/N). See Figure 8.

Table 1. Pin Assignment and Descriptions (Continued)

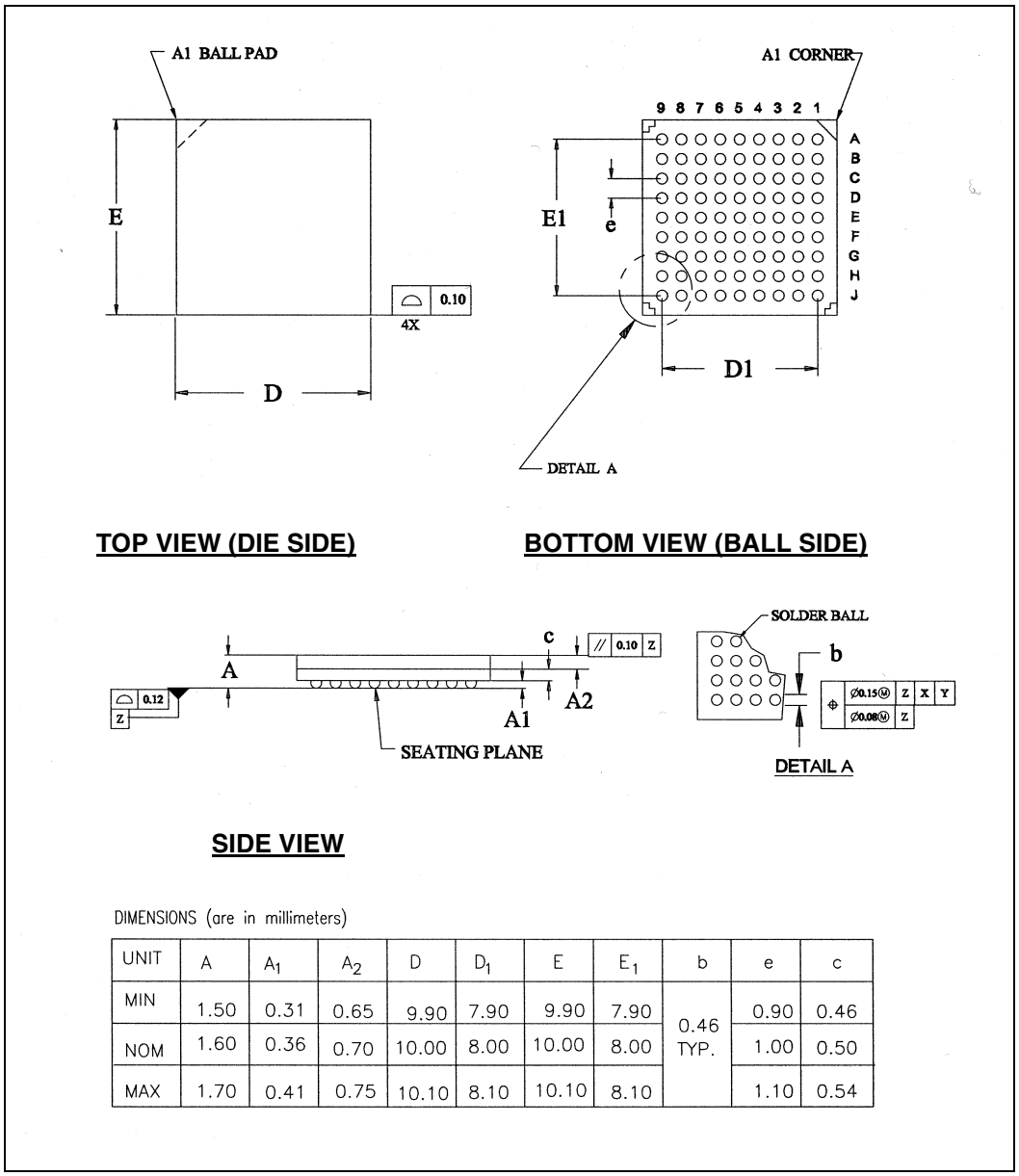
Pin Name	Level	I/O	Pin#	Description
LOCKDET	LVTTL	O	H8	Lock Detect. Clock recovery indicator. When high, the internal clock recovery unit has locked onto the incoming data stream. LOCKDET is an asynchronous output.
TESTEN	LVTTL	I	B3	Test Enable. Active High input used for production test. This pin should be grounded for normal operation.
TESTCLK	LVTTL	I	H9	Test clock. Used for production test. This pin should be grounded for normal operation.
RST	LVTTL	I	F8	Reset. Active High input used for production test. This pin should be grounded for normal operation.
TESTOUT	LVPECL	O	E8	Test Output. Leave open for normal operation.
VCC1	Power		A1, B1	LA (Limiting Amplifier) supply #1
VEE1	Ground		C2	LA (Limiting Amplifier) ground #1
VCC2	Power		C1	LA (Limiting Amplifier) supply #2
VEE2	Ground		D2	LA (Limiting Amplifier) ground #2
VCC3	Power		H6	LA (Limiting Amplifier) supply #3
VEE3	Ground		G6	LA (Limiting Amplifier) ground #3
VCC4	Power		F1	LA (Limiting Amplifier) supply #4
VEE4	Ground		F2, G1	LA (Limiting Amplifier) ground #4
VCC5	Power		H1, H2, J1	LA (Limiting Amplifier) supply #5
VEE5	Ground		G3, G4, H3, H4, H5, J2, J5	LA (Limiting Amplifier) ground #5
VEEX	Ground		C4, C5, C6, D3, D4, E3, E4, F3, F4	Ground
VCC7	Power		A2	CRU digital supply #1
VEE7	Ground		A3	CRU digital ground #1
VCC8	Power		E9	CRU digital supply #2
VEEG	Ground		D5, E5, F5	CRU digital ground #2
VCC9	Power		J9	CRU low speed digital circuit supply
VCC10	Power		A4	CRU Analog supply #1
VEE10	Ground		B4	CRU Analog ground #1
VCC11	Power		A6	CRU Analog supply #2
VEE11	Ground		B6	CRU Analog ground #2
VCC13	Power		C8	Data output buffer supply
VEE13	Ground		C7	Data output buffer ground
VCC14	Power		B7, B8	Clock output buffer supply

Table 1. Pin Assignment and Descriptions (Continued)

Pin Name	Level	I/O	Pin#	Description
VEE14	Ground		A7	Clock output buffer supply
VCC15	Power		D7	Low speed digital output buffer supply
VEEX3	Ground		E2	Ground
VEE17	Ground		D8	Data output buffer ground
VEE18	Ground		B9	Clock output buffer ground
VEEX4	Ground		G2	Ground
VSSX	Ground		F6	Shield ground
VSUB	Ground		G7	Substrate ground
VDD	Power		J8	Digital supply
VSS	Ground		F7	Digital ground

Note: Power is 3.3 V.

Figure 3. 81 PBGA Package



DIMENSIONS (are in millimeters)

UNIT	A	A_1	A_2	D	D_1	E	E_1	b	e	c
MIN	1.50	0.31	0.65	9.90	7.90	9.90	7.90	0.46 TYP.	0.90	0.46
NOM	1.60	0.36	0.70	10.00	8.00	10.00	8.00		1.00	0.50
MAX	1.70	0.41	0.75	10.10	8.10	10.10	8.10		1.10	0.54

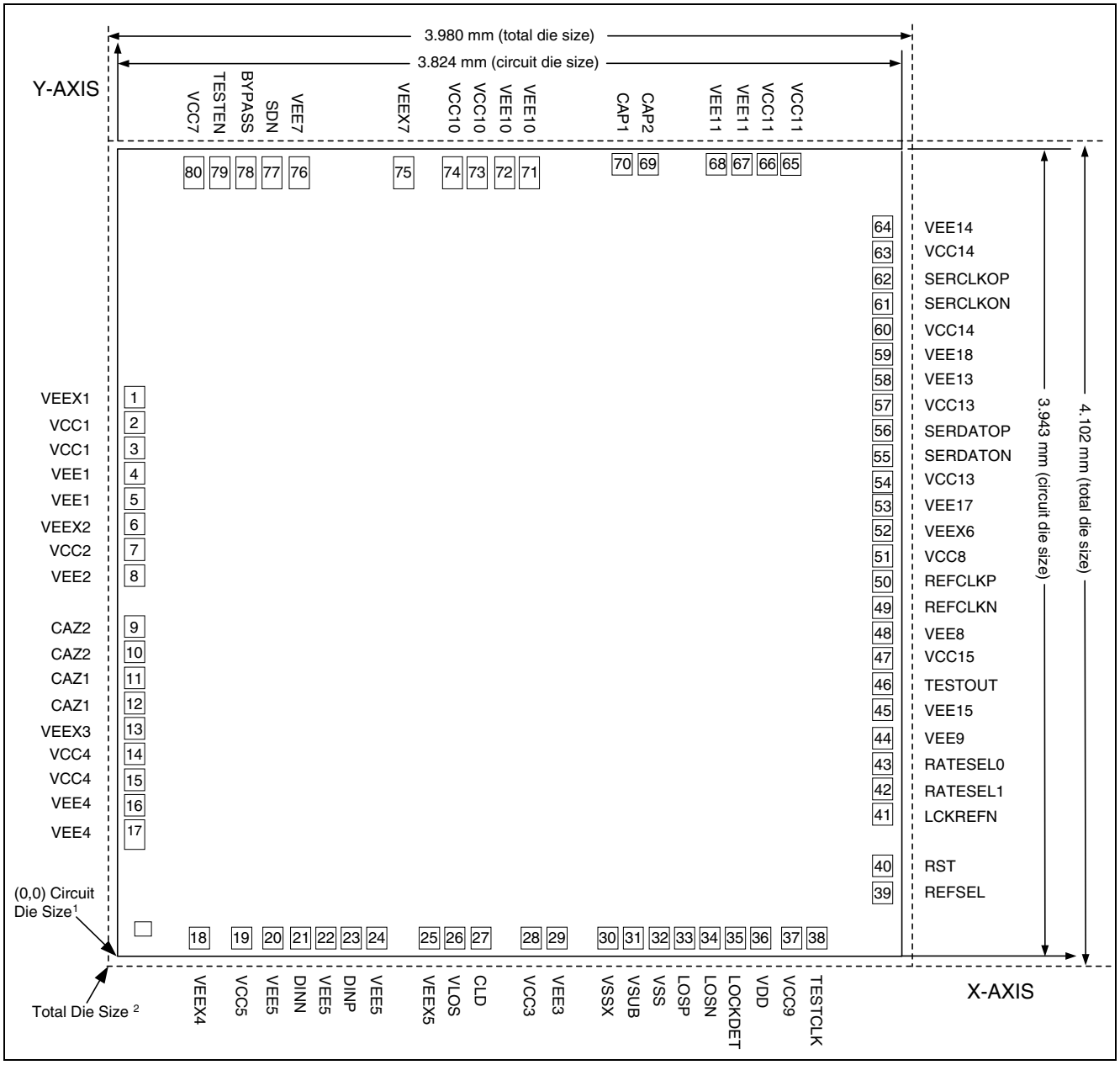
Thermal Management

Device	Max Package Power	Θja
S3078	0.988 W	37.0°C/W

Figure 4. S3078 81 Pin PBGA-Top View

	J	H	G	F	E	D	C	B	A
1	VCC5	VCC5	VEE4	VCC4	CAZ1	CAZ2	VCC2	VCC1	VCC1
2	VEE5	VCC5	VEEX4	VEE4	VEEX3	VEE2	VEE1	SDN	VCC7
3	DINN	VEE5	VEE5	VEEX	VEEX	VEEX	BYPASS	TESTEN	VEE7
4	DINP	VEE5	VEE5	VEEX	VEEX	VEEX	VEEX	VEE10	VCC10
5	VEE5	VEE5	VLOS	VEEG	VEEG	VEEG	VEEX	CAP2	CAP1
6	CLD	VCC3	VEE3	VSSX	RATE SEL0	RATE SEL1	VEEX	VEE11	VCC11
7	LOSN	LOSP	VSUB	VSS	LCK REFN	VCC15	VEE13	VCC14	VEE14
8	VDD	LOCK DET	REFSEL	RST	TEST OUT	VEE17	VCC13	VCC14	SERCLK OP
9	VCC9	TEST CLK	REF CLKN	REF CLKP	VCC8	SERDAT ON	SERDAT OP	VEE18	SERCLK ON

Figure 5. S3078 Bonding Pad Location



1. The circuit die size is the smallest possible size of the die. The lower left hand corner of the circuit die is the origin of the xy-coordinate system. Pad coordinates indicated in Table 2 are measured from this origin to the pad's center.
2. The total die size is the largest possible size of the die. It includes a splicing area around the circuit die. The actual size of any given die may vary in size from the minimum (circuit die) size to the maximum (total die) size.

Table 2. Pad Assignment and Descriptions

Pin Name	Level	I/O	Pad#	Coordinates [X,Y][1]	Description
DINP DINN	Analog	I	23 21	1186.900, 72.425 976.900, 72.425	Positive/Negative data Inputs.
CLD	Analog	I	27	1816.900, 72.425	A capacitor to V_{CC} can be added here to set the LOS circuit response time. It can be left open for minimum response time. See Design Procedures to determine the desired capacitance.
VLOS	DC	I	26	1711.900, 72.425	Power Detect/LOS level set. This input is to program the required threshold level for LOS assertion. If left open, the threshold will be set to the minimum level. The value of V_{LOS} can be determined using the plot in Figure 9. This pad should be bypassed to VCC through a 0.1 µF capacitor.
CAZ1 CAZ2	Analog		11 12 9 10	72.425, 1401.900 72.425, 1296.900 72.425, 1611.900 72.425, 1506.900	A 10 nF offset-correction loop compensation capacitor should be connected between these two pins. (See Design Procedures.)
LOSP	LVTTL	O	33	2775.900, 72.425	Loss-of-Signal Detect. This pin is asserted High when the power drops below the LOS threshold, set by V_{LOS}.
LOSN	LVTTL	O	34	2880.900, 72.425	Loss-of-Signal Detect. This pin is asserted Low when the power drops below the LOS threshold, set by V_{LOS}.
BYPASS	LVTTL	I	78	861.900, 3871.375	Bypass. Active High. Used to bypass the PLL. It allows transmission of the data without clock recovery.
SDN	Single-Ended LVPECL	I	77	966.900, 3871.375	Signal Detect. Active Low. A single-ended 10K PECL input to be driven by the external optical receiver module to indicate a loss of received optical power. When SDN is inactive, the input data will be internally forced to a constant zero, and the PLL will be forced to lock to the REFCLK inputs. When SDN is active, data on the DINP/N pins will be processed normally. If not used leave open.
REFCLKP REFCLKN	Internally Biased Diff. LVPECL	I	50 49	3751.375, 1782.900 3751.375, 1677.900	Reference Clock. 155.52/19.44 MHz input used to establish the initial operating frequency of the clock recovery PLL and also used as a standby clock in the absence of data, during reset or when SDN is inactive.
CAP1 CAP2	Analog		70 69	2541.900, 3871.375 2436.900, 3871.375	PLL Loop FIlter Capacitor. The loop filter capacitor and resistors are connected to these pins. See Figure 14.
LCKREFN	LVTTL	I	41	3751.375, 725.900	Lock to Reference. Active Low. When active, the serial clock output will be forced to lock to the local reference clock input [REFCLK].

Table 2. Pad Assignment and Descriptions (Continued)

Pin Name	Level	I/O	Pad#	Coordinates [X,Y][1]	Description
RATESEL0 RATESEL1	LVTTL	I	43 42	3751.375, 935.900 3751.375, 830.900	Rate Select. Selects the operating mode. See Table 16. If left open, they will default to a (Logic “1”) High state.
REFSEL	LVTTL	I	39	3751.375, 478.900	Reference Clock Select. Selects the reference frequency. See Table 17.
SERDATOP SERDATON	Diff. CML	O	56 55	3751.375, 2439.400 3751.375, 2334.400	Serial Data Out. This signal is the data output updated on the falling edge of Serial Clock Out (SERCLKOP).
SERCLKOP SERCLKON	Diff. CML	O	62 61	3751.375, 3081.900 3751.375, 2976.900	Serial Clock Out. This signal is phase aligned with Serial Data Out (SERDATOP/N). See Figure 8.
LOCKDET	LVTTL	O	35	2985.900, 72.425	Lock Detect. Clock recovery indicator. When high, the internal clock recovery unit has locked onto the incoming data stream. LOCKDET is an asynchronous output.
TESTEN	LVTTL	I	79	756.900, 3871.375	Test Enable. Active High input used for production test. It should be grounded for normal operation.
TESTCLK	LVTTL	I	38	3344.900, 72.425	Test clock. Used for production test. It should be grounded for normal operation.
RST	LVTTL	I	40	3751.375, 620.900	Reset. Active High input used for production test. It should be grounded for normal operation.
TESTOUT	LVPECL	O	46	3751.375, 1355.900	Test Output. Leave open for normal operation.
VCC1	Power		2 3	72.425, 2451.900 72.425, 2346.900	LA (Limiting Amplifier) supply #1
VEE1	Ground		4 5	72.425, 2241.900 72.425, 2136.900	LA (Limiting Amplifier) ground #1
VCC2	Power		7	72.425, 1926.900	LA (Limiting Amplifier) supply #2
VEE2	Ground		8	72.425, 1821.900	LA (Limiting Amplifier) ground #2
VCC3	Power		28	2026.900, 72.425	LA (Limiting Amplifier) supply #3
VEE3	Ground		29	2131.900, 72.425	LA (Limiting Amplifier) ground #3
VCC4	Power		14 15	72.425, 1086.900 72.425, 981.900	LA (Limiting Amplifier) supply #4
VEE4	Ground		16 17	72.425, 876.900 72.425, 771.900	LA (Limiting Amplifier) ground #4
VCC5	Power		19	766.900, 72.425	LA (Limiting Amplifier) supply #5
VEE5	Ground		20 22 24	871.900, 72.425 1081.900, 72.425 1291.900, 72.425	LA (Limiting Amplifier) ground #5
VEEX1	Ground		1	72.425, 2556.900	Ground
VCC7	Power		80	651.900, 3871.375	CRU digital supply #1
VEE7	Ground		76	1071.900, 3871.375	CRU digital ground #1

Table 2. Pad Assignment and Descriptions (Continued)

Pin Name	Level	I/O	Pad#	Coordinates [X,Y][1]	Description
VCC8	Power		51	3751.375, 1887.900	CRU digital supply #2
VEE8	Ground		48	3751.375, 1572.900	CRU digital ground #2
VCC9	Power		37	3202.900, 72.425	CRU low speed digital circuitry supply
VEE9	Ground		44	3751.375, 1040.900	CRU low speed digital circuitry ground
VCC10	Power		73 74	1701.900, 3871.375 1596.900, 3871.375	CRU analog supply #1
VEE10	Ground		71 72	1911.900, 3871.375 1806.900, 3871.375	CRU analog ground #1
VCC11	Power		65 66	3171.900, 3871.375 3066.900, 3871.375	CRU analog supply #2
VEE11	Ground		67 68	2961.900, 3871.375	CRU analog ground #2
VEEX2	Ground		6	72.425, 2031.9	Ground
VCC13	Power		54 57	3751.375, 2229.400 3751.375, 2544.400	Data output buffer supply
VEE13	Ground		58	3751.375, 2649.400	Data output buffer ground
VCC14	Power		60 63	3751.375, 2871.900 3751.375, 3186.900	Clock output buffer supply
VEE14	Ground		64	3751.375, 3291.900	Clock output buffer supply
VCC15	Power		47	3751.375, 1460.900	Low speed digital output buffer supply
VEE15	Ground		45	3751.375, 1250.900	Low speed digital output buffer ground
VEEX3	Ground		13	72.425, 1191.900	Ground
VEE17	Ground		53	3751.375, 2124.400	Data output buffer ground
VEE18	Ground		59	3751.375, 2766.900	Clock output buffer ground
VEEX4	Ground		18	556.900, 72.425	Ground
VEEX5	Ground		25	1501.900, 72.425	Ground
VEEX7	Ground		75	1386.900, 3871.375	Ground
VEEX6	Ground		52	3751.375, 1999.900	Ground
VSSX	Ground		30	2446.900, 72.425	Shield ground
VSUB	Ground		31	2558.900, 72.425	Substrate ground
VDD	Power		36	3090.900, 72.425	Digital supply
VSS	Ground		32	2670.900, 72.425	Digital ground

1. The coordinates represent the center of the pad in µm, with respect to the lower left corner of the circuit die. Power is 3.3 V.
2. Pad size is 80 µm x 80 µm.

Table 3. DINP/N AC and DC Electrical Characteristics

Parameter	Description	Min	Typ	Max	Units	Conditions
V_{ID}	Input Voltage Range	5		1200	mV	Input is 1240 MHz sine wave, 1mV peak to peak differential
V_n [1]	Differential Input Noise			200 4.47	µV nv/Hz	Input referred noise = RMS output noise/low-frequency gain 7 kHz - 2 GHz
V_{DIN}	Input Common Mode Bias Voltage		2.1		V	

1. This parameter cannot be measured directly.

Table 4. LOS (Loss-of-Signal) Electrical Characteristics

Parameter	Description	Min	Typ	Max	Units	Conditions
t_{OFFL}	LOS Release time (DIN to internal signal detect), minimum input.	0.01			µs	V_{ID} = 6mV Data Pattern=2^7-1 PRBS CLD pin open
t_{ONL}	LOS Assert Time (DIN to internal signal loss detect)	0.01			µs	V_{ID} = 6mV_{p-p} Data Pattern=2^7-1 PRBS CLD pin open
R_{VLOS}	VLOS Input Resistance		1		kΩ	To V_{CC}
V_{TH}	LOS Assert Threshold	25		60	mV	Peak to peak differential Data pattern = 2^7-1 PRBS
HYS	LOS Hysteresis	2		8	dB	Electrical power Data pattern=2^7-1 PRBS

Table 5. CRU Performance Specifications

Parameter	Min	Typ	Max	Units	Conditions
Nominal VCO Center Frequency	2.488	2.579	2.67	GHz	
Data Output Jitter with VCO locked to DINP/N STS-48			0.006	UI (rms)	With no jitter on serial data inputs.
Reference Clock Frequency Tolerance	-100		+100	ppm	
Acquisition Lock Time 19.44 MHz Ref Clock 155.52 MHz Ref Clock			 1800 250	 µsec µsec	Minimum transition density of 20%. With device already powered up and valid ref clock.
Reference Clock Input Duty Cycle	40		60	% of UI	
Reference Clock Rise and Fall Times			1.5	ns	20% to 80% of amplitude at 155.52 Mhz.
CML Output Rise and Fall Times		60	110	ps	20% to 80%, 50Ω load, 1 pF cap.
Frequency difference at which out of lock is declared (REFCLK compared to the divided down VCO clock)	450	600	770	ppm	
Frequency difference at which receive PLL is declared in lock (REFCLK compared to the divided down VCO clock)	220	300	390	ppm	
t_{SU} OC-48/Fibre Channel (2125 Mbps) OC-24/GBE/Fibre Channel (1062.5 Mbps) OC-12 OC-3	 100 250 500 2500			ps	See Figure 8.
t_H OC-48/Fibre Channel (2125 Mbps) OC-24/GBE/Fibre Channel (1062.5 Mbps) OC-12 OC-3	 100 250 500 2500			ps	See Figure 8.

Table 6. Fibre Channel Jitter Generation Specification

Parameter	Min	Typ	Max	Units	Condition
Deterministic Jitter (DJ)			0.08	UI (p-p)	
Total Jitter (TJ)			0.28	UI (p-p)	

Table 7. Jitter Tolerance Specification (See Figure 6)

Parameter	Min	Typ	Max	Units	Condition
Jitter Tolerance STS-48	0.4	0.5		UI	1 MHz < F < 5 MHz Data Pattern = 2^7-1 PRBS
Jitter Tolerance STS-24					
Jitter Tolerance STS-12	0.4	0.6		UI	250 kHz < F < 5 MHz Data Pattern = 2^7-1 PRBS
Jitter Tolerance STS-3	0.4	0.8		UI	65 kHz < F < 1.3 MHz Data Pattern = 2^7-1 PRBS
GBE T_J, Total Input Jitter Tolerance	599			ps	As specified in IEEE 802.3z
GBE T_{DJ}, Deterministic Input Jitter Tolerance	370			ps	As specified in IEEE 802.3z
Fibre Channel Frequency Dependent Jitter Tolerance t_{FDJ}.	0.10			UI (p-p)	637 kHz to ≥ 5 MHz.
Fibre Channel Deterministic Jitter Tolerance $t_{DJ.}$	0.38			UI (p-p)	637 kHz to – 531 MHz.
Fibre Channel Random Jitter $t_{RJ.}$	0.22			UI (p-p)	637 kHz to – 531 MHz.
Fibre Channel Total Jitter $t_{TJ.}$	0.70			UI (p-p)	

1. Not tested.

Table 8. Jitter Transfer Specification (See Figure 7)

Parameter	f_C	P	Condition
OC-48	2000 kHz	0.1 dB	Input sinusoidal jitter up to the mask level in Figure 6.
OC-12	500 kHz	0.1 dB	Input sinusoidal jitter up to the mask level in Figure 6.
OC-3	130 kHz	0.1 dB	Input sinusoidal jitter up to the mask level in Figure 6.

CRU JITTER CHARACTERISTICS

The PLL complies with the jitter specifications proposed for Fibre Channel equipment defined by the Fibre Channel methodology for Jitter Specification, and SONET/SDH equipment defined by the Bellcore Specifications: GR-253-CORE, Issue 2, December 1995 and ITU-T Recommendations: G.958 document, when used with differential inputs and outputs.

Input Jitter Tolerance

Input jitter tolerance is defined as the peak to peak amplitude of sinusoidal jitter applied on the input signal that causes an equivalent 1 dB optical/electrical power penalty. SONET input jitter tolerance requirements are shown in Figure 6. The input Jitter Tolerance requirements are shown in Table 7.

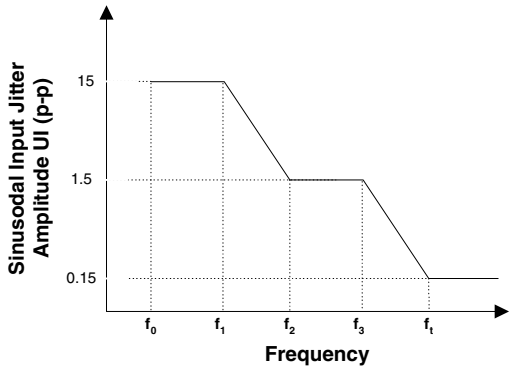
Jitter Transfer

The jitter transfer function is defined as the ratio of jitter on the output OC-N/STS-N signal to the jitter applied on the input OC-N/STS-N signal versus frequency. Jitter transfer requirements are shown in Figure 7. The measurement condition is that input sinusoidal jitter up to the mask level in Figure 6 be applied.

Jitter Generation

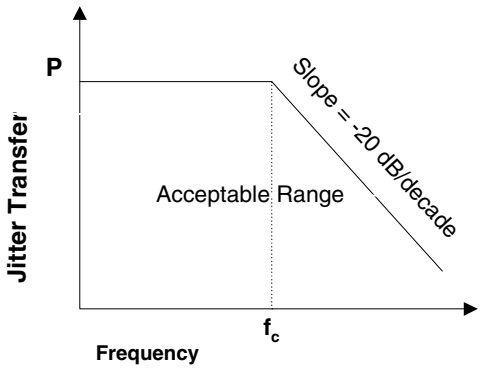
The jitter generation of the serial clock and serial data outputs shall not exceed the values specified in Table 6 for Fibre Channel and 0.01 UI rms for SONET when a serial data input with no jitter is presented to the serial data inputs.

Figure 6. Input Jitter Tolerance Specification



OC/STS Level [1,2]	f_0 (Hz)	f_1 (Hz)	f_2 (Hz)	f_3 (kHz)	f_t (kHz)
48	10	600	6000	100	1000
24[3]					
12	10	30	300	25	250
3	10	30	300	6.5	65

Figure 7. Jitter Transfer Specification



OC/STS Level [1,2]	f_c (kHz)	P (dB)
48	2000	0.1
24[3]		
12	500	0.1
3	130	0.1

1. Bellcore Specifications: GR-253-CORE, Issue 2, December 1995.
2. ITU-T Recommendations: G.958.
3. Not Specified in GR-253 or G.958

The following are the absolute maximum stress ratings for the S3078 device. Stresses beyond those listed may cause permanent damage to the device. Absolute maximum ratings are stress ratings only and operation of the device at the maximums stated or any other conditions beyond those indicated in the “Recommended Operating Conditions” of the document are not inferred. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 9. Recommended Operating Conditions

Parameter	Min	Typ	Max	Units
Ambient Temperature Under Bias	-40		+85	°C
Voltage on V_{CC} with Respect to VEE	3.13	3.3	3.465	V
Voltage on any LVTTL Pin	0.0		3.465	V
Voltage on any LVPECL Pin	0		3.465	V
I_{CC} Supply Current Outputs Open		220	285	mA

Note: Die tested at only 25 ºC.

Table 10. Absolute Maximum Ratings

Parameter	Min	Typ	Max	Units
Storage Temperature Range	-55		+150	°C
Voltage on V_{CC} with Respect to VEE	-0.5		4.0	V
Voltage on DINP, DINN	-0.5		V_{CC}	V
Voltage on CAZ1, CAZ2, V_{LOS}, LOS, V_{OFFSET}	-0.5		V_{CC}	V
Voltage on any LVTTL Input Pin	-0.5		3.465	V
Voltage on any LVPECL Input Pin	0		V_{CC}	V

Electrostatic Discharge (ESD) Ratings

The S3078 is rated to the following voltages based on the human body model.

1. All pins/pads are rated at or above 100 V.

Adherence to standards for ESD protection should be taken during the handling of the devices to ensure that the devices are not damaged. The standards to be used are defined in ANSI standard ANSI/ESD S20.20-1999, “Protection of Electrical and Electronic Parts, Assemblies and Equipment.” Contact your local FAE or Sales representative for applicable ESD application notes.

Table 11. Internally Biased LVPECL Input Characteristics (AC and DC) (REFCLKP/N)

Parameters	Description	Min	Typ	Max	Units	Conditions
ΔV_{INDIFF}	Differential Input Voltage Swing	300		1200	mV	
$\Delta V_{INSINGLE}$	Single-Ended Input Voltage Swing	150		600	mV	
Rin	Differential Input Resistance	80		120	Ω	
V_{IL}	Input Low Voltage	V_{CC} -2.00		V_{CC} -1.4	V	
V_{IH}	Input High Voltage	V_{CC} -1.2		V_{CC} -0.5	V	
I_{IL}	Input Low Current	-300			µA	$V_{IL} = V_{CC}$ - 2 V
I_{IH}	Input High Current	-50		100	µA	$V_{IH} = V_{CC}$ - 0.5 V

Table 12. Single-Ended LVPECL Input DC Characteristics (SDN)

Parameters	Description	Min	Typ	Max	Units	Conditions
V_{IL}	Input Low Voltage	V_{CC} - 2.00		V_{CC} - 1.4	V	
V_{IH}	Input High Voltage	V_{CC} - 1.2		V_{CC} - 0.5	V	
I_{IL}	Input Low Current	-100			µA	$V_{IL} = V_{CC}$ - 2 V
I_{IH}	Input High Current	50		350	µA	$V_{IH} = V_{CC}$ - 0.5 V

Table 13. CML Output Characteristics (AC and DC) (SERDATOP/N, SERCLKOP/N)

Parameters	Description	Min	Typ	Max	Units	Conditions
V_{OL}	CML Output Low Voltage	V_{CC} - 1.5		V_{CC} - 0.65	V	100 Ω line-to-line.
V_{OH}	CML Output High Voltage	V_{CC} - 0.5		V_{CC} - 0.2	V	100 Ω line-to-line.
$\Delta V_{OUTDIFF}$	CML Serial Output Differential Voltage Swing	800		1800	mV	100 Ω line-to-line.
$\Delta V_{OUTSINGLE}$	CML Serial Output Single-Ended Voltage Swing	400		900	mV	100 Ω line-to-line.

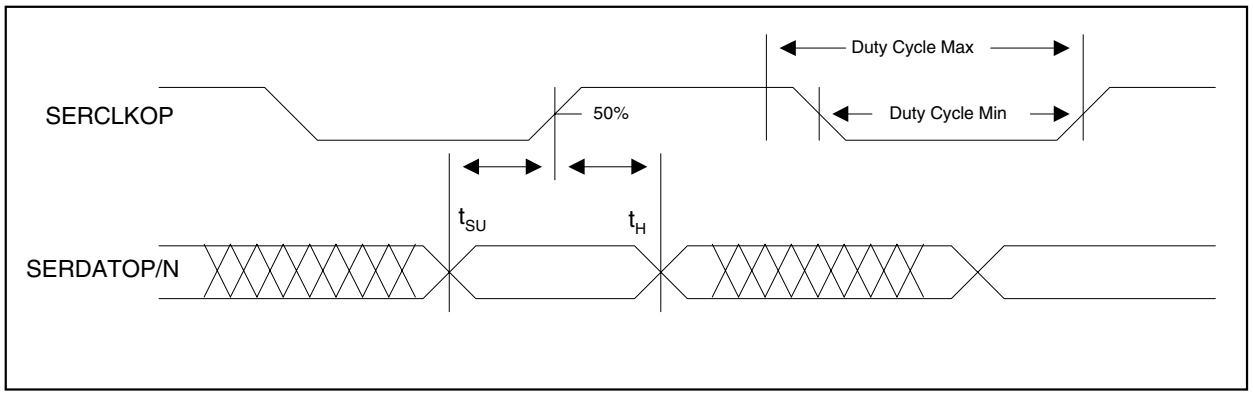
Table 14. LVTTL Input DC Characteristics

Parameters	Description	Min	Typ	Max	Units	Conditions
V_{IL}	Input Low Voltage	0		0.8	V	V_{CC} = Max
V_{IH}	Input High Voltage	2.0		3.47	V	V_{CC} = Max
I_{IL}	Input Low Current	-500			µA	V_{IN} = 0.5V
I_{IH}	Input High Current			50	µA	V_{IN} = 2.4V

Table 15. LVTTL Output DC Characteristics

Parameters	Description	Min	Typ	Max	Units	Conditions
V_{OL}	Output Low Voltage			0.5	V	I_{OL} = 1 mA
V_{OH}	Output High Voltage	2.4			V	I_{OH} = -0.1 mA

Figure 8. Output Timing Diagram



Design Procedures

Determining C_{AZ} and C_{LD}

The values for C_{AZ} and C_{LD} can be selected using the following formulas:

C_{AZ} (µF) = 0.7/BW_L (kHz)
where BW_L is the Low frequency cutoff.

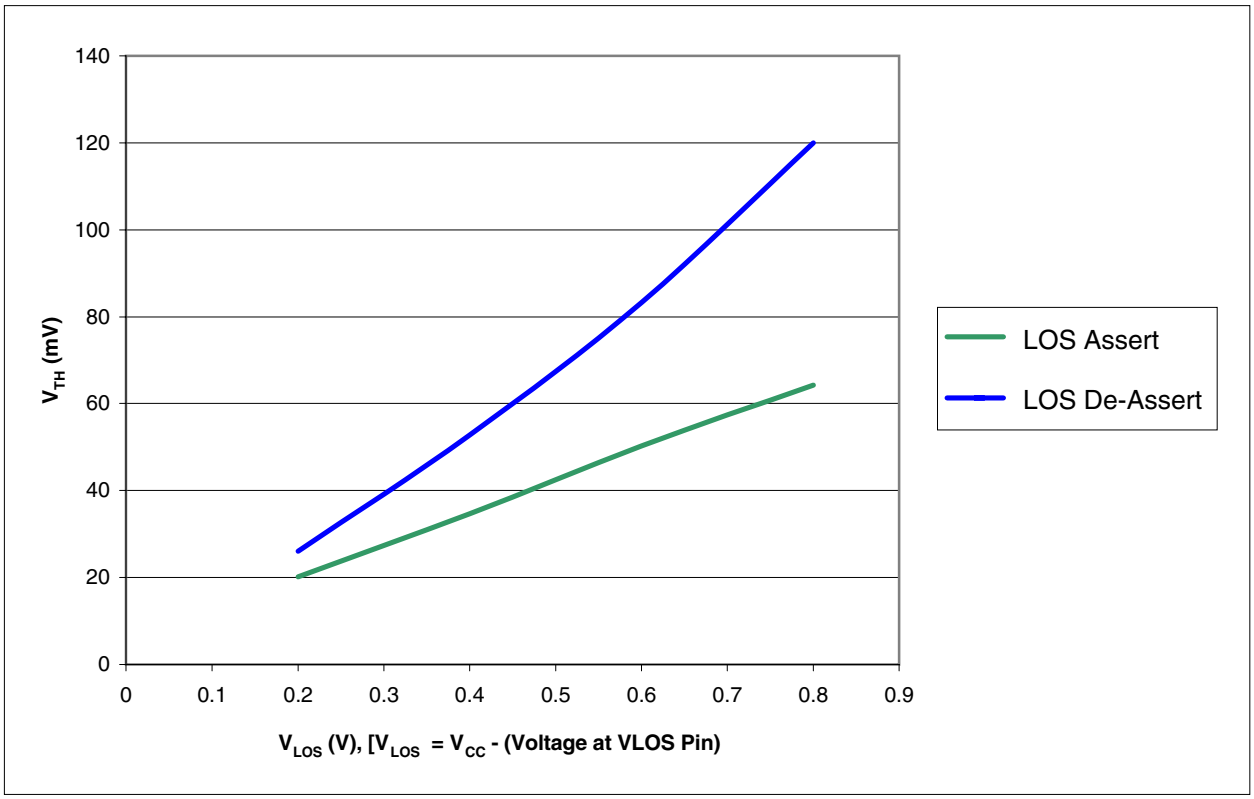
C_{LD} (pF) = (t (µs) x 1250) - 12.5
where t is the LOS response time.

Determining V_{LOS}

Figure 9 is the plot of the LOS threshold, V_{TH}, vs. voltage with respect to V_{CC}, V_{LOS}, at the VLOS pin.

V_{LOS} = Vcc -(Voltage at VLOS pin)

Figure 9. V_{TH} (LOS Assert Threshold) vs. V_{LOS} Setting (Typical)



Selecting Data Rate and Reference Frequency

Table 16. Data Rate Select

RATESEL0	RATESEL1	Operating Mode	Data Rate/Mbps	REFCLK Frequency/ MHz
0	0	OC-3	155.52	155.52/19.44
0	1	OC-12	622.08	155.52/1944
1	0	OC-24	1244.16	155.52/19.44
1	0	GBE	1250	156.25/19.53
1	1	OC-48	2488.32	155.52/19.44
1	0	FC	1062.5	132.81/16.60
1	1	FC	2125	132.81/16.60

Table 17. Reference Frequency Select

REFSEL	Reference Frequency for Data Rates with FEC Capability of X Bytes per 255-Byte Block (For OC-3/12/24/48 Rates only)						
	X = 0	X = 3	X = 4	X = 5	X = 6	X = 7	X = 8
0	19.44 MHz	19.99 MHz	20.15 MHz	20.31 MHz	20.48 MHz	20.65 MHz	20.83 MHz
1	155.52 MHz	159.91 MHz	161.21 MHz	162.53 MHz	163.87 MHz	165.26 MHz	166.63 MHz

Application Information

Figure 10. Connecting to DINP/DINN Inputs of the S3078

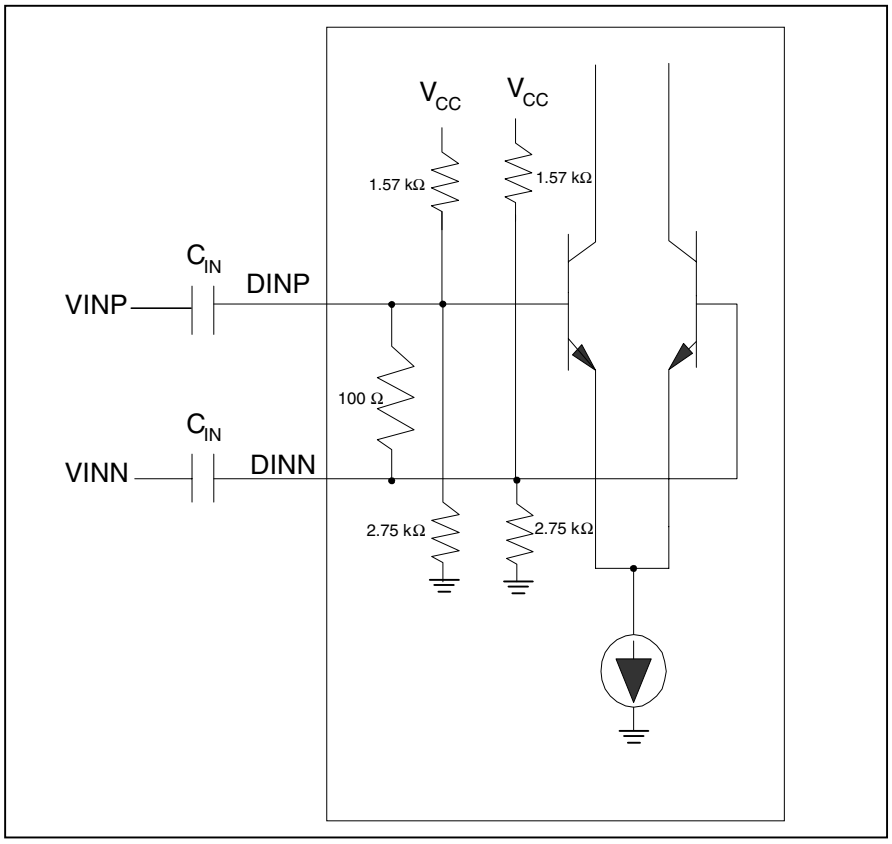


Figure 11. S3078 Differential CML Output to S3057/S3067 Terminations

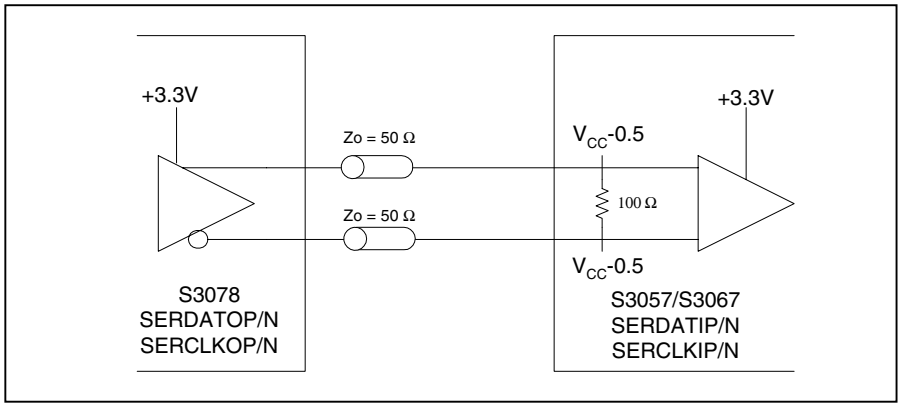


Figure 12. +5 V Differential PECL Driver to S3078 Reference Clock Input AC Coupled Termination

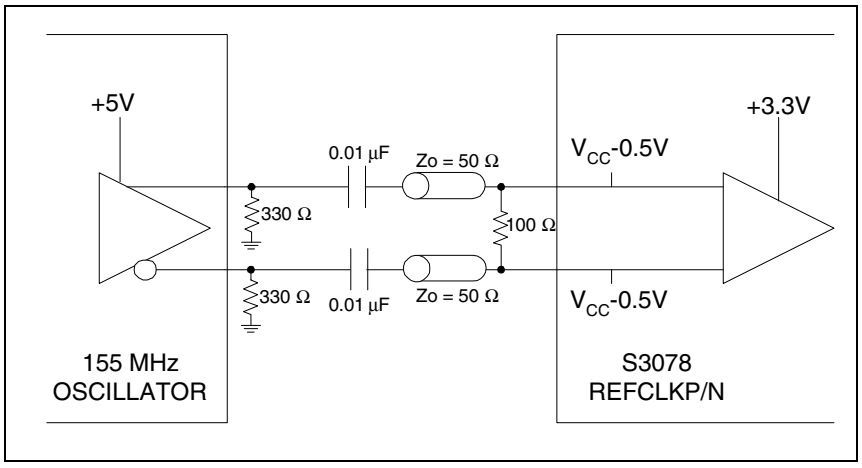


Figure 13. +3.3V Differential LVPECL Driver to S3078 Reference Clock Input DC Coupled Termination

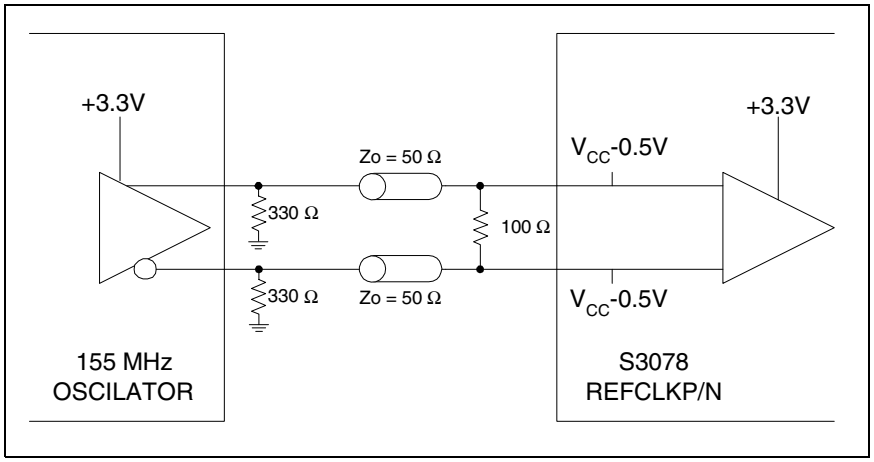
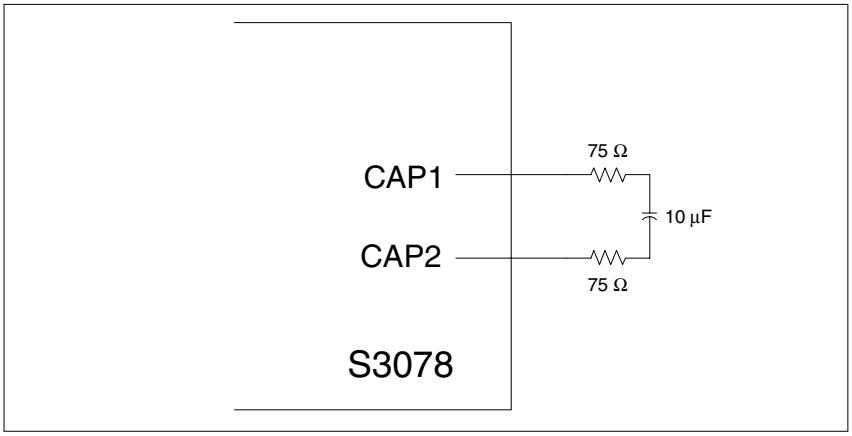
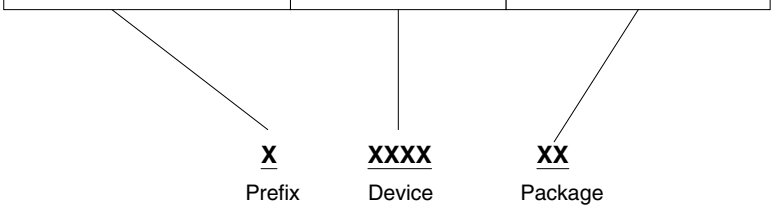


Figure 14. Loop Filter Capacitor Connections



Ordering Information

Prefix	Device	Package
S – Integrated Circuit	3078	PB - 81 PBGA DI - DIE



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