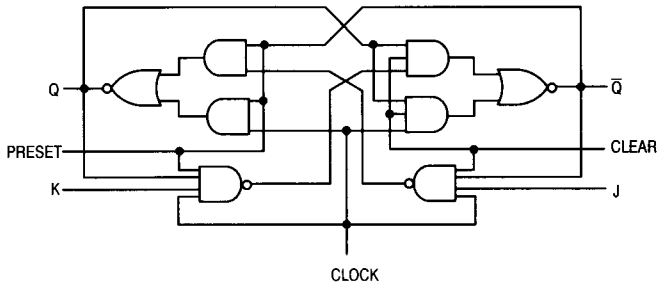
MOTOROLA

Dual J-K Flip-Flop With Clear and Preset

ELECTRICALLY TESTED PER:
MIL-M-38510/30103

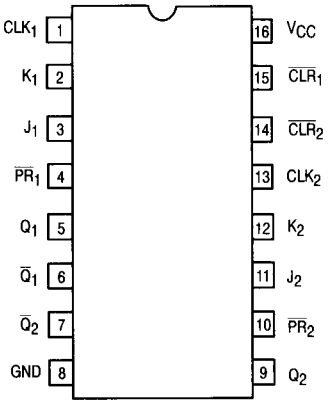
The 54LS112A dual flip-flop features individual J, K, clock, and asynchronous set and clear inputs to each flip-flop. When the clock goes HIGH, the inputs are enabled and data will be accepted. The logic level of the J and K inputs may be allowed to change when the clock pulse is HIGH and the bistable will perform according to the truth table as long as minimum set-up and hold time are observed. Input data is transferred to the outputs on the negative-going edge of the clock pulse.

LOGIC DIAGRAM (one half shown)

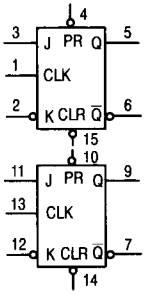


Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

CONNECTION DIAGRAM



LOGIC SYMBOL



Military 54LS112A

AVAILABLE AS:

1) JAN: JM38510/30103BXA
2) SMD: N/A
3) 883: 54LS112A/BXAJC

X = CASE OUTLINE AS FOLLOWS:
PACKAGE: CERDIP: E
CERFLAT: F
LCC: 2

THE LETTER "M" APPEARS BEFORE THE / ON LCC.

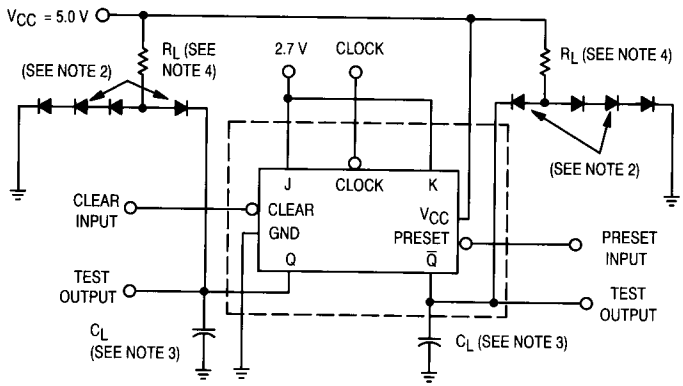
PIN ASSIGNMENTS

FUNCT.	DIL 620-09	FLATS 650-05	LCC 756A-02	BURN-IN (COND. A)
CLK_1	1	1	2	V_{CC}
K_1	2	2	3	V_{CC}
J_1	3	3	4	V_{CC}
PR_1	4	4	5	GND
Q_1	5	5	7	V_{CC}
$\overline{Q}_1$	6	6	8	V_{CC}
$\overline{Q}_2$	7	7	9	V_{CC}
GND	8	8	10	GND
Q_2	9	9	12	V_{CC}
PR_2	10	10	13	GND
J_2	11	11	14	V_{CC}
K_2	12	12	15	V_{CC}
CLK_2	13	13	17	V_{CC}
CLR_2	14	14	18	GND
CLR_1	15	15	19	GND
V_{CC}	16	16	20	V_{CC}

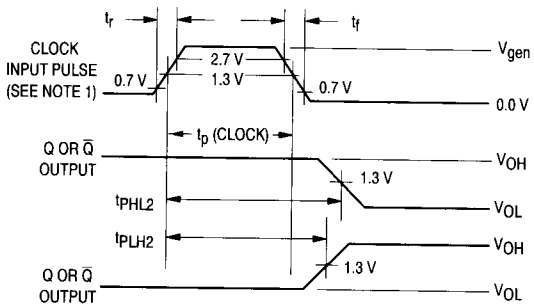
BURN-IN CONDITIONS:
V_{CC} = 5.0 V MIN/6.0 V MAX

5

AC TEST CIRCUIT



WAVEFORMS



NOTES:

1. Clock input characteristics for t_{PLH}, t_{PHL} (clock to output): V_{gen} = 3.0 V, $t_r \leq 15$ ns, t_f = 6.0 ns, t_p (clock) = 25 ns and PRR = ≤ 1.0 MHz. When testing f_{MAX} the clock input characteristics are: V_{gen} = 3.0 V, $t_r = t_f \leq 10$ ns, t_p (clock) ≤ 25 ns and PRR = (see table).
2. All diodes are 1N3064, or equivalent.
3. C_L = 50 pF ± 10% (including jig and probe capacitance).
4. R_L = 2.0 kΩ ± 5.0%.

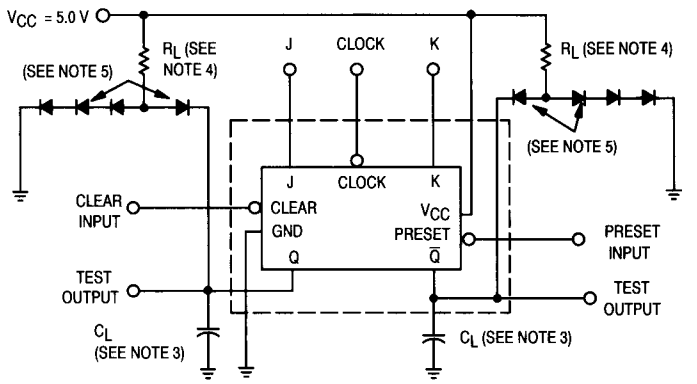
MODE SELECT – TRUTH TABLE

Operating Mode	Inputs				Outputs	
	$\overline{PR}$	$\overline{CLR}$	J	K	Q	$\overline{Q}$
Set	L	H	X	X	H	L
Reset (Clear)	H	L	X	X	L	H
*Undetermined	L	L	X	X	H	H
Toggle	H	H	h	l	$\overline{q}$	q
Load "0" (Reset)	H	H	h	l	L	H
Load "1" (Set)	H	H	l	h	H	L
Hold	H	H	l	h	q	$\overline{q}$

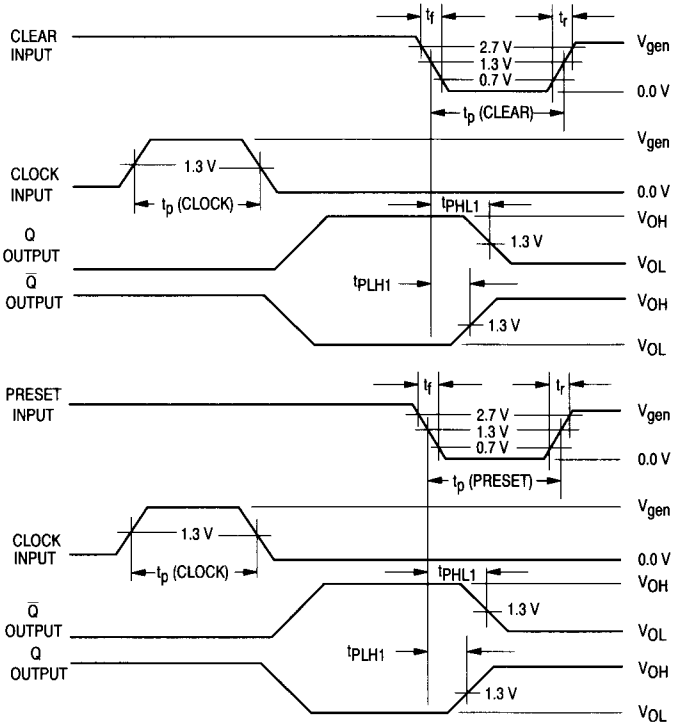
H, h = HIGH Voltage Level
L, l = LOW Voltage Level
X = Don't Care
l, h (q) = Lower case letters indicate the state of referenced input (or output) one set-up time prior to the HIGH to LOW clock transition.

*Both outputs will be HIGH while both $\overline{PR}$ and $\overline{CLR}$ are LOW, but the output states are unpredictable if $\overline{PR}$ and $\overline{CLR}$ go HIGH simultaneously.

AC TEST CIRCUIT



WAVEFORMS

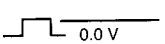


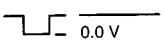
NOTES:

1. Clear or preset inputs dominate regardless of the state of clock J-K inputs.
2. Clear or preset input pulse characteristics: V_{gen} = 3.0 V, $t_r \leq 15$ ns, $t_f \leq 6.0$ ns, PRR $\leq$ 1.0 MHz, t_p (clear) = t_p (preset) = 30 ns, $Z_{OUT} \approx 50\ \Omega$.
3. C_L = 50 pF ± 10% (including jig and probe capacitance).
4. R_L = 2.0 kΩ ± 5.0%.
5. All diodes are 1N3064, or equivalent.
6. When testing clear to output switching, preset shall have a logical "1" voltage applied. When testing preset to output switching, clear input shall have a logical "1" voltage applied (see table).
7. Clock input pulse characteristics: t_p (clock) ≥ 25 ns, V_{gen} = 3.0 V, PRR ≤ 1.0 MHz.

Symbol	Parameter	Limits						Unit	Test Condition (Unless Otherwise Specified)	
		+ 25°C		+ 125°C		− 55°C				
	Static Parameters:	Subgroup 1		Subgroup 2		Subgroup 3				
		Min	Max	Min	Max	Min	Max			
V_{OH}	Logical "1" Output Voltage	2.5		2.5		2.5		V	V_{CC} = 4.5 V, I_{OH} = − 0.4 mA, V_{IN} = 2.0 V, V_{IL} = 0.7 V.	
V_{OL}	Logical "0" Output Voltage		0.4		0.4		0.4	V	V_{CC} = 4.5 V, I_{OL} = 4.0 mA, V_{IH} = 2.0 V, V_{IL} = 0.7 V.	
V_{IC}	Input Clamping Voltage		− 1.5					V	V_{CC} = 4.5 V, I_{IN} = − 18 mA, other inputs are open.	
I_{IH}	Logical "1" Input Current (J & K inputs)		20		20		20	µA	V_{CC} = 5.5 V, V_{IH} = 2.7 V, other inputs = 4.5 V, CLR & CLK = GND.	
I_{IHH}	Logical "1" Input Current (J & K inputs)		100		100		100	µA	V_{CC} = 5.5 V, V_{IHH} = 5.5 V, J & CLR = 4.5 V, PR & CLK = GND.	
I_{IH}	Logical "1" Input Current (CLR & PR)		60		60		60	µA	V_{CC} = 5.5 V, V_{IH} = 2.7 V, other inputs = 4.5 V, CLK & J = GND, PR = (see note 2).	
I_{IHH}	Logical "1" Input Current (CLR & PR)		300		300		300	µA	V_{CC} = 5.5 V, V_{IHH} = 5.5 V, J = 4.5 V, CLK & K = GND, CLR = (see note 2).	
I_{IH}	Logical "1" Input Current (CLK inputs)		80		80		80	µA	V_{CC} = 5.5 V, V_{IH} = 2.7 V, other inputs are GND.	
I_{IHH}	Logical "1" Input Current (CLK inputs)		400		400		400	µA	V_{CC} = 5.5 V, V_{IHH} = 5.5 V, other inputs are GND.	
I_{IL}	Logical "0" Input Current (J & K inputs)	− 0.12	− 0.36	− 0.12	− 0.36	− 0.12	− 0.36	mA	V_{CC} = 5.5 V, V_{IL} = 0.4 V, other inputs = 4.5 V, PR = (see note 2).	
I_{IL}	Logical "0" Input Current (CLK inputs)	− 0.24	− 0.72	− 0.24	− 0.72	− 0.24	− 0.72	mA	V_{CC} = 5.5 V, V_{IL} = 0.4 V, other inputs = 4.5 V, CLR = (see note 2).	
I_{IL}	Logical "0" Input Current (CLR & PR)	− 0.12	− 0.72	− 0.12	− 0.72	− 0.12	− 0.72	mA	V_{CC} = 5.5 V, V_{IL} = 0.4 V, other inputs = 4.5 V, PR is open.	
I_{OS}	Output Short Circuit Current	− 15	− 100	− 15	− 100	− 15	− 100	mA	V_{CC} = 5.5 V, V_{IN} = 4.5 V, other inputs = GND.	
I_{CC}	Power Supply Current		8.0		8.0		8.0	mA	V_{CC} = 5.5 V, other inputs are open.	CLR = 5.5 V. PR = 5.5 V.
V_{IH}	Logical "1" Input Voltage	2.0		2.0		2.0		V	V_{CC} = 4.5 V.	
V_{IL}	Logical "0" Input Voltage		0.7		0.7		0.7	V	V_{CC} = 4.5 V.	
	Functional Tests	Subgroup 7		Subgroup 8A		Subgroup 8B			per Truth Table with V_{CC} = 5.0 V, V_{INL} = 0.V, and V_{INH} = 2.5 V.	

NOTES:

1. =  2.5 V min/5.5 V max

2. =  2.5 V min/5.5 V max

Symbol	Parameter	Limits						Unit	Test Condition (Unless Otherwise Specified)
	Switching Parameters:	+ 25°C		+ 125°C		− 55°C			
		Subgroup 9		Subgroup 10		Subgroup 11			
		Min	Max	Min	Max	Min	Max		
t_{PHL1} t_{PHL1}	Propagation Delay /Data-Output Output High-Low	5.0 —	28 20	5.0 —	40 35	5.0 —	40 35	ns	V_{CC} = 5.0 V, C_L = 50 pF, R_L = 2.0 kΩ ± 5.0%. V_{CC} = 5.0 V, C_L = 15 pF R_L = 2.0 kΩ ± 5.0%.
t_{PLH1} t_{PLH1}	Propagation Delay /Data-Output Output Low-High	5.0 —	21 20	5.0 —	32 27	5.0 —	32 27	ns	V_{CC} = 5.0 V, C_L = 50 pF, R_L = 2.0 kΩ ± 5.0%. V_{CC} = 5.0 V, C_L = 15 pF, R_L = 2.0 kΩ ± 5.0%.
t_{PHL2}	Propagation Delay /Data-Output Output High-Low	5.0	30	5.0	42	5.0	42	ns	V_{CC} = 5.0 V, C_L = 50 pF, R_L = 2.0 kΩ ± 5.0%.
t_{PLH2}	Propagation Delay /Data-Output Output Low-High	5.0	22	5.0	32	5.0	32	ns	V_{CC} = 5.0 V, C_L = 50 pF, R_L = 2.0 kΩ ± 5.0%.
f_{MAX}	Maximum Clock Frequency	25		25		25		MHz	V_{CC} = 5.0 V, V_{IN} = 2.7 V, C_L = 50 pF, R_L = 2.0 kΩ ± 5.0%.
f_{MAX}	Maximum Clock Frequency	30						MHz	V_{CC} = 5.0 V, C_L = 15 pF, R_L = 2.0 kΩ ± 5.0%.

NOTES:

1. f_{MAX}, min. limit specified is the frequency of the input pulse. The output frequency shall be one-half of the input frequency.
2. Tests shall be performed in sequence, attributes data only.
3. The limits specified for C_L = 15 pF are guaranteed but not tested.

5