THIS SPEC IS OBSOLETE

Spec No: 001-52039

Spec Title: STK17TA8 128K X 8 AUTOSTORE NVSRAM WITH REAL TIME CLOCK

Sunset Owner: Girija Chougala (GVCH)

Replaced by: None

STK17TA8

128k X 8 AutoStore nvSRAM with Real Time Clock

Features

- nvSRAM Combined with Integrated Real Time Clock Functions (RTC, Watchdog Timer, Clock Alarm, Power Monitor)
- Capacitor or Battery Backup for RTC
- 25 ns [1], 45 ns Read Access and Read/Write Cycle Time
- Unlimited Read/Write Endurance
- Automatic nonvolatile STORE on Power Loss
- Nonvolatile STORE Under Hardware or Software Control
- Automatic RECALL to SRAM on Power Up
- Unlimited RECALL Cycles
- 200K STORE Cycles
- 20-Year nonvolatile Data Retention
- Single 3 V +20%, -10% Power Supply
- Commercial and Industrial Temperatures
- 48-pin 300-mil SSOP Package (RoHS-Compliant)

Description

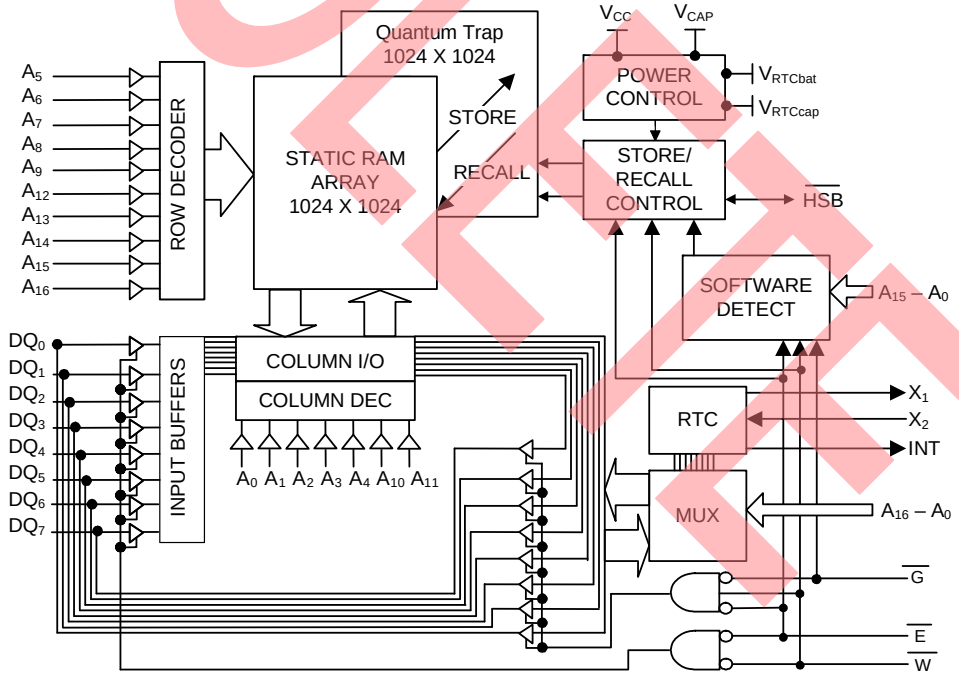
The Cypress STK17TA8 combines a 1 Mb nonvolatile static RAM (nvSRAM) with a full featured real time clock in a reliable, monolithic integrated circuit.

The 1 Mb nvSRAM is a fast static RAM with a nonvolatile Quantum Trap storage element included with each memory cell.

The SRAM provides the fast access and cycle times, ease of use and unlimited read and write endurance of a normal SRAM. Data transfers automatically to the nonvolatile storage cells when power loss is detected (the STORE operation). On power up, data is automatically restored to the SRAM (the RECALL operation). Both STORE and RECALL operations are also available under software control.

The real time clock function provides an accurate clock with leap year tracking and a programmable, high accuracy oscillator. The Alarm function is programmable for one-time alarms or periodic minutes, hours, or days alarms. There is also a programmable watchdog timer for processor control.

Logic Block Diagram

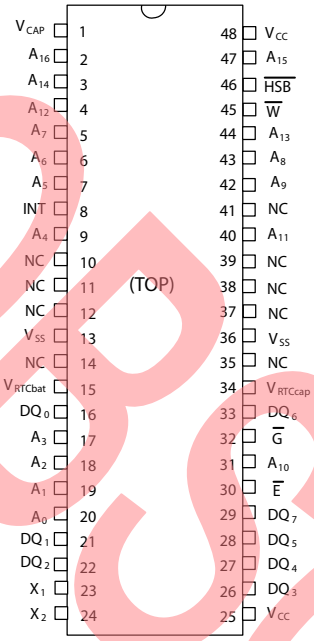


Note
1. 25 ns speed in Industrial temperature range is over the operating voltage range of 3.3V± 0.3V only.

Contents

Pinouts

Figure 1. Pin Diagram - 48-Pin SSOP



Relative PCB Area Usage[2]

Pin Descriptions

Pin Name	I/O Type	Description
A_{16}-A_0	Input	**Address**: The 17 address inputs select one of 131,072 bytes in the nvSRAM array or one of 16 bytes in the clock register map
DQ_7-DQ_0	I/O	**Data**: Bi-directional 8-bit data bus for accessing the nvSRAM and RTC
E	Input	**Chip Enable**: The active low $\overline{E}$ input selects the device
W	Input	**Write Enable**: The active low $\overline{W}$ enables data on the DQ pins to be written to the address location selected on the falling edge of $\overline{E}$
G	Input	**Output Enable**: The active low $\overline{G}$ input enables the data output buffers during read cycles. De-asserting $\overline{G}$ high caused the DQ pins to tristate.
X_1	Output	**Crystal Connection, drives crystal on startup**
X_2	Input	**Crystal Connection for 32.768 kHz crystal**
V_{RTCcap}	Power Supply	**Capacitor supplied backup RTC supply voltage (Left unconnected if V_{RTCbat} is used)**
V_{RTCbat}	Power Supply	**Battery supplied backup RTC supply voltage (Left unconnected if V_{RTCcap} is used)**
V_{CC}	Power Supply	**Power**: 3.0V, +20%, -10%
HSB	I/O	**Hardware Store Busy**: When low this output indicates a Store is in progress. When pulled low external to the chip, it initiates a nonvolatile STORE operation. A weak pull up resistor keeps this pin high if not connected. (Connection Optional).
INT	Output	**Interrupt Control**: Can be programmed to respond to the clock alarm, the watchdog timer and the power monitor. Programmable to either active high (push/pull) or active low (open-drain)
V_{CAP}	Power Supply	**Autostore Capacitor**: Supplies power to nvSRAM during power loss to store data from SRAM to nonvolatile storage elements.
V_{SS}	Power Supply	**Ground**
NC	No Connect	**Unlabeled pins have no internal connections.**

Note
2. For detailed package size specifications, See "Package Diagrams" on page 23..

Absolute Maximum Ratings

Voltage on Input Relative to Ground .....–0.1V to 4.1V
Voltage on Input Relative to V_{SS} .....–0.5V to (V_{CC} + 0.5V)
Voltage on DQ_{0-7} or $\overline{HSB}$.....–0.5V to (V_{CC} + 0.5V)
Temperature under Bias ..... –55°C to 125°C
Junction Temperature ..... –55°C to 140°C
Storage Temperature ..... –65°C to 150°C
Power Dissipation..... 1W
DC Output Current (1 output at a time, 1s duration).... 15 mA

RF (SSOP-48) Package Thermal Characteristics

θ_{jc} 6.2 C/W; θ_{ja} 51.1 [0 fpm], 44.7 [200 fpm], 41.8 C/W [500 fpm]

Note Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC Electrical Characteristics

(V_{CC} = 2.7V-3.6V)

Symbol	Parameter	Commercial		Industrial		Units	Notes
		Min	Max	Min	Max		
I_{CC_1}	Average V_{CC} Current		65 50		70 55	mA mA	t_{AVAV} = 25 ns t_{AVAV} = 45 ns Dependent on output loading and cycle rate. Values obtained without output loads.
I_{CC_2}	Average V_{CC} Current during *STORE*		3		3	mA	All Inputs Don't Care, V_{CC} = max Average current for duration of STORE cycle (t_{STORE})
I_{CC_3}	Average V_{CC} Current at t_{AVAV} = 200ns 3V, 25°C, Typical		10		10	mA	$\overline{W} \geq (V_{CC} - 0.2V)$ All Other Inputs Cycling at CMOS Levels Dependent on output loading and cycle rate. Values obtained without output loads.
I_{CC_4}	Average V_{CAP} Current during <Emphasis>AutoStore™ Cycle		3		3	mA	All Inputs Don't Care Average current for duration of STORE cycle (t_{STORE})
I_{SB}	V_{CC} Standby Current (Standby, Stable CMOS Levels)		3		3	mA	$E \geq (V_{CC} - 0.2V)$ All Others $V_{IN} \leq 0.2V$ or $\geq (V_{CC} - 0.2V)$ Standby current level after nonvolatile cycle complete
I_{ILK}	Input Leakage Current		±1		±1	mA	V_{CC} = max $V_{IN} = V_{SS}$ to V_{CC}
I_{OLK}	Off-State Output Leakage Current		±1		±1	mA	V_{CC} = max $V_{IN} = V_{SS}$ to V_{CC}, $\overline{E}$ or $\overline{G} \geq V_{IH}$
V_{IH}	Input Logic "1" Voltage	2.0	V_{CC} + 0.5	2.0	V_{CC} + 0.5	V	All Inputs
V_{IL}	Input Logic "0" Voltage	V_{SS} –0.5	0.8	V_{SS} –0.5	0.8	V	All Inputs
V_{OH}	Output Logic "1" Voltage	2.4		2.4		V	I_{OUT} = –2 mA (except $\overline{HSB}$)
V_{OL}	Output Logic "0" Voltage		0.4		0.4	V	I_{OUT} = 4 mA

Note

- The $\overline{HSB}$ pin has I_{OUT}=-10uA for V_{OH} of 2.4V, this parameter is characterized but not tested.
- The INT is open-drain and does not source or sink high current when interrupt Register bit D3 is below.

DC Electrical Characteristics (continued)

(V_{CC} = 2.7V-3.6V)

Symbol	Parameter	Commercial		Industrial		Units	Notes
		Min	Max	Min	Max		
T_A	Operating Temperature	0	70	–40	85	°C	
V_{CC}	Operating Voltage	2.7	3.6	2.7	3.6	V	3.0V +20%, -10%
V_{CAP}	Storage Capacitance	17	57	17	57	µF	Between V_{CAP} pin and V_{SS}, 5V rated.
NV_C	Nonvolatile STORE operations	200		200		K	
$DATA_R$	Data Retention	20		20		Years	At 55 °C

AC Test Conditions

Input Pulse Levels .....0V to 3V
Input Rise and Fall Times ..... ≤5 ns
Input and Output Timing Reference Levels 1.5V
Output Load.....See Figure 2 and Figure 3

Capacitance

(T_A = 25°C, f = 1.0MHz)[3]

Symbol	Parameter	Max	Units	Conditions
C_{IN}	Input Capacitance	7	pF	ΔV = 0 to 3V
C_{OUT}	Output Capacitance	7	pF	ΔV = 0 to 3V

Figure 2. AC Output Loading

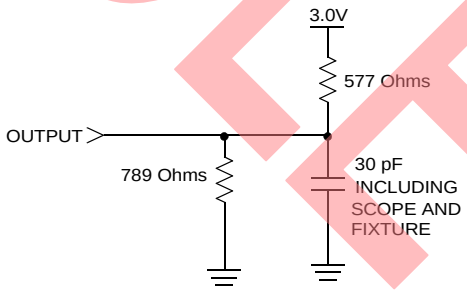
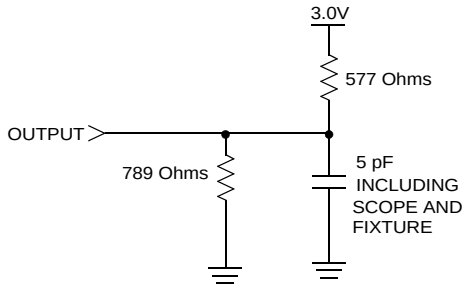


Figure 3. AC Output Loading for Tristate Specs (t_{HZ}, t_{LZ}, t_{WLQZ}, t_{WHQZ}, t_{GLQX}, t_{GHQZ}

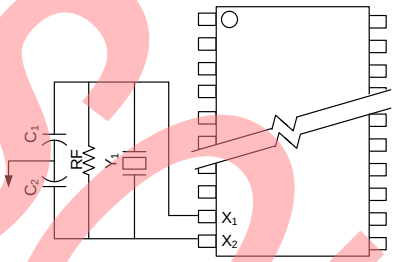


Note
3. These parameters are guaranteed but not tested.

RTC DC Characteristics

Symbol	Parameter	Commercial		Industrial		Units	Notes
		Min	Max	Min	Max		
I_{BAK}	RTC Backup Current	—	300	—	350	nA	From either V_{RTCcap} or V_{RTCbat}
VRTCbat	RTC Battery Pin Voltage	1.8	3.3	1.8	3.3	V	Typical = 3.0 Volts during normal operation
VRTCcap	RTC Capacitor Pin Voltage	1.2	2.7	1.2	2.7	V	Typical = 2.4 Volts during normal operation
tOSCS	RTC Oscillator time to start	—	10	—	10	sec	At MIN Temperature from Power up or Enable
		—	5	—	5	sec	At 25°C from Power up or Enable

Figure 4. RTC Recommended Component Configuration



Recommended Values

Y_1 = 32.768 KHz

RF = 10M Ohm

C_1 = 0 (install cap footprint, but leave unloaded)

C_2 = 56 pF ± 10% (do not vary from this value)

SRAM READ Cycles #1 and #2

NO.	Symbols			Parameter	STK17TA8-25[1]		STK17TA8-45		Units
	#1	#2	Alt.		Min	Max	Min	Max	
1		t_{ELQV}	t_{ACS}	Chip Enable Access Time		25		45	ns
2	t_{AVAV}[4]	t_{ELEH}[4]	t_{RC}	Read Cycle Time	25		45		ns
3	t_{AVQV}[5]	t_{AVQV}[5]	t_{AA}	Address Access Time		25		45	ns
4		t_{GLQV}	t_{OE}	Output Enable to Data Valid		12		20	ns
5	t_{AXQX}[5]	t_{AXQX}[5]	t_{OH}	Output Hold after Address Change	3		3		ns
6		t_{ELQX}	t_{LZ}	Address Change or Chip Enable to Output Active	3		3		ns
7		t_{EHQZ}[6]	t_{HZ}	Address Change or Chip Disable to Output Inactive		10		15	ns
8		t_{GLQX}	t_{OLZ}	Output Enable to Output Active	0		0		ns
9		t_{GHQZ}[6]	t_{OHZ}	Output Disable to Output Inactive		10		15	ns
10		t_{ELICCL}[3]	t_{PA}	Chip Enable to Power Active	0		0		ns
11		t_{EHICCH}[3]	t_{PS}	Chip Disable to Power Standby		25		45	ns

Figure 5. SRAM READ Cycle #1: Address Controlled[4, 5, 7]

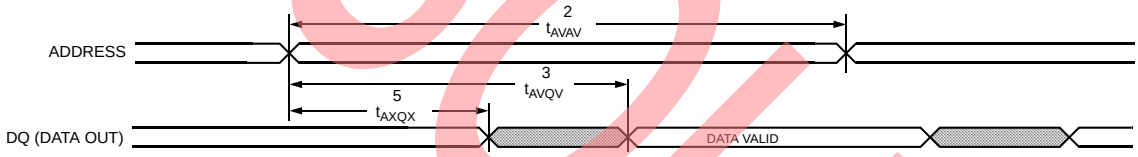
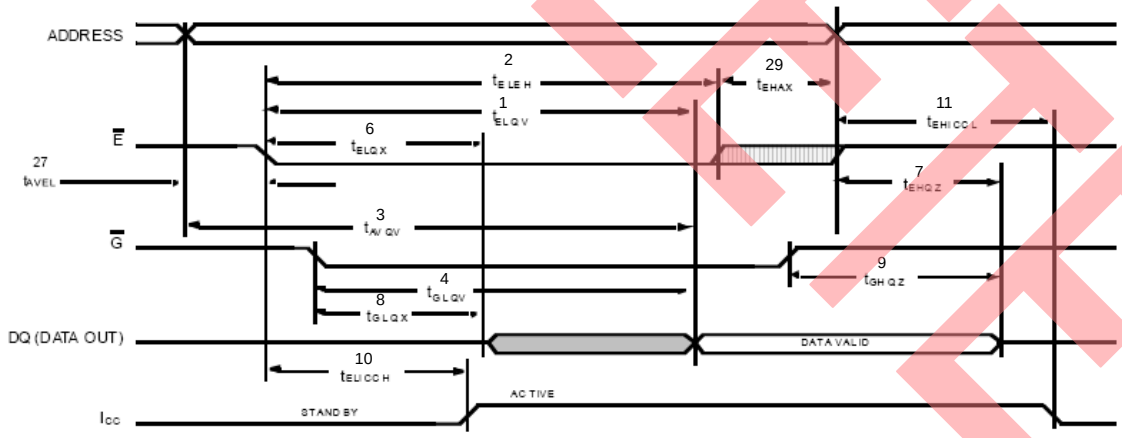


Figure 6. SRAM READ Cycle #2: $\overline{E}$ and $\overline{G}$ Controlled[4, 7]



Notes
4. $\overline{W}$ must be high during SRAM READ cycles.
5. Device is continuously selected with $\overline{E}$ and $\overline{G}$ both low
6. Measured ± 200mV from steady state output voltage.
7. $\overline{HSB}$ must remain high during READ and WRITE cycles.

SRAM WRITE Cycles #1 and #2

NO.	Symbols			Parameter	STK17TA8-25[1]		STK17TA8-45		Units
	#1	#2	Alt.		Min	Max	Min	Max	
11	t_{AVAV}	t_{AVAV}	t_{WC}	Write Cycle Time	25		45		ns
13	t_{WLWH}	t_{WLEH}	t_{WP}	Write Pulse Width	20		30		ns
14	t_{ELWH}	t_{ELEH}	t_{CW}	Chip Enable to End of Write	20		30		ns
15	t_{DVWH}	t_{DVEH}	t_{DW}	Data Setup to End of Write	10		15		ns
16	t_{WHDX}	t_{EHDX}	t_{DH}	Data Hold after End of Write	0		0		ns
17	t_{AVWH}	t_{AVEH}	t_{AW}	Address Setup to End of Write	20		30		ns
18	t_{AVWL}	t_{AVEL}	t_{AS}	Address Setup to Start of Write	0		0		ns
19	t_{WHAX}	t_{EHAX}	t_{WR}	Address Hold after End of Write	0		0		ns
20	t_{WLQZ}[6, 8]		t_{WZ}	Write Enable to Output Disable		10		15	ns
21	t_{WHQX}		t_{OW}	Output Active after End of Write	3		3		ns

Figure 7. SRAM WRITE Cycle #1: $\overline{W}$ Controlled[8, 9]

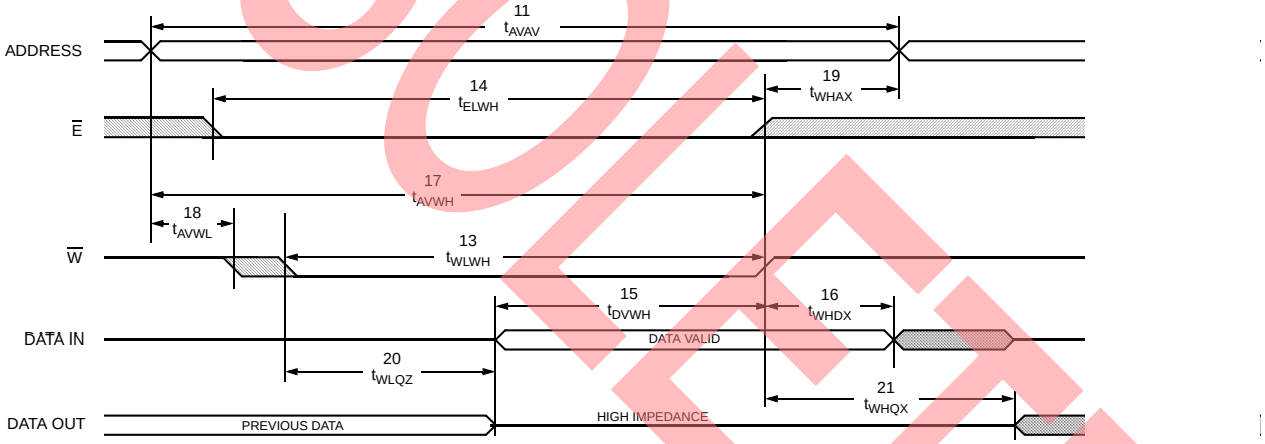
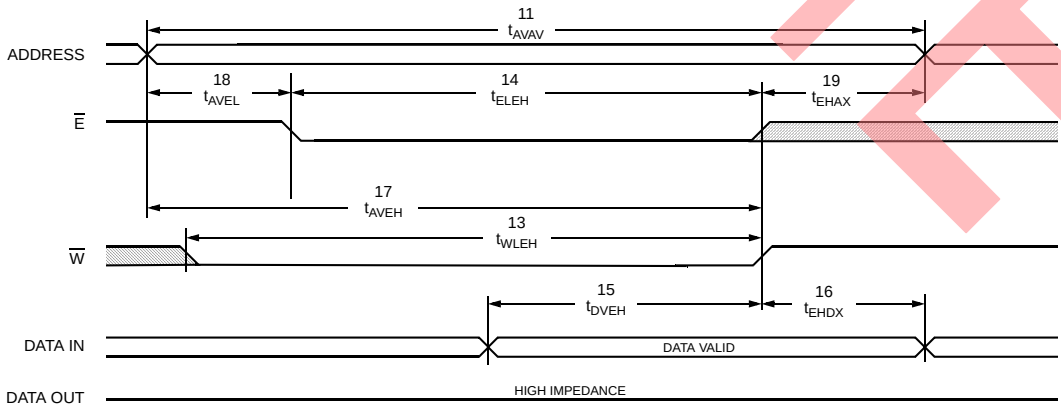


Figure 8. SRAM WRITE Cycle #2: $\overline{E}$ Controlled[8, 9]

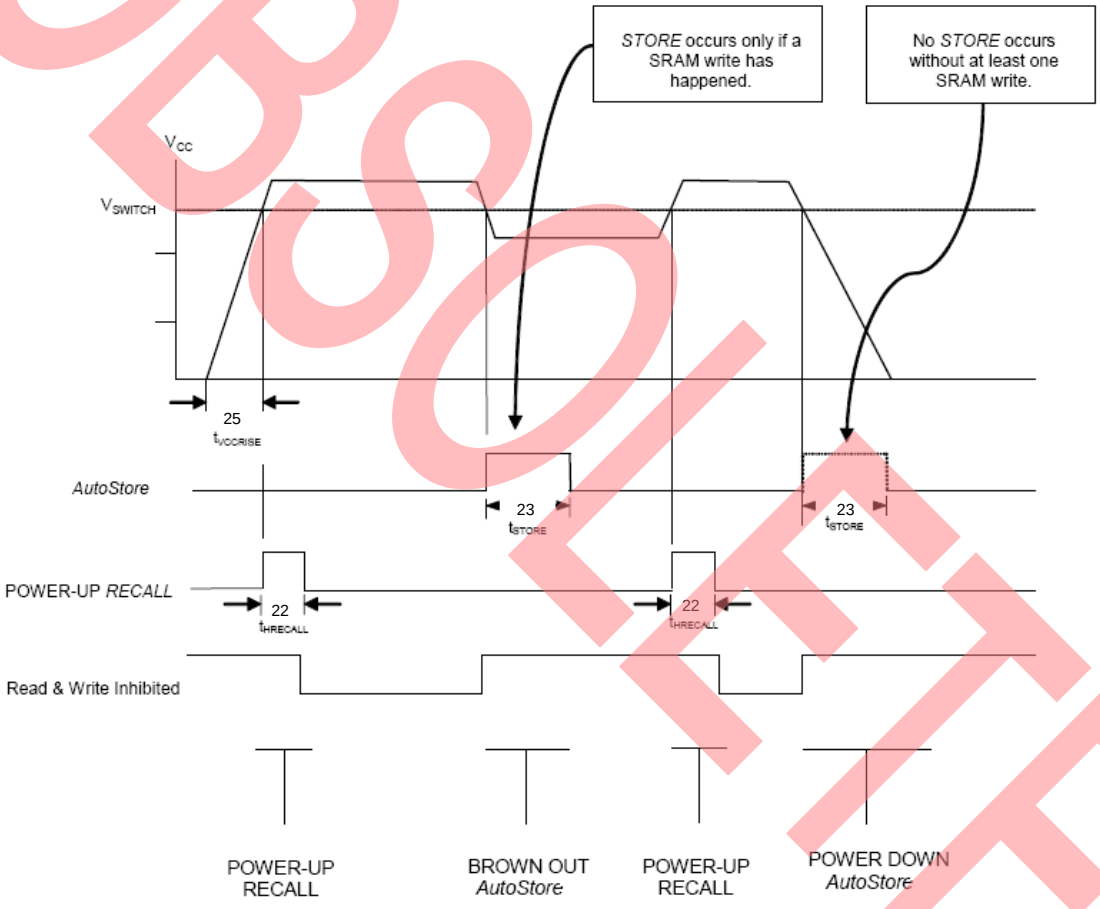


Notes
8. If $\overline{W}$ is low when $\overline{E}$ goes low, the outputs remain in the high-impedance state.
9. $\overline{E}$ or $\overline{W}$ must be ≥ V_{IH} during address transitions.

AutoStore/Power Up Recall

NO.	Symbols		Parameter	STK17TA8		Units	Notes
	Standard	Alternate		Min	Max		
22	$t_{HRECALL}$		Power up *RECALL* Duration		40	ms	10
23	t_{STORE}	t_{HLHZ}	*STORE* Cycle Duration		12.5	ms	11,12
24	V_{SWITCH}		Low Voltage Trigger Level		2.65	V	
25	V_{CCRISE}		V_{CC} Rise Time	150		µS	

Figure 9. AutoStore/Power Up RECALL



NOTE: Read and Write cycles will be ignored during STORE, RECALL and while V_{CC} is below V_{SWITCH}

Notes
10. $t_{HRECALL}$ starts from the time V_{CC} rises above V_{SWITCH}
11. If an SRAM WRITE has not taken place since the last nonvolatile cycle, no STORE will take place
12. Industrial Grade Devices require 15 ms MAX.

Software-Controlled STORE/RECALL Cycle

In the following table, the software controlled STORE and RECALL cycle parameters are listed. [13, 14]

NO.	Symbols			Parameter	STK17TA8-25[1]		STK17TA8-45		Units	Notes
	$\overline{E}$ Cont	$\overline{G}$ Cont	Alternate		Min	Max	Min	Max		
26	t_{AVAV}	t_{AVAV}	t_{RC}	*STORE* / *RECALL* Initiation Cycle Time	25		45		ns	14
27	t_{AVEL}	t_{AVGL}	tAS	Address Setup Time	0		0		ns	
28	t_{ELEH}	t_{GLGH}	tCW	Clock Pulse Width	20		30		ns	
29	t_{EHAX}	t_{GHAX}		Address Hold Time	1		1		ns	
30	t_{RECALL}	t_{RECALL}		*RECALL* Duration		100		100	µs	

Figure 10. Software *STORE/RECALL* Cycle: $\overline{E}$ CONTROLLED[14]

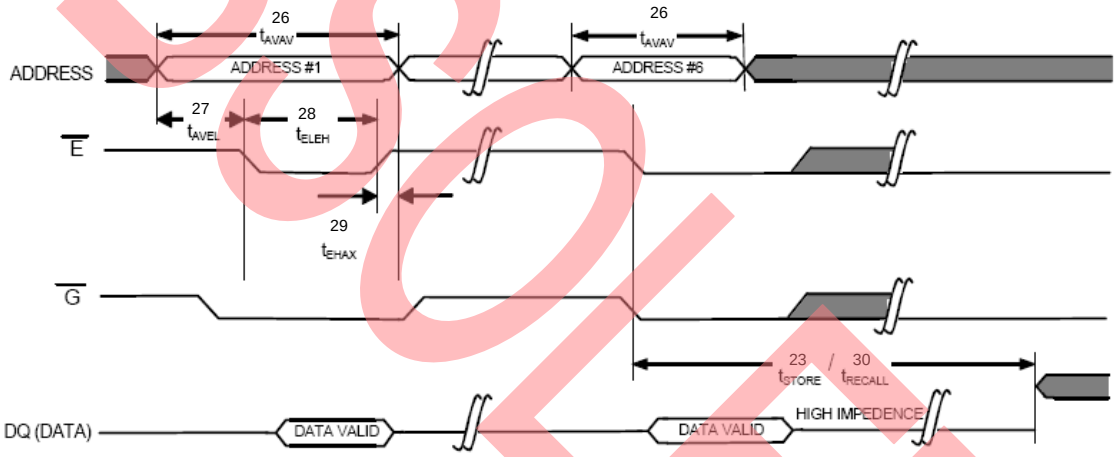
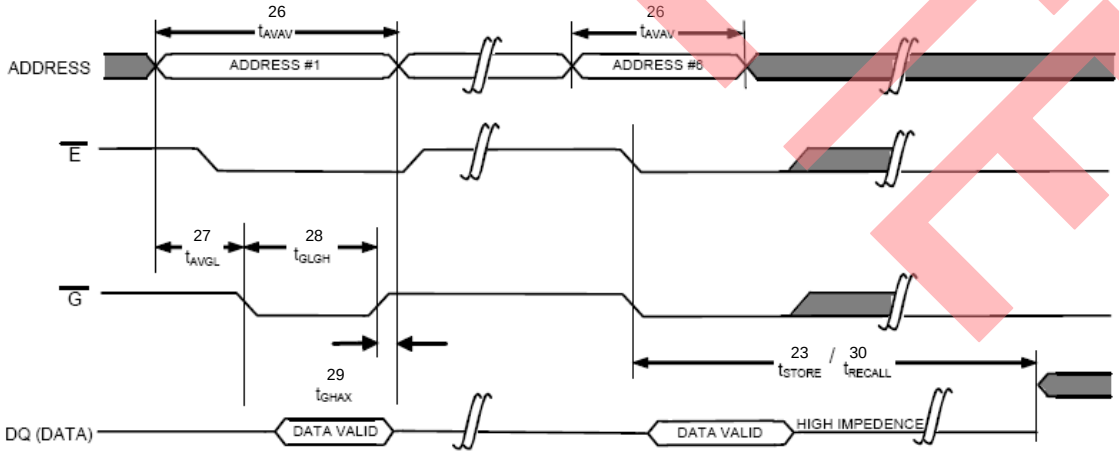


Figure 11. Software *STORE/RECALL* Cycle: $\overline{G}$ Controlled[14]



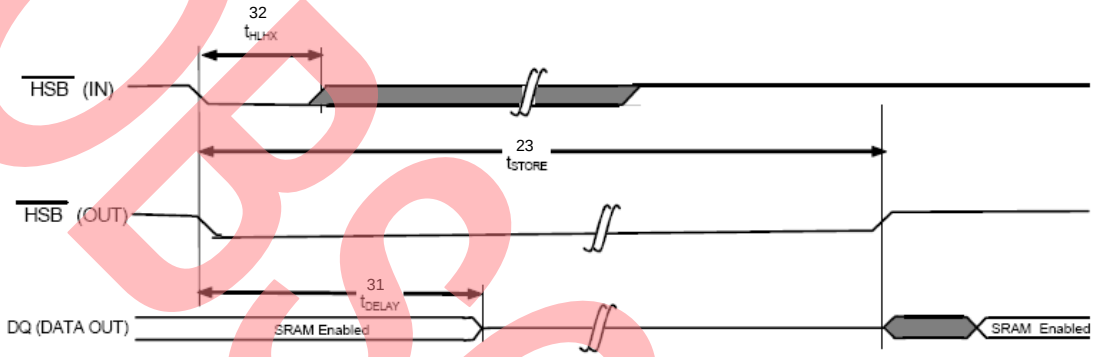
Notes

13. The software sequence is clocked on the falling edge of $\overline{E}$ controlled READs or $\overline{G}$ controlled READs
14. The six consecutive addresses must be read in the order listed in the Software *STORE/RECALL* Mode Selection Table W must be high during all six consecutive cycles.

Hardware STORE Cycle

NO.	Symbols		Parameter	STK17TA8		Units	Notes
	Standard	Alternate		Min	Max		
31	t_{DELAY}	t_{HLQZ}	Hardware STORE to SRAM Disabled	1	70	µs	15
32	t_{HLHX}		Hardware STORE Pulse Width	15		ns	

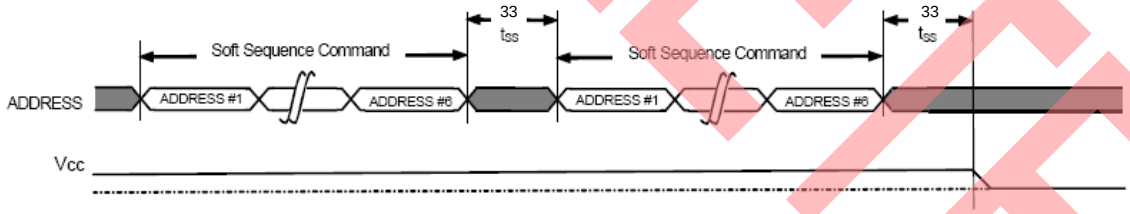
Figure 12. Hardware STORE Cycle



Soft Sequence Commands

NO.	Symbols	Parameter	STK17TA8		Units	Notes
	Standard		Min	Max		
33	t_{SS}	Soft Sequence Processing Time		70	µs	16,17

Figure 13. Soft Sequence Commands



Notes
15. On a hardware STORE initiation, SRAM operation continues to be enabled for time tDELAY to allow READ/WRITE cycles to compete.
16. This is the amount of time that it takes to take action on a soft sequence command. Vcc power must remain high to effectively register command.
17. Commands like Store and Recall lock out I/O until operation is complete which further increases this time. See specific command.

MODE Selection

$\overline{E}$	$\overline{W}$	$\overline{G}$	A_{16}-A_0	Mode	I/O	Power	Notes
H	X	X	X	Not Selected	Output High Z	Standby	
L	H	L	X	Read SRAM	Output Data	Active	
L	L	X	X	Write SRAM	Input Data	Active	
L	H	L	0x04E38 0x0B1C7 0x083E0 0x07C1F 0x0703F	Read SRAM Read SRAM Read SRAM Read SRAM Read SRAM	Output Data Output Data Output Data Output Data Output Data	Active	18, 19, 20
			0x08FC0	Nonvolatile Store	Output High Z	I_{CC2}	
L	H	L	0x04E38 0x0B1C7 0x083E0 0x07C1F 0x0703F 0x04C63	Read SRAM Read SRAM Read SRAM Read SRAM Read SRAM Nonvolatile Recall	Output Data Output Data Output Data Output Data Output Data Output High Z	Active	18, 19, 20

Notes
18. The six consecutive addresses must be in the order listed. $\overline{W}$ must be high during all six consecutive cycles to enable a nonvolatile cycle.
19. While there are 17 addresses on the STK17TA8, only the lower 16 are used to control software modes
20. I/O state depends on the state of $\overline{G}$. The I/O table shown assumes $\overline{G}$ low

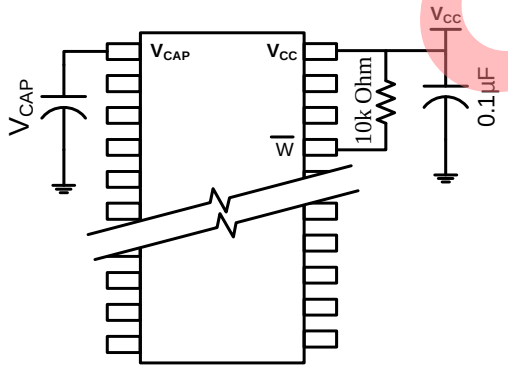
nvSRAM Operation

The STK17TA8 nvSRAM is made up of two functional components paired in the same physical cell. These are the SRAM memory cell and a nonvolatile QuantumTrap cell. The SRAM memory cell operates like a standard fast static RAM. Data in the SRAM can be transferred to the nonvolatile cell (the STORE operation), or from the nonvolatile cell to SRAM (the RECALL operation). This unique architecture enables all cells to be stored and recalled in parallel. During the STORE and RECALL operations SRAM READ and WRITE operations are inhibited. The STK17TA8 supports unlimited read and writes like a typical SRAM. In addition, it provides unlimited RECALL operations from the nonvolatile cells and up to 200K STORE operations.

SRAM READ

The STK17TA8 performs a READ cycle whenever $\overline{E}$ and $\overline{G}$ are low while $\overline{W}$ and $\overline{HSB}$ are high. The address specified on pins A_{0-16} determine which of the 131,072 data bytes are accessed. When the READ is initiated by an address transition, the outputs are valid after a delay of t_{AVQV} (READ cycle #1). If the READ is initiated by $\overline{E}$ and $\overline{G}$, the outputs are valid at t_{ELQV} or at t_{GLQV}, whichever is later (READ cycle #2). The data outputs repeatedly respond to address changes within the t_{AVQV} access time without the need for transitions on any control input pins, and remain valid until another address change or until $\overline{E}$ or $\overline{G}$ is brought high, or $\overline{W}$ and $\overline{HSB}$ is brought low.

Figure 14. AutoStore Mode



SRAM WRITE

A WRITE cycle is performed whenever $\overline{E}$ and $\overline{W}$ are low and $\overline{HSB}$ is high. The address inputs must be stable prior to entering the WRITE cycle and must remain stable until either $\overline{E}$ or $\overline{W}$ goes high at the end of the cycle. The data on the common I/O pins DQ0-7 is written into memory if it is valid t_{DVWH} before the end of a $\overline{W}$ controlled WRITE or t_{DVEH} before the end of an $\overline{E}$ controlled WRITE.

It is recommended that $\overline{G}$ be kept high during the entire WRITE cycle to avoid data bus contention on common I/O lines. If $\overline{G}$ is left low, internal circuitry turns off the output buffers t_{WLQZ} after $\overline{W}$ goes low.

AutoStore Operation

The STK17TA8 stores data to nvSRAM using one of three storage operations. These three operations are Hardware Store (activated by $\overline{HSB}$), Software Store (activated by an address sequence), and AutoStore (on power down).

AutoStore operation, a unique feature of Cypress QuantumTrap technology is a standard feature on the STK17TA8.

During normal operation, the device draws current from V_{CC} to charge a capacitor connected to the V_{CAP} pin. This stored charge is used by the chip to perform a single STORE operation. If the voltage on the V_{CC} pin drops below V_{SWITCH}, the part automatically disconnects the V_{CAP} pin from V_{CC}. A STORE operation is initiated with power provided by the V_{CAP} capacitor.

Figure 14 shows the proper connection of the storage capacitor (V_{CAP}) for automatic store operation. Refer to the DC Electrical Characteristics on page 4 for the size of the capacitor. The voltage on the V_{CAP} pin is driven to 5V by a charge pump internal to the chip. A pull up should be placed on $\overline{W}$ to hold it inactive during power up.

To reduce unneeded nonvolatile stores, AutoStore and Hardware Store operations are ignored unless at least one WRITE operation has taken place since the most recent STORE or RECALL cycle. Software initiated STORE cycles are performed regardless of whether a WRITE operation has taken place. The $\overline{HSB}$ signal can be monitored by the system to detect an AutoStore cycle is in progress.

Hardware STORE ($\overline{HSB}$) Operation

The STK17TA8 provides the $\overline{HSB}$ pin for controlling and acknowledging the STORE operations. The $\overline{HSB}$ pin can be used to request a hardware STORE cycle. When the $\overline{HSB}$ pin is driven low, the STK17TA8 conditionally initiates a STORE operation after t_{DELAY}. An actual STORE cycle only begins if a WRITE to the SRAM took place since the last STORE or RECALL cycle. The $\overline{HSB}$ pin has a very resistive pullup and is internally driven low to indicate a busy condition while the STORE (initiated by any means) is in progress. This pin should be externally pulled up if it is used to drive other inputs.

SRAM READ and WRITE operations that are in progress when $\overline{HSB}$ is driven low by any means are given time to complete before the STORE operation is initiated. After $\overline{HSB}$ goes low, the STK17TA8 continues to allow SRAM operations for t_{DELAY}. During t_{DELAY}, multiple SRAM READ operations may take place. If a WRITE is in progress when $\overline{HSB}$ is pulled low, it is allowed a time, t_{DELAY}, to complete. However, any SRAM WRITE cycles requested after $\overline{HSB}$ goes low is inhibited until $\overline{HSB}$ returns high.

If $\overline{HSB}$ is not used, it should be left unconnected.

Hardware RECALL (POWER UP)

During power up or after any low power condition (V_{CC}<V_{SWITCH}), an internal RECALL request is latched. When V_{CC} once again exceeds the sense voltage of V_{SWITCH}, a RECALL cycle is automatically initiated and takes $t_{HRECALL}$ to complete.

Software STORE

Data can be transferred from the SRAM to the nonvolatile memory by a software address sequence. The STK17TA8 software STORE cycle is initiated by executing sequential $\overline{E}$ controlled or $\overline{G}$ controlled READ cycles from six specific address locations in exact order. During the STORE cycle, previous data is erased and then the new data is programmed into the nonvol-

atile elements. Once a STORE cycle is initiated, further memory inputs and outputs are disabled until the cycle is completed.

To initiate the Software STORE cycle, the following read sequence must be performed:

1. Read Address 0x4E38 Valid READ
2. Read Address 0xB1C7 Valid READ
3. Read Address 0x83E0 Valid READ
4. Read Address 0x7C1F Valid READ
5. Read Address 0x703F Valid READ
6. Read Address 0x8FC0 Initiate STORE Cycle

Once the sixth address in the sequence has been entered, the STORE cycle starts and the chip is disabled. It is important that READ cycles and not WRITE cycles be used in the sequence and that $\overline{G}$ is active. After the t_{STORE} cycle time has been fulfilled, the SRAM is again activated for READ and WRITE operation.

Software RECALL

Data is transferred from nonvolatile memory to the SRAM by a software address sequence. A Software RECALL cycle is initiated with a sequence of READ operations in a manner similar to the Software STORE initiation. To initiate the RECALL cycle, the following sequence of $\overline{E}$ or $\overline{G}$ controlled or READ operations must be performed:

1. Read Address 0x4E38 Valid READ
2. Read Address 0xB1C7 Valid READ
3. Read Address 0x83E0 Valid READ
4. Read Address 0x7C1F Valid READ
5. Read Address 0x703F Valid READ
6. Read Address 0x4C63 Initiate RECALL Cycle

Internally, RECALL is a two-step procedure. First, the SRAM data is cleared, and second, the nonvolatile information is transferred into the SRAM cells. After the t_{RECALL} cycle time, the SRAM is once again be ready for READ or WRITE operations. The RECALL operation in no way alters the data in the nonvolatile storage elements.

Data Protection

The STK17TA8 protects data from corruption during low-voltage conditions by inhibiting all externally initiated STORE and WRITE operations. The low voltage condition is detected when V_{CC}<V_{SWITCH}.

If the STK17TA8 is in a WRITE mode (both $\overline{E}$ and $\overline{W}$ low) at power up, after a RECALL, or after a STORE, the WRITE will be inhibited until a negative transition on $\overline{E}$ or $\overline{W}$ is detected. This protects against inadvertent writes during power up or brown out conditions.

Noise Considerations

The STK17TA8 is a high speed memory and so must have a high frequency bypass capacitor of 0.1 µF connected between both V_{CC} pins and V_{SS} ground plane with no plane break to chip V_{SS}. Use leads and traces that are as short as possible. As with all high speed CMOS ICs, careful routing of power, ground, and signals reduces circuit noise.

Preventing AutoStore

Because of the use of nvSRAM to store critical RTC data, the AutoStore function cannot be disabled on the STK17TA8.

Best Practices

nvSRAM products have been used effectively for over 15 years. While ease-of-use is one of the product's main system values, experience gained working with hundreds of applications has resulted in the following suggestions as best practices:

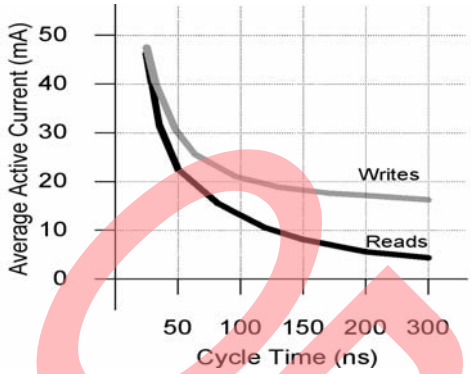
- The nonvolatile cells in an nvSRAM are programmed on the test floor during final test and quality assurance. Incoming inspection routines at customer or contract manufacturer's sites sometimes reprogram these values. Final NV patterns are typically repeating patterns of AA, 55, 00, FF, A5, or 5A. End product's firmware should not assume an NV array is in a set programmed state. Routines that check memory content values to determine first time system configuration, cold or warm boot status, should always program a unique NV pattern (for example, complex 4-byte pattern of 46 E6 49 53 hex or more random bytes) as part of the final system manufacturing test to ensure these system routines work consistently.
- Power up boot firmware routines should rewrite the nvSRAM into the desired state (autostore enabled and so on). While the nvSRAM is shipped in a preset state, best practice is to again rewrite the nvSRAM into the desired state as a safeguard against events that might flip the bit inadvertently (program bugs, incoming inspection routines, and so on.
- The OSCEN bit in the Calibration register at 0x1FFF8 should be set to 1 to preserve battery life when the system is in storage (see "Stopping And Starting The RTC Oscillator" on page 15).
- The V_{cap} value specified in this data sheet includes a minimum and a maximum value size. Best practice is to meet this requirement and not exceed the max V_{cap} value because the nvSRAM internal algorithm calculates V_{cap} charge time based on this max Vcap value. Customers that want to use a larger V_{cap} value to make sure there is extra store charge and store time should discuss their V_{cap} size selection with Cypress to understand any impact on the V_{cap} voltage level at the end of a t_{RECALL} period.

Low Average Active Power

CMOS technology provides the STK17TA8 with the benefit of power supply current that scales with cycle time. Less current is drawn as the memory cycle time becomes longer than 50 ns. Figure 15 shows the relationship between I_{CC} and READ/WRITE cycle time. Worst-case current consumption is shown for commercial temperature range, V_{CC}=3.6V, and chip enable at maximum frequency. Only standby current is drawn when the chip is disabled. The overall average current drawn by the STK17TA8 depends on the following items:

1. The duty cycle of chip enable.
2. The overall cycle rate for accesses.
3. The ration of READs to WRITEs.
4. The operating temperature.
5. The VCC level.
6. I/O loading.

Figure 15. Current versus Cycle Time



RTC Operations

Real Time Clock

The clock registers maintain time up to 9,999 years in one second increments. The user can set the time to any calendar time and the clock automatically keeps track of days of the week and month, leap years, and century transitions. There are eight registers dedicated to the clock functions which are used to set time with a write cycle and to read time during a read cycle. These registers contain the Time of Day in BCD format. Bits defined as "0" are currently not used and are reserved for future use by Cypress.

Reading The Clock

The user should halt internal updates to the real time clock registers before reading clock data to prevent the reading of data in transition. Stopping the internal register updates does not affect clock accuracy.

Write a “1” to the read bit "R" (in the Flags register at 0x1FFF0) captures the current time in holding registers. Clock updates will not restart until a “0” is written to the read bit. The RTC registers can then be read while the internal clock continues to run.

Within 20ms after a “0” is written to the read bit, all real time clock registers are simultaneously updated.

Setting The Clock

Set the write bit “W” (in the Flags register at 0x1FFF0) to a "1" to enable the time to be set. The correct day, date and time can then be written into the real time clock registers in 24-hour BCD format. The time written is referred to as the "Base Time." This value is stored in nonvolatile registers and used in calculation of the current time. Reset the write bit to "0" to transfer the time to the actual clock counters. The clock starts counting at the new base time.

Backup Power

The RTC in intended to keep time even when system power is lost. When primary power, V_{CC}, drops below V_{SWITCH}, the real time clock switches to the backup power supply connected to either the V_{RTCcap} or V_{RTCbat} pin.

The clock oscillator uses a maximum of 300 nano amps at 2 volts to maximize the backup time available from the backup source.

You can power the real time clock with either a capacitor or a battery. Factors to be considered when choosing a backup power source include the expected duration of power outages and the cost and reliability trade-off of using a battery versus a capacitor.

If you select a capacitor power source, connect the capacitor to the V_{RTCcap} pin and leave the V_{RTCbat} pin unconnected. Capacitor backup time values based on maximum current specs are shown below. Nominal times are approximately three times longer.

Capacitor Value	Backup Time
0.1 F	72 hours
0.47 F	14 days
1.0 F	30 days

A capacitor has the obvious advantage of being more reliable and not containing hazardous materials. The capacitor is recharged every time the power is turned on so that real time clock continues to have the same backup time over years of operation.

If you select a battery power source, connect the battery to the V_{RTCbat} pin and leave the V_{RTCcap} pin unconnected. A 3V lithium battery is recommended for this application. The battery capacity should be chosen for the total anticipated cumulative down-time required over the life of the system.

The real time clock is designed with a diode internally connected to the V_{RTCbat} pin. This prevents the battery from ever being charged by the circuit.

Stopping And Starting The RTC Oscillator

The OSCEN bit in Calibration register at 0x1FFF8 enables RTC oscillator operation. This bit is nonvolatile and shipped to customers in the “enabled” state (set to 0). OSCEN should be set to a 1 to preserve battery life while the system is in storage. This turns off the oscillator circuit extending the battery life. If the OSCEN bit goes from disabled to enabled, it typically takes 5 seconds (10 seconds max) for the oscillator to start.

The STK17TA8 has the ability to detect oscillator failure due to loss of backup power. The failure is recorded by the OSCF (Oscillator Failed) bit of the Flags register (at address 0x1FFF0). When the device is powered on (V_{CC} goes above V_{SWITCH}), the OSCEN bit is checked for "enabled" status. If the OSCEN bit is enabled and the oscillator is not active within the first 5 ms, the OSCF bit is set. The user should check for this condition and then write a 0 to clear the flag. When the OSCF flag bit is set, the real time clock registers are reset to the “Base Time” (see the section "Setting the Clock"), the value last written to the real time clock registers.

The value of OSCF should be reset to 0 when the real time clock registers are written for the first time. This initializes the state of this bit which may have become set when the system was first powered on.

To reset OSCF, set the write bit “W” (in the Flags register at 0x1FFF0) to a "1" to enable writes to the Flag register. Write a “0” to the OSCF bit. and then reset the write bit to "0" to disable writes.

Calibrating The Clock

The RTC is driven by a quartz controlled oscillator with a nominal frequency of 32.768 KHz. Clock accuracy will depend on the quality of the crystal, specified (usually 35 ppm at 25 C). This error could equate to 1.53 minutes gain or loss per month. The STK17TA8 employs a calibration circuit that can improve the accuracy to +1/-2 ppm at 25 C. The calibration circuit adds or subtracts counts from the oscillator divider circuit.

The number of time pulses are added or substracted depends upon the value loaded into the five calibration bits found in Calibration register (at 0x1FFF8). Adding counts speeds the clock up; subtracting counts slows the clock down. The Calibration bits occupy the five lower order bits of the register. These bits can be set to represent any value between 0 and 31 in binary form. Bit D5 is a Sign bit, where a “1” indicates positive calibration and a “0” indicates negative calibration. Calibration occurs during a 64 minute period. The first 62 minutes in the cycle may, once per minute, have one second either shortened by 128 or lengthened by 256 oscillator cycles.

If a binary “1” is loaded into the register, only the first 2 minutes of the 64 minute cycle is modified; if a binary 6 is loaded, the first 12 will be affected, and so on. Therefore each calibration step has the effect of adding 512 or subtracting 256 oscillator cycles for every 125,829,120 actual oscillator cycles. That is +4.068 or -2.034 ppm of adjustment per calibration step in the calibration register.

The calibration register value is determined during system test by setting the CAL bit in the Flags register (at 0x1FFF0) to 1. This causes the INT pin to toggle at a nominal 512 Hz. This frequency can be measured with a frequency counter. Any deviation measured from the 512 Hz will indicate the degree and direction of the required correction. For example, a reading of 512.01024 Hz would indicate a +20 ppm error, requiring a -10 (001010) to be loaded into the Calibration register. Note that setting or changing the calibration register does not affect the frequency test output frequency.

To set or clear CAL, set the write bit “W” (in the Flags register at 0x1FFF0) to a "1" to enable writes to the Flag register. Write a value to CAL. and then reset the write bit to "0" to disable writes.

The default Calibration register value from the factory is 00h. The user calibration value loaded is retained during a power loss.

Alarm

The alarm function compares a user-programmable alarm time/date (stored in registers 0x1FFF1-5) with the real time clock time-of-day/date values. When a match occurs, the alarm flag (AF) is set and an interrupt is generated if the alarm interrupt is enabled. The alarm flag is automatically reset when the Flags register is read.

Each of the alarm registers has a match bit as its MSB. Setting the match bit to a 1 disables this alarm register from the alarm comparison. When the match bit is 0, the alarm register is compared with the equivalent real time clock register. Using the match bits, the alarm can occur as specifically as one particular second on one day of the month or as frequently as once per minute.

Note The product requires the match bit for seconds(1x1FFF2 - D7) be set to 0 for proper operation of the Alarm Flag and Interrupt.

The alarm value should be initialized on power up by software since the alarm registers are not nonvolatile.

To set or clear Alarm registers, set the write bit “W” (in the Flags register at 0x1FFF0) to a "1" to enable writes to the Alarm registers. Write an alarm value to the alarm registers and then reset the write bit to "0" to disable writes.

Watchdog Timer

The watchdog timer is designed to interrupt or reset the processor should the program get hung in a loop and not respond in a timely manner. The software must reload the watchdog timer before it counts down to zero to prevent this interrupt or reset.

The watchdog timer is a free running down counter that uses the 32 Hz clock (31.25 ms) derived from the crystal oscillator. The watchdog timer function does no operate unless the oscillator is running.

The watchdog counter is loaded with a starting value from the load register and then counts down to zero setting the watchdog flag (WDF) and generating an interrupt if the watchdog interrupt is enabled. The watchdog flag bit is reset when the flag register is read. The operating software would normally reload the counter by setting the watchdog strobe bit (WDS) to 1 within the timing interval programmed into the load register.

To use the watchdog timer to reset the processor on timeout, the INT is tied to processor master reset and Interrupt register is programmed to 24h to enable interrupts to pulse the reset pin on timeout.

To load the watch dog timer, set a new value into the load register by writing a “0” to the watchdog write bit (WDW) of the watchdog register (at 01x1FFF7). Then load a new value into the load register. Once the new value is loaded, the watchdog write bit is then set to 1 to disable watchdog writes. The watchdog strobe bit (WDS) is then set to 1 to load this value into the watchdog timer.

Note Setting the load register to zero disables the watchdog timer function.

The system software should initialize the watchdog load register on power up to the desired value since the register is not nonvolatile.

Power Monitor

The STK17TA8 provides a power monitor function. The power monitor is based on an internal band-gap reference circuit that compares the V_{CC} voltage to V_{SWITCH}.

When the power supply drops below V_{SWITCH}, the real time clock circuit is switched to the backup supply (battery or capacitor).

When operating from the backup source, no data may be read or written to the nvSRAM and the clock functions are not available to the user. The clock continues to operate in the background. Updated clock data is available to the user $t_{HRECALL}$ delay after VCC has been restored to the device.

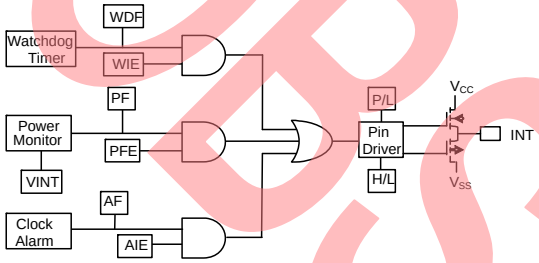
When power is lost, the PF flag in the Flags Register is set to indicate the power failure and an interrupt is generated if the power fail interrupt is enabled (interrupt register=20h). This line would normally be tied to the processor master reset input for perform power-off reset.

Interrupts

The STK17TA8 has a Flags register, Interrupt Register, and interrupt logic that can interrupt a microcontroller or generate a power up master reset signal. There are three potential interrupt sources: the watchdog timer, the power monitor, and the clock alarm. Each can be individually enabled to drive the INT pin by setting the appropriate bit in the Interrupt register. In addition, each has an associated flag bit in the Flags register that the host processor can read to determine the interrupt source. Two bits in the Interrupt register determine the operation of the INT pin driver.

A functional diagram of the interrupt logic is shown below:

Figure 16. Interrupt Block Diagram



Interrupt Register

Watchdog Interrupt Enable (WIE). When set to 1, the watchdog timer drives the INT pin when a watchdog time-out occurs. When WIE is set to 0, the watchdog time-out only sets the WDF flag bit.

Alarm Interrupt Enable (AIE). When set to 1, the INT pin is driven when an alarm match occurs. When set to 0, the alarm match only sets the AF flag bit.

Power Fail Interrupt Enable (PFE). When set to 1, the INT pin is driven by a power fail signal from the power monitor circuit. When set to 0, only the PF flag is set.

High/Low (H/L). When set to a 1, the INT pin is active high and the driver mode is push-pull. The INT pin can drive high only when V_{CC}>V_{SWITCH}. When set to a 0, the INT pin is active low and the drive mode is open-drain. The active low (open drain) output is maintained even when power is lost.

Pulse/Level (P/L). When set to a 1, the INT pin is driven for approximately 200 ms when an interrupt occurs. The pulse is reset when the Flags register is read. When P/L is set to a 0, the INT pin is driven high or low (determined by H/L) until the Flags register is read.

The Interrupt register is loaded with the default value 00h at the factory. The user should configure the Interrupt register to the value desired for their desired mode of operation. Once configured, the value is retained during power failures.

Flags Register

The Flags register has three flag bits: WDF, AF, and PF. These flags are set by the watchdog time-out, alarm match, or power fail monitor respectively. The processor can either poll this register or enable interrupts to be informed when a flag is set. The flags are automatically reset once the register is read.

The Flags register is automatically loaded with the value 00h on power up (with the exception of the OSCF bit).

RTC Register

Register	BCD Format Data								Function / Range
	D7	D6	D5	D4	D3	D2	D1	D0	
0x1FFFF	10s Years				Years				Years: 00-99
0x1FFFE	0	0	0	10s Months	Months				Months: 01-12
0x1FFFD	0	0	10s Day of Month		Day of Month				Day of Month: 01-31
0x1FFFC	0	0	0	0	0	Day of Week			Day of week: 01-07
0x1FFFB	0	0	10s Hours		Hours				Hours: 00-23
0x1FFFA	0	10s Minutes			Minutes				Minutes: 00-59
0x1FFF9	0	10s Seconds			Seconds				Seconds: 00-59
0x1FFF8	OSCEN [0]	0	Cal Sign	Calibration[00000]					Calibration values*
0x1FFF7	WDS	WDW	WDT						Watchdog*
0x1FFF6	WIE [0]	AIE [0]	PFE [0]	0	H/L [1]	P/L [0]	0	0	Interrupts*
0x1FFF5	M	0	10s Alarm Date		Alarm Day				Alarm, Day of Month: 01-31
0x1FFF4	M	0	10s Alarm Hours		Alarm Hours				Alarm, hours: 00-23
0x1FFF3	M	10 Alarm Minutes			Alarm Minutes				Alarm, minutes: 00-59
0x1FFF2	M	10 Alarm Seconds			Alarm Seconds				Alarm, seconds: 00-59
0x1FFF1	10s Centuries				Centuries				Centuries: 00-99
0x1FFF0	WDF	AF	PF	OSCF	0	CAL[0]	W[0]	R[0]	Flags*

***** A binary value, not a BCD value.

0 - Not implemented, reserved for future use.

Default Settings of nonvolatile Calibration and Interrupt registers from factory

Calibration Register=00h

Interrupt Register=00h

The User should configure to desired value at startup or during operation and the value is then retained during a power failure.

[ ] designates values shipped from the factory. See “Stopping And Starting The RTC Oscillator” on page 15.

Register Map Detail

0x1FFFF	Real Time Clock – Years							
	D7	D6	D5	D4	D3	D2	D1	D0
	10s Years				Years			
	Contains the lower two BCD digits of the year. Lower nibble contains the value for years; upper nibble contains the value for 10s of years. Each nibble operates from 0 to 9. The range for the register is 0-99.							
0x1FFFE	**Real Time Clock – Months**							
	D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
	0	0	0	10s Month	Months			
	Contains the BCD digits of the month. Lower nibble contains the lower digit and operates from 0 to 9; upper nibble (one bit) contains the upper digit and operates from 0 to 1. The range for the register is 1-12.							
0x1FFFD	**Real Time Clock – Date**							
	D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
	0	0	10s Day of month		Day of month			
	Contains the BCD digits for the date of the month. Lower nibble contains the lower digit and operates from 0 to 9; upper nibble contains the upper digit and operates from 0 to 3. The range for the register is 1-31. Leap years are automatically adjusted for.							
0x1FFFC	**Real Time Clock – Day**							
	D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
	0	0	0	0	0	Day of week		
	Lower nibble contains a value that correlates to day of the week. Day of the week is a ring counter that counts from 1 to 7 then returns to 1. The user must assign meaning to the day value, as the day is not integrated with the date.							
0x1FFFB	**Real Time Clock – Hours**							
	D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
	0	0	10s Hours		Hours			
	Contains the BCD value of hours in 24 hour format. Lower nibble contains the lower digit and operates from 0 to 9; upper nibble (two bits) contains the upper digit and operates from 0 to 2. The range for the register is 0-23.							
0x1FFFA	**Real Time Clock – Minutes**							
	D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
	0	10s Minutes			Minutes			
	Contains the BCD value of minutes. Lower nibble contains the lower digit and operates from 0 to 9; upper nibble contains the upper minutes digit and operates from 0 to 5. The range for the register is 0-59.							
0x1FFF9	**Real Time Clock – Seconds**							
	D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
	0	10s Seconds			Seconds			
	Contains the BCD value of seconds. Lower nibble contains the lower digit and operates from 0 to 9; upper nibble contains the upper digit and operates from 0 to 5. The range for the register is 0-59.							
0x1FFF8	**Calibration**							
	D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
	OSCEN	0	Calibration Sign	Calibration				
OSCEN	Oscillator Enable. When set to 1, the oscillator is disabled. When set to 0, the oscillator is enabled. Disabling the oscillator saves battery/capacitor power during storage.							
Calibration Sign	Determines if the calibration adjustment is applied as an addition (1) to or as a subtraction (0) from the time-base.							
Calibration	These five bits control the calibration of the clock.							

Register Map Detail (continued)

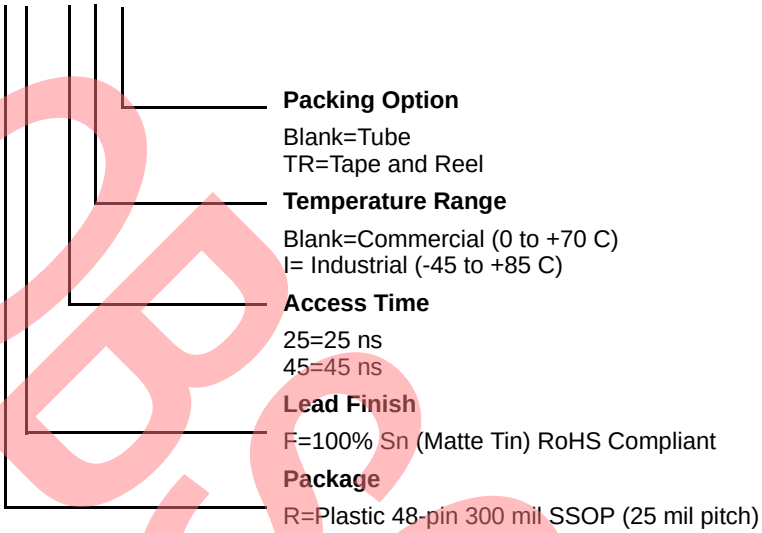
0x1FFF7	Watchdog Timer							
	D7	D6	D5	D4	D3	D2	D1	D0
	WDS	WDW	WDT					
WDS	Watchdog Strobe. Setting this bit to 1 reloads and restarts the watchdog timer. The bit is cleared automatically once the watchdog timer is reset. The WDS bit is write only. Reading it always will return a 0.							
WDW	Watchdog Write Enable. Set this bit to 1 to disable writing of the watchdog time-out value (WDT5-WDT0). This allows the user to strobe the watchdog stobe bit without disturbing the time-out value. Set this bit to 0 to allow bits 5-0 to be written.							
WDT	Watchdog time-out selection. The watchdog timer interval is selected by the 6-bit value in this register. It represents a multiplier of the 32 Hz count (31.25 ms). The range of time-out values is 31.25 ms (a setting of 1) to 2 seconds (setting of 3Fh). Setting the watchdog timer register to 0 disables the timer. These bits can be written only if the WDW bit was cleared to 0 on a previous cycle.							
0x1FFF6	**Interrupt**							
	D7	D6	D5	D4	D3	D2	D1	D0
	WIE	AIE	PFIE	ABE	H/L	P/L	0	0
WIE	Watchdog Interrupt Enable. When set to 1 and a watchdog time-out occurs, the watchdog timer drives the INT pin as well as setting the WDF flag. When set to 0, the watchdog time-out only sets the WDF flag.							
AIE	Alarm Interrupt Enable. When set to 1, the alarm match drives the INT pin as well as setting the AF flag. When set to 0, the alarm match only affects the AF flag.							
PFIE	Power-Fail Enable. When set to 1, a power failure drives the INT pin as well as setting the PF flag. When set to 0, the power failure only sets the PF flag.							
0	Reserved For Future Used							
H/L	High/Low. When set to a 1, the INT pin is driven active high. When set to 0, the INT pin is open drain, active low.							
P/L	Pulse/Level. When set to a 1, the INT pin is driven active (determined by H/L) by an interrupt source for approximately 200 ms. When set to a 0, the INT pin is driven to an active level (as set by H/L) until the Flags register is read.							
0x1FFF5	**Alarm – Day**							
	D7	D6	D5	D4	D3	D2	D1	D0
	M	0	10s Alarm Date		Alarm Date			
	Contains the alarm value for the date of the month and the mask bit to select or deselect the date value.							
M	Match. Setting this bit to 0 causes the date value to be used in the alarm match. Setting this bit to 1 causes the match circuit to ignore the date value.							
0x1FFF4	**Alarm – Hours**							
	D7	D6	D5	D4	D3	D2	D1	D0
	M	0	10s Alarm Hours		Alarm Hours			
	Contains the alarm value for the hours and the mask bit to select or deselect the hours value.							
M	Match. Setting this bit to 0 causes the hours value to be used in the alarm match. Setting this bit to 1 causes the match circuit to ignore the hours value.							
0x1FFF4	**Alarm – Hours**							
	D7	D6	D5	D4	D3	D2	D1	D0
	M	0	10s Alarm Hours		Alarm Hours			
	Contains the alarm value for the hours and the mask bit to select or deselect the hours value.							
M	Match. Setting this bit to 0 causes the hours value to be used in the alarm match. Setting this bit to 1 causes the match circuit to ignore the hours value.							

Register Map Detail (continued)

0x1FFF2	Alarm – Seconds							
	D7	D6	D5	D4	D3	D2	D1	D0
	M	10s Alarm Seconds			Alarm Seconds			
	Contains the alarm value for the seconds and the mask bit to select or deselect the seconds' value.							
M	Match. Setting this bit to 0 causes the seconds' value to be used in the alarm match. Setting this bit to 1 causes the match circuit to ignore the seconds value.							
0x1FFF1	**Real Time Clock – Centuries**							
	D7	D6	D5	D4	D3	D2	D1	D0
	10s Centuries				Centuries			
	Contains the BCD value of centuries. Lower nibble contains the lower digit and operates from 0 to 9; upper nibble contains the upper digit and operates from 0 to 9. The range for the register is 0-99 centuries.							
0x1FFF0	**Flags**							
	D7	D6	D5	D4	D3	D2	D1	D0
	WDF	AF	PF	OSCF	0	CAL	W	R
WDF	Watchdog Timer Flag. This read-only bit is set to 1 when the watchdog timer is allowed to reach 0 without being reset by the user. It is cleared to 0 when the Flags register is read or on power up.							
AF	Alarm Flag. This read-only bit is set to 1 when the time and date match the values stored in the alarm registers with the match bits = 0. It is cleared when the Flags register is read or on power up.							
PF	Power-fail Flag. This read-only bit is set to 1 when power falls below the power-fail threshold V_{SWITCH}. It is cleared to 0 when the Flags register is read or on power up.							
OSCF	Oscillator Fail Flag. Set to 1 on power up only if the oscillator is enabled and not running in the first 5ms of operation. This indicates that RTC backup power failed and clock value is no longer valid. The user must reset this bit to 0 to clear this condition.							
CAL	Calibration Mode. When set to 1, a 512Hz square wave is output on the INT pin. When set to 0, the INT pin resumes normal operation. This bit defaults to 0 (disabled) on power up.							
W	Write Enable. Setting the W bit to 1 freezes updates of the RTC registers and enables writes to RTC registers, Alarm registers, Calibration register, Interrupt register and Flags register. Setting the W bit to 0 causes the contents of the RTC registers to be transferred to the timekeeping counters if the time has been changed (a new base time is loaded). This bit defaults to 0 on power up.							
R	Read Time. Set R to 1 to captures the current time in holding registers so that clock updates are not seen during the reading process. Set R to 0 to enable the holding register to resume clock updates. This bit defaults to 0 on power up.							

Ordering Information

STK17TA8-R F 45 ITR



Packing Option
Blank=Tube
TR=Tape and Reel

Temperature Range
Blank=Commercial (0 to +70 C)
I= Industrial (-45 to +85 C)

Access Time
25=25 ns
45=45 ns

Lead Finish
F=100% Sn (Matte Tin) RoHS Compliant

Package
R=Plastic 48-pin 300 mil SSOP (25 mil pitch)

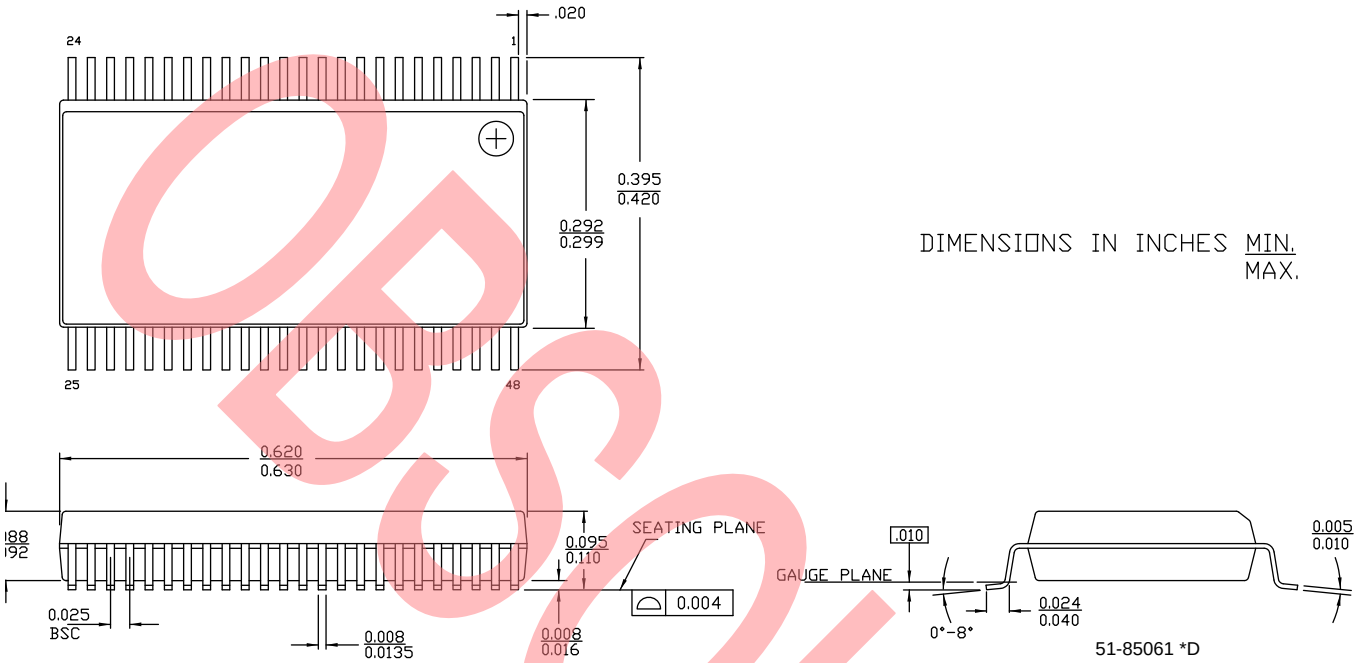
Ordering Codes

These parts are not recommended for new designs.

Ordering Code	Description	Access Times (ns)	Temperature
STK17TA8-RF25	3V 128Kx8 AutoStore nvSRAM+RTC SSOP48-300	25	Commercial
STK17TA8-RF45	3V 128Kx8 AutoStore nvSRAM+RTC SSOP48-300	45	Commercial
STK17TA8-RF25TR	3V 128Kx8 AutoStore nvSRAM+RTC SSOP48-300	25	Commercial
STK17TA8-RF45TR	3V 128Kx8 AutoStore nvSRAM+RTC SSOP48-300	45	Commercial
STK17TA8-RF25I	3.3V 128Kx8 AutoStore nvSRAM+RTC SSOP48-300	25	Industrial
STK17TA8-RF45I	3V 128Kx8 AutoStore nvSRAM+RTC SSOP48-300	45	Industrial
STK17TA8-RF25ITR	3.3V 128Kx8 AutoStore nvSRAM+RTC SSOP48-300	25	Industrial
STK17TA8-RF45ITR	3V 128Kx8 AutoStore nvSRAM+RTC SSOP48-300	45	Industrial

Package Diagrams

Figure 17. 48-Pin SSOP (51-85061)



Document History Page

Document Title: STK17TA8 128k X 8 AutoStore nvSRAM with Real Time Clock Document Number: 001-52039				
Rev.	**ECN No.**	**Orig. of Change**	**Submission Date**	**Description of Change**
**	2668660	GVCH/PYRS	03/04/2009	New Data Sheet
*A	2814390	GVCH	11/25/2009	Added note in the Ordering Information section mentioning that these parts are not recommended for new designs. Added “Not recommended for new designs” watermark in the PDF.
*B	2895330	GVCH	03/18/2010	Added foot note 1 for 25ns access speed. Updated Package Diagram 48 Pin SSOP. Updated Ordering Codes Description
*C	2902517	GVCH	03/31/2010	Added watermark "Not Recommended for New Designs" in pdf version. Move to external web.
*D	3185985	GVCH	03/02/2011	Obsolete datasheet

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