Data Sheet | October 30, 2007 | FN3142.8

Single 16 and 8/Differential 8-Channel and 4-Channel CMOS Analog Multiplexers

The HI-506/HI-507 and HI-508/HI-509 monolithic CMOS multiplexers each include an array of sixteen and eight analog switches respectively, a digital decoder circuit for channel selection, voltage reference for logic thresholds, and an enable input for device selection when several multiplexers are present. The Dielectric Isolation (DI) process used in fabrication of these devices eliminates the problem of latchup. DI also offers much lower substrate leakage and parasitic capacitance than conventional junction isolated CMOS (see Application Note AN520).

The switching threshold for each digital input is established by an internal +5V reference, providing a guaranteed minimum 2.4V for logic “1” and maximum 0.8V for logic “0”. This allows direct interface without pullup resistors to signals from most logic families: CMOS, TTL, DTL and some PMOS. For protection against transient overvoltage, the digital inputs include a series 200Ω resistor and diode clamp to each supply.

The HI-506 is a single 16-channel, the HI-507 is an 8-channel differential, the HI-508 is a single 8-channel and the HI-509 is a 4-channel differential multiplexer.

If input overvoltages are present, the HI-546/HI-547/HI-548/HI-549 multiplexers are recommended.

Features

- Pb-Free Available (RoHS Compliant) (See Ordering Info)
- Low ON Resistance 180Ω
- Wide Analog Signal Range . . . . . ±15V
- TTL/CMOS Compatible
- Access Time 250ns
- Maximum Power Supply 44V
- Break-Before-Make Switching
- No Latch-Up
- Replaces DG506A/DG506AA and DG507A/DG507AA
- Replaces DG508A/DG508AA and DG509A/DG509AA
- Pb-Free Available (RoHS Compliant)

Applications

- Data Acquisition Systems
- Precision Instrumentation
- Demultiplexing
- Selector Switch

Ordering Information

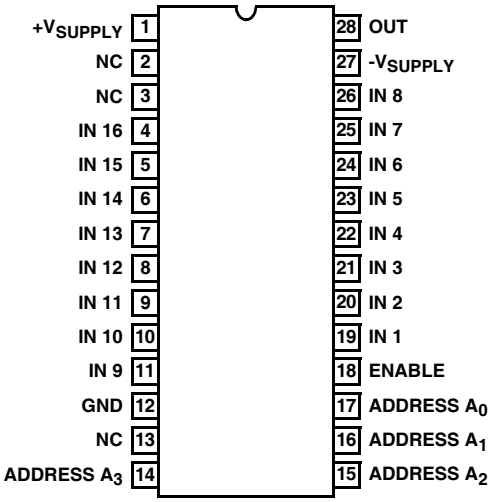
PART NUMBER	PART MARKING	TEMP. RANGE (°C)	PACKAGE	PKG. DWG. #
HI1-0506-2	HI1-506-2	-55 to +125	28 Ld CERDIP	F28.6
HI1-0506-5	HI1-506-5	0 to +75	28 Ld CERDIP	F28.6
HI4P0506-5	HI4P 506-5	0 to +75	28 Ld PLCC	N28.45
HI4P0506-5Z (Note 1)	HI4P 506-5Z	0 to +75	28 Ld PLCC (Pb-free)	N28.45
HI9P0506-5	HI9P506-5	0 to +75	28 Ld SOIC	M28.3
HI9P0506-9	HI9P506-9	-40 to +85	28 Ld SOIC	M28.3
HI9P0506-9Z (Note 1)	HI9P506-9Z	-40 to +85	28 Ld SOIC (Pb-free)	M28.3
HI1-0507-2	HI1-507-2	-55 to +125	28 Ld CERDIP	F28.6
HI3-0507-5	HI3-507-5	0 to +75	28 Ld PDIP	E28.6
HI3-0507-5Z	HI3-507-5Z	0 to +75	28 Ld PDIP (Note 3) (Pb-free)	E28.6
HI1-0508-2	HI1-508-2	-55 to 125	16 Ld CERDIP	F16.3
HI1-0508-5	HI1-508	0 to +75	16 Ld CERDIP	F16.3
HI3-0508-5	HI3-508-5	0 to +75	16 Ld PDIP	E16.3
HI3-0508-5Z (Note 1)	HI3-508-5Z	0 to +75	16 Ld PDIP (Note 3) (Pb-free)	E16.3
HI9P0508-5	HI9P508-5	0 to +75	16 Ld SOIC	M16.15
HI9P0508-5Z (Notes 1, 2)	HI9P508-5Z	0 to +75	16 Ld SOIC (Pb-free)	M16.15
HI9P0508-9	HI9P508-9	-40 to +85	16 Ld SOIC	M16.15
HI9P0508-9Z (Note 1)	HI9P508-9Z	-40 to +85	16 Ld SOIC (Pb-free)	M16.15
HI1-0509-2	HI1-509-2	-55 to +125	16 Ld CERDIP	F16.3
HI1-0509-4	HI1-509-4	-25 to +85	16 Ld CERDIP	F16.3
HI1-0509-5	HI1-509-5	0 to +75	16 Ld CERDIP	F16.3
HI3-0509-5	HI3-509-5	0 to +75	16 Ld PDIP	E16.3
HI4P0509-5	HI4P 509-5	0 to +75	20 Ld PLCC	N20.35
HI4P0509-5Z (Notes 1, 2)	HI4P 509-5Z	0 to +75	20 Ld PLCC (Pb-free)	N20.35
HI9P0509-5	HI9P 509-5	0 to +75	16 Ld SOIC	M16.15
HI9P0509-5Z (Notes 1, 2)	HI9P 509-5Z	0 to +75	16 Ld SOIC (Pb-free)	M16.15

NOTES:

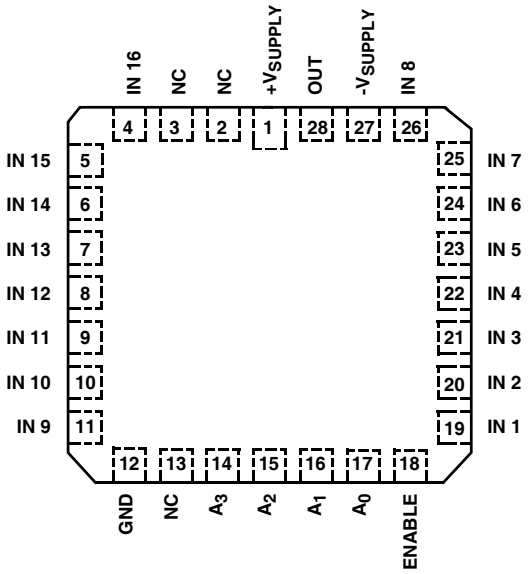
1. These Intersil Pb-free plastic packaged products employ special Pb-free material sets; molding compounds/die attach materials and 100% matte tin plate PLUS ANNEAL - e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
2. Add “96” suffix for tape and reel. Please refer to TB347 for details on reel specifications.
3. Pb-free PDIPs can be used for through hole wave solder processing only. They are not intended for use in Reflow solder processing applications.

Pinouts

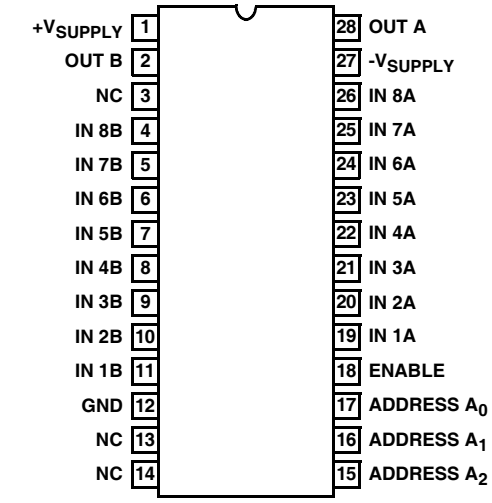
HI-506 (CERDIP, SOIC)
TOP VIEW



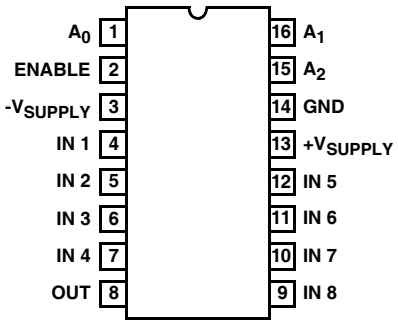
HI-506 (PLCC)
TOP VIEW



HI-507 (PDIP, CERDIP)
TOP VIEW

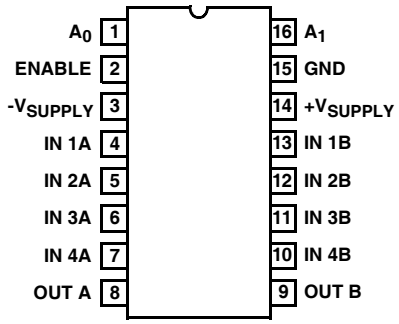


HI-508 (PDIP, CERDIP, SOIC)
TOP VIEW

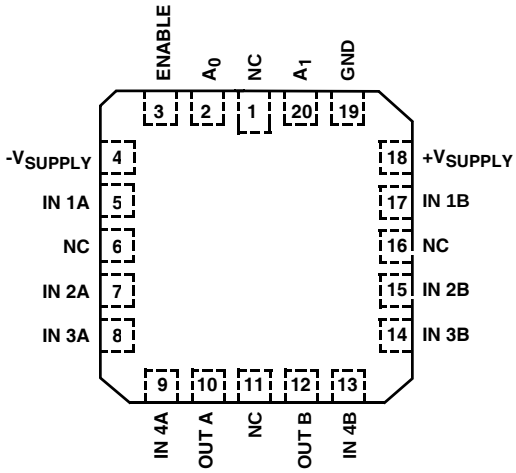


Pinouts (Continued)

HI-509 (PDIP, CERDIP, SOIC)
TOP VIEW



HI-509 (PLCC)
TOP VIEW



Truth Tables

HI-506

A_3	A_2	A_1	A_0	EN	"ON" CHANNEL
X	X	X	X	L	None
L	L	L	L	H	1
L	L	L	H	H	2
L	L	H	L	H	3
L	L	H	H	H	4
L	H	L	L	H	5
L	H	L	H	H	6
L	H	H	L	H	7
L	H	H	H	H	8
H	L	L	L	H	9
H	L	L	H	H	10
H	L	H	L	H	11
H	L	H	H	H	12
H	H	L	L	H	13
H	H	L	H	H	14
H	H	H	L	H	15
H	H	H	H	H	16

HI-507

A_2	A_1	A_0	EN	"ON" CHANNEL
X	X	X	L	None
L	L	L	H	1
L	L	H	H	2
L	H	L	H	3
L	H	H	H	4
H	L	L	H	5
H	L	H	H	6
H	H	L	H	7
H	H	H	H	8

HI-508

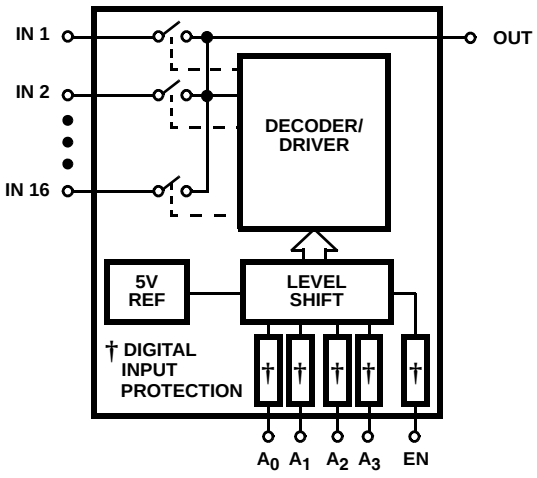
A_2	A_1	A_0	EN	"ON" CHANNEL
X	X	X	L	None
L	L	L	H	1
L	L	H	H	2
L	H	L	H	3
L	H	H	H	4
H	L	L	H	5
H	L	H	H	6
H	H	L	H	7
H	H	H	H	8

HI-509

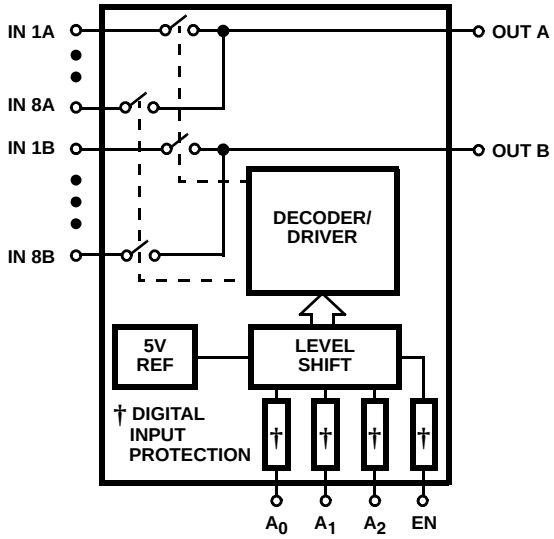
A_1	A_0	EN	"ON" CHANNEL PAIR
X	X	L	None
L	L	H	1
L	H	H	2
H	L	H	3
H	H	H	4

Functional Diagrams

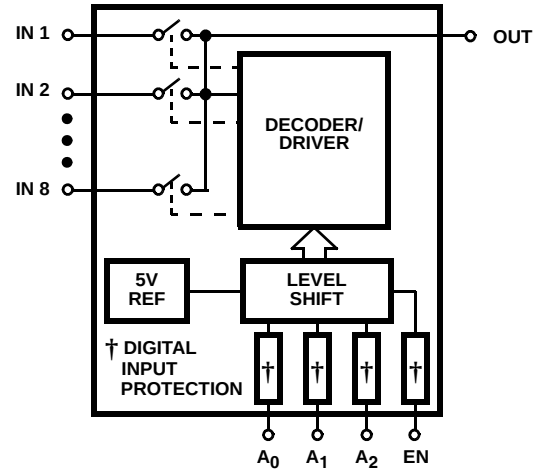
HI-506



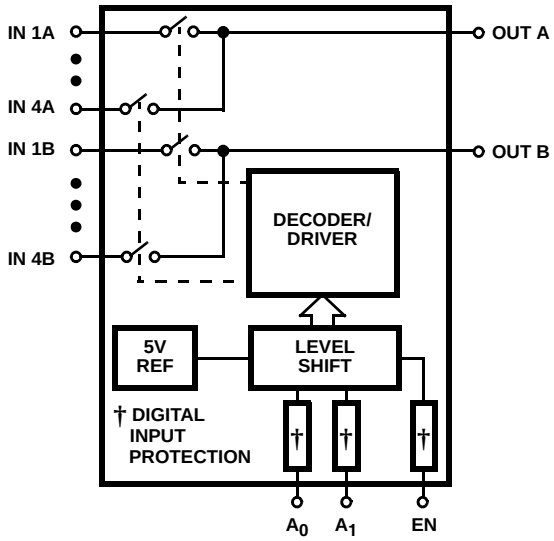
HI-507



HI-508

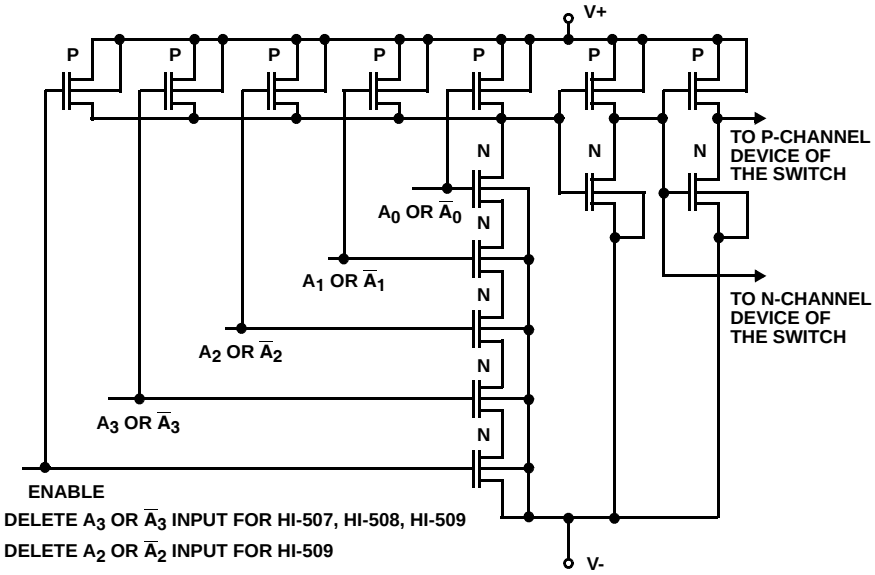


HI-509



Schematic Diagrams

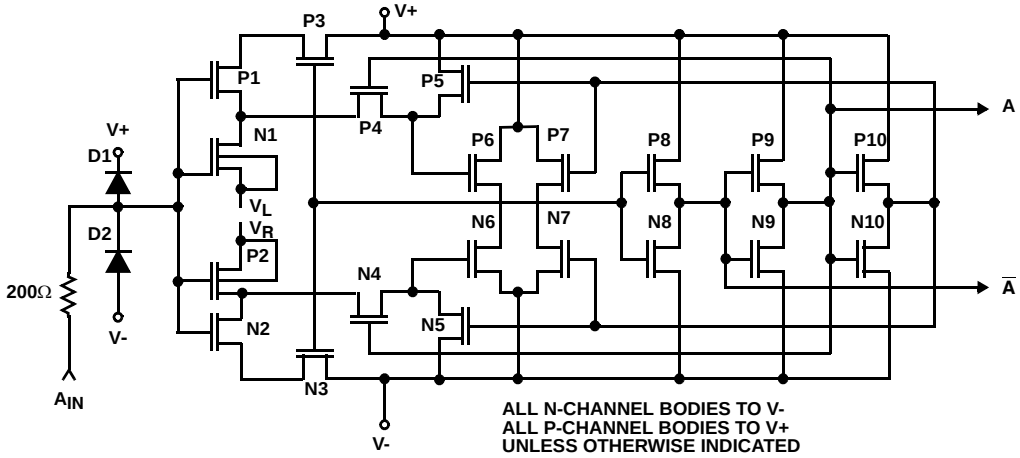
ADDRESS DECODER



DELETE A_3 OR $\bar{A}_3$ INPUT FOR HI-507, HI-508, HI-509

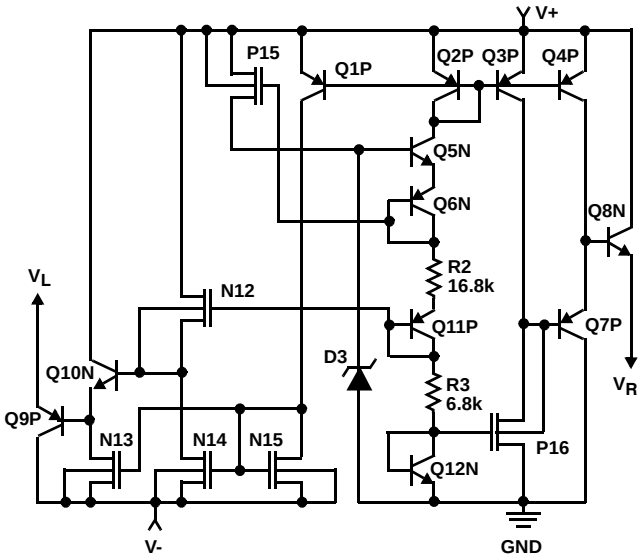
DELETE A_2 OR $\bar{A}_2$ INPUT FOR HI-509

ADDRESS INPUT BUFFER LEVEL SHIFTER

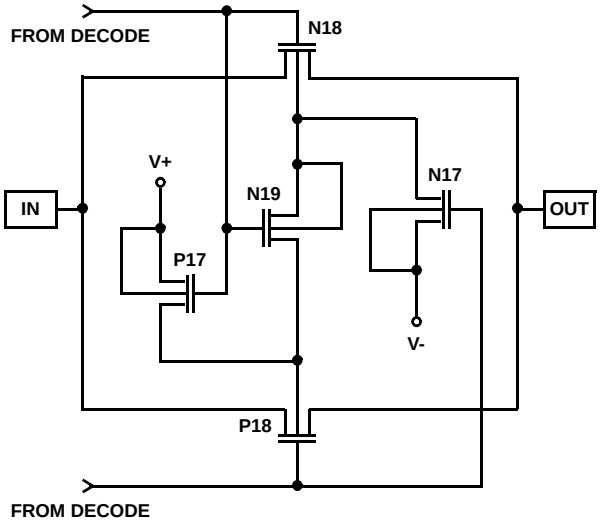


ALL N-CHANNEL BODIES TO V-
ALL P-CHANNEL BODIES TO V+
UNLESS OTHERWISE INDICATED

TTL REFERENCE CIRCUIT



MULTIPLEX SWITCH



Absolute Maximum Ratings

V+ to V- . . . . . +44V
V+ to GND . . . . . +22V
V- to GND. . . . . -25V
Digital Input Voltage (V_{EN}, V_A) . . . . . (V-) -4V to (V+) +4V or 20mA, Whichever Occurs First
Analog Signal (V_{IN}, V_{OUT}, Note 5) . . . . . (V-) -2V to (V+) +2V
Continuous Current, In or Out 20mA
Peak Current, In or Out (Pulsed 1ms, 10% Duty Cycle Max) . 40mA

Operating Conditions

Temperature Ranges
HI-50X-2. . . . . -55°C to +125°C
HI-50X-4. . . . . -25°C to +85°C
HI-50X-5. . . . . 0°C to +75°C
HI-50X-9. . . . . -40°C to +85°C
Typical Minimum Supply Voltage . . . . . ±10V or Single 20V

Thermal Information

Thermal Resistance (Typical, Note 4)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
16 Ld CERDIP Package.	85	32
16 Ld SOIC Package	115	N/A
16 Ld PDIP Package	100	N/A
20 Ld PLCC Package.	80	N/A
28 Ld CERDIP Package.	55	18
28 Ld PDIP Package	60	N/A
28 Ld SOIC Package	70	N/A
28 Ld PLCC Package.	70	N/A

Maximum Junction Temperature
Ceramic Packages . . . . . +175°C
Plastic Packages . . . . . +150°C
Maximum Storage Temperature Range . . . . . -65°C to +150°C
Pb-free reflow profile . . . . . .see link below
http://www.intersil.com/pbfree/Pb-FreeReflow.asp

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTE:

4. θ_{JA} is measured with the component mounted on a low effective thermal conductivity test board in free air. See Tech Brief TB379 for details.
5. Signals on IN or OUT exceeding V+ or V- are clamped by internal diodes. Limit resulting current to maximum current ratings. If an overvoltage condition is anticipated (analog input exceeds either power supply voltage), the Intersil HI-546/HI-547/HI-548/HI-549 multiplexers are recommended.

Electrical Specifications

Supplies = +15V, -15V; V_{AH} (Logic Level High) = 2.4V; V_{AL} (Logic Level Low) = 0.8V, Unless Otherwise Specified. For Test Conditions, Consult Test Circuits Section

PARAMETER	TEST CONDITIONS	TEMP (°C)	-2			-4, -5, -9			UNITS
			MIN (Note 11)	TYP	MAX	MIN (Note 11)	TYP	MAX	
DYNAMIC CHARACTERISTICS									
Access Time, t_A		25	-	250	500	-	250	-	ns
		Full	-	-	1000	-	-	1000	ns
Break-Before-Make Delay, t_{OPEN}		25	25	80	-	25	80	-	ns
Enable Delay (ON), $t_{ON(EN)}$		25	-	250	500	-	250	-	ns
		Full	-	-	1000	-	-	1000	ns
Enable Delay (OFF), $t_{OFF(EN)}$		25	-	250	500	-	250	-	ns
		Full	-	-	1000	-	-	1000	ns
Settling Time, t_S (HI-506 and HI-507)	To 0.1%	25	-	1.2	-	-	1.2	-	µs
	To 0.01%	25	-	2.4	-	-	2.4	-	µs
Settling Time, t_S (HI-508 and HI-509)	To 0.1%	25	-	360	-	-	360	-	ns
	To 0.01%	25	-	600	-	-	600	-	ns
Off Isolation	Note 9	25	-	68	-	-	68	-	dB
Channel Input Capacitance, $C_{S(OFF)}$		25	-	10	-	-	10	-	pF
Channel Output Capacitance, $C_{D(OFF)}$									
HI-506		25	-	52	-	-	52	-	pF
HI-507		25	-	30	-	-	30	-	pF
HI-508		25	-	17	-	-	17	-	pF
HI-509		25	-	12	-	-	12	-	pF
Digital Input Capacitance, C_A		25	-	6	-	-	6	-	pF
Input to Output Capacitance, $C_{DS(OFF)}$		25	-	0.08	-	-	0.08	-	pF
DIGITAL INPUT CHARACTERISTICS									
Input Low Threshold, V_{AL}		Full	-	-	0.8	-	-	0.8	V
Input High Threshold, V_{AH}		Full	2.4	-	-	2.4	-	-	V

Electrical Specifications Supplies = +15V, -15V; V_{AH} (Logic Level High) = 2.4V; V_{AL} (Logic Level Low) = 0.8V, Unless Otherwise Specified. For Test Conditions, Consult Test Circuits Section **(Continued)**

PARAMETER	TEST CONDITIONS	TEMP (°C)	-2			-4, -5, -9			UNITS
			MIN (Note 11)	TYP	MAX	MIN (Note 11)	TYP	MAX	
Input Leakage Current (High or Low), I_A	Note 8	Full	-	-	1.0	-	-	1.0	µA
ANALOG CHANNEL CHARACTERISTICS									
Analog Signal Range, V_{IN}		Full	-15	-	+15	-15	-	+15	V
On Resistance, r_{ON}	Note 6	25	-	180	300	-	180	400	Ω
Δr_{ON}, (Any Two Channels)		25	-	5	-	-	5	-	%
Off Input Leakage Current, $I_{S(OFF)}$	Note 7	25	-	0.03	-	-	0.03	-	nA
		Full	-	-	50	-	-	50	nA
Off Output Leakage Current, $I_{D(OFF)}$	Note 7	25	-	0.3	-	-	0.3	-	nA
HI-506		Full	-	-	300	-	-	300	nA
HI-507		Full	-	-	200	-	-	200	nA
HI-508		Full	-	-	200	-	-	200	nA
HI-509		Full	-	-	100	-	-	100	nA
On Channel Leakage Current, $I_{D(ON)}$	Note 7	25	-	0.3	-	-	0.3	-	nA
HI-506		Full	-	-	300	-	-	300	nA
HI-507		Full	-	-	200	-	-	200	nA
HI-508		Full	-	-	200	-	-	200	nA
HI-509		Full	-	-	100	-	-	100	nA
Differential Off Output Leakage Current, I_{DIFF} (HI-507, HI-509 Only)		Full	-	-	50	-	-	50	nA
POWER SUPPLY CHARACTERISTICS									
Current, I+									
HI-506/HI-507	Note 10	Full	-	1.5	3.0	-	1.5	3.0	mA
HI-508/HI-509	Note 10	Full	-	1.5	2.4	-	1.5	2.4	mA
Current, I-									
HI-506/HI-507	Note 10	Full	-	0.4	1.0	-	0.4	1.0	mA
HI-508/HI-509	Note 10	Full	-	0.4	1.0	-	0.4	1.0	mA
Power Dissipation, P_D									
HI-506/HI-507		Full	-	-	60	-	-	60	mW
HI-508/HI-509		Full	-	-	51	-	-	51	mW

NOTES:

6. V_{OUT} = ±10V, I_{OUT} = $\overline{+}$1mA.
7. 10nA is the practical lower limit for high speed measurement in the production test environment.
8. Digital input leakage is primarily due to the clamp diodes (see Schematic). Typical leakage is less than 1nA at +25°C.
9. V_{EN} = 0.8V, R_L = 1k, C_L = 15pF, V_S = $7V_{RMS}$, f = 100kHz.
10. V_{EN}, V_A = 0V or 2.4V.
11. Parts are 100% tested at +25°C. Over-temperature limits established by characterization and are not production tested.

Test Circuits and Waveforms T_A = +25°C, V_{SUPPLY} = ±15V, V_{AH} = 2.4V, V_{AL} = 0.8V, Unless Otherwise Specified

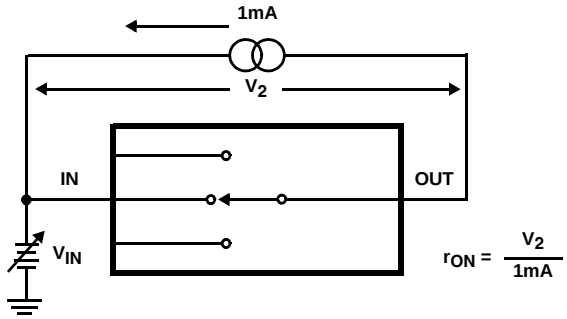


FIGURE 1A. TEST CIRCUIT

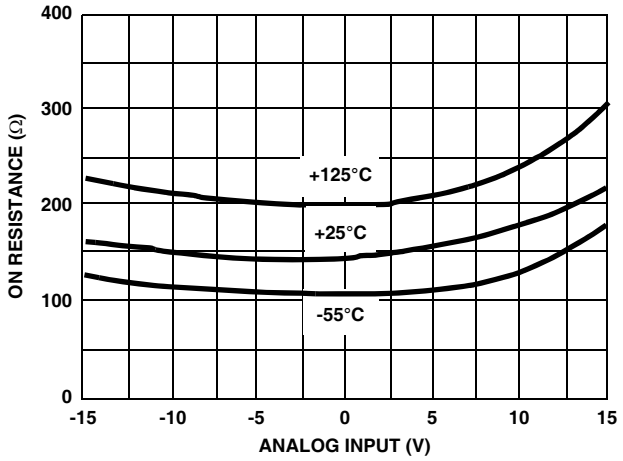


FIGURE 1B. ON RESISTANCE vs ANALOG INPUT VOLTAGE

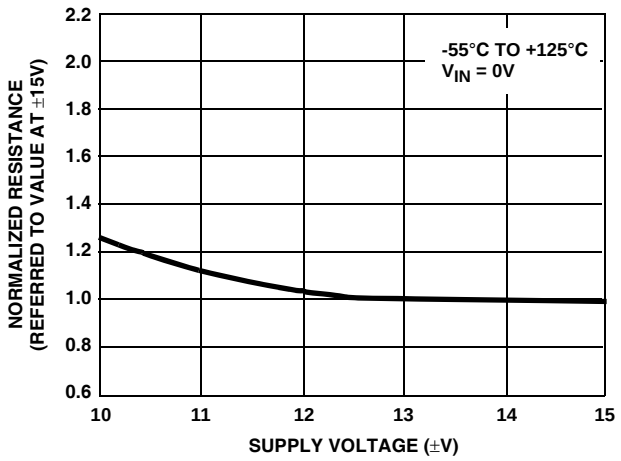


FIGURE 1C. NORMALIZED ON RESISTANCE vs SUPPLY VOLTAGE

FIGURE 1. ON RESISTANCE

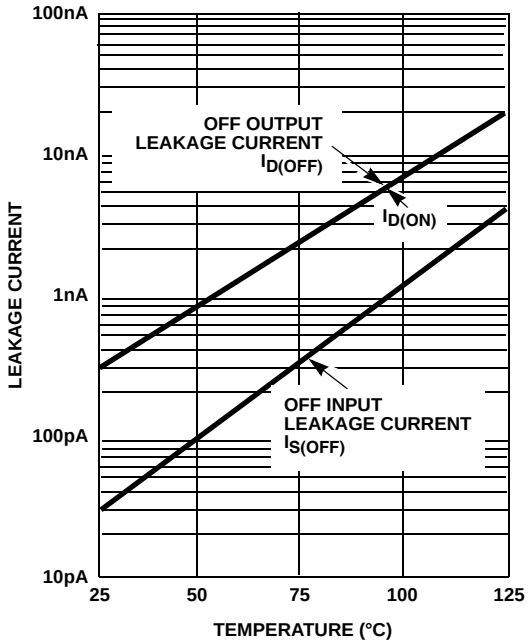


FIGURE 2A. LEAKAGE CURRENT vs TEMPERATURE

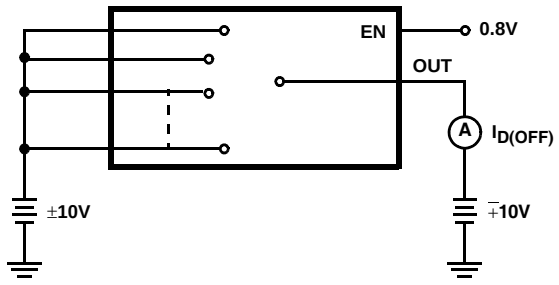


FIGURE 2B. $I_{D(OFF)}$ TEST CIRCUIT (NOTE 12)

Test Circuits and Waveforms T_A = +25°C, V_{SUPPLY} = ±15V, V_{AH} = 2.4V, V_{AL} = 0.8V, Unless Otherwise Specified **(Continued)**

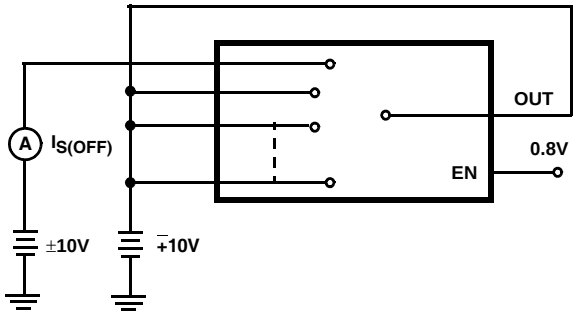


FIGURE 2C. $I_{S(OFF)}$ TEST CIRCUIT (NOTE 12)

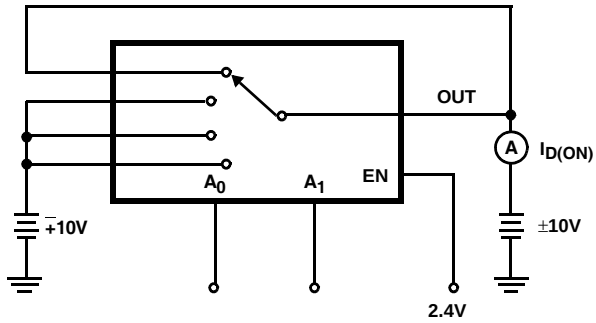


FIGURE 2D. $I_{D(ON)}$ TEST CIRCUIT (NOTE 12)

FIGURE 2. LEAKAGE CURRENTS

NOTE:

12. Two measurements per channel: ±10V and $\overline{+}$10V. (Two measurements per device for $I_{D(OFF)}$ ±10V and $\overline{+}$10V)

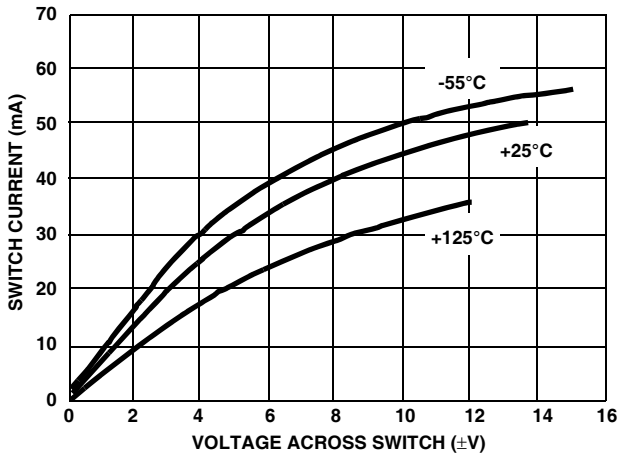


FIGURE 3A. ON CHANNEL CURRENT vs VOLTAGE

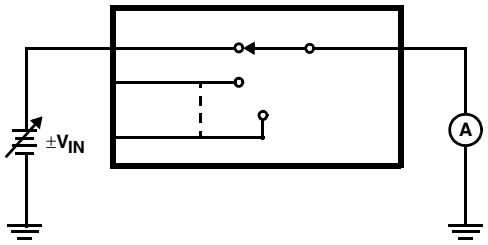


FIGURE 3B. TEST CIRCUIT

FIGURE 3. ON CHANNEL CURRENT

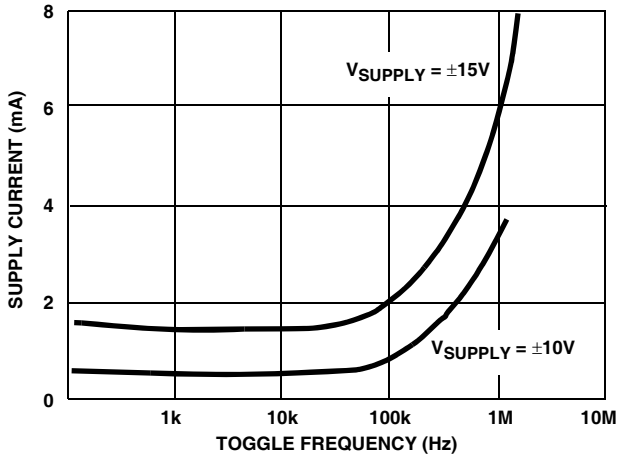


FIGURE 4A. SUPPLY CURRENT vs TOGGLE FREQUENCY

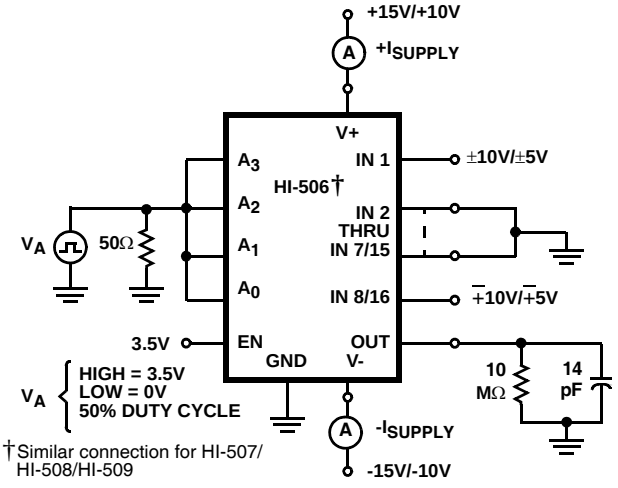


FIGURE 4B. TEST CIRCUIT

FIGURE 4. DYNAMIC SUPPLY CURRENT

Test Circuits and Waveforms T_A = +25°C, V_{SUPPLY} = ±15V, V_{AH} = 2.4V, V_{AL} = 0.8V, Unless Otherwise Specified **(Continued)**

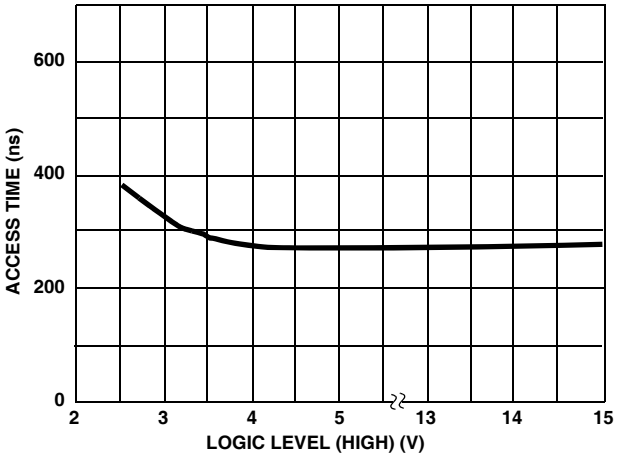
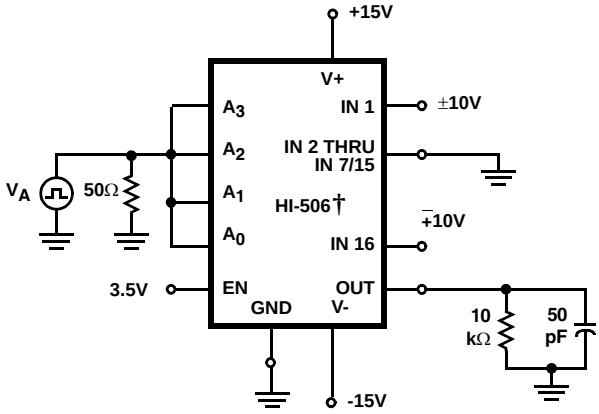


FIGURE 5A. ACCESS TIME vs LOGIC LEVEL (HIGH)



†Similar connection for HI-507/ HI-508/HI-509

FIGURE 5B. TEST CIRCUIT

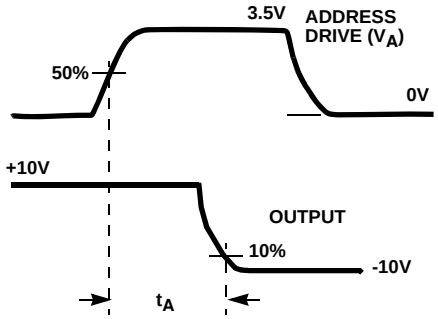


FIGURE 5C. MEASUREMENT POINTS

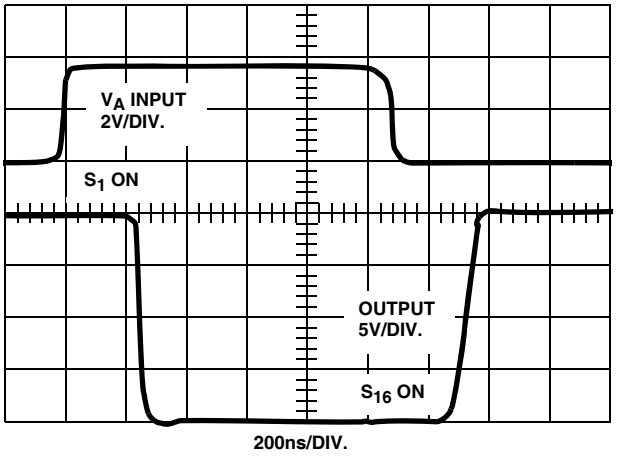
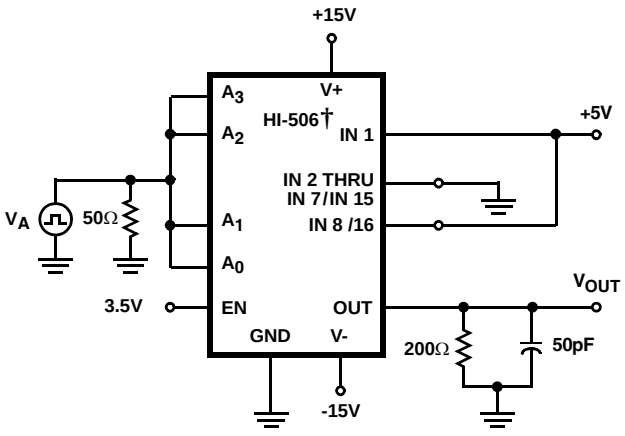


FIGURE 5D. WAVEFORMS

FIGURE 5. ACCESS TIME



†Similar connection for HI-507/HI-508/HI-509

FIGURE 6A. TEST CIRCUIT

Test Circuits and Waveforms T_A = +25°C, V_{SUPPLY} = ±15V, V_{AH} = 2.4V, V_{AL} = 0.8V, Unless Otherwise Specified **(Continued)**

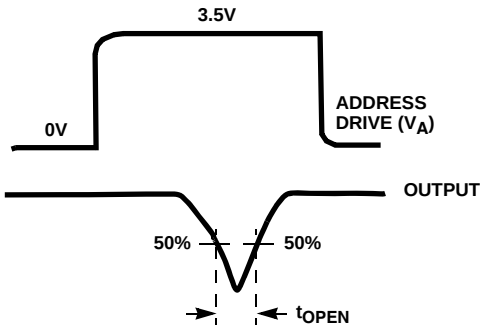


FIGURE 6B. MEASUREMENT POINTS

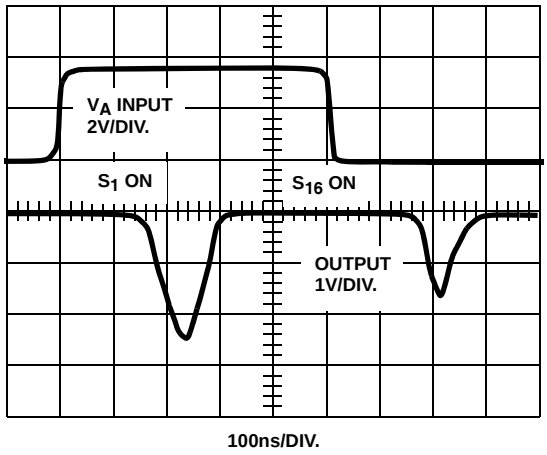
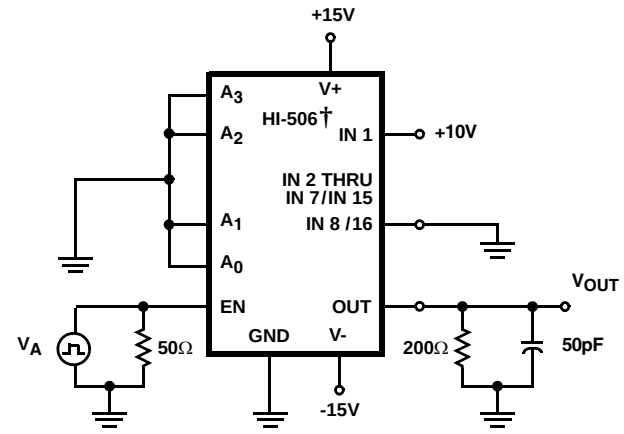


FIGURE 6C. WAVEFORMS

FIGURE 6. BREAK-BEFORE-MAKE DELAY



†Similar connection for HI-507/HI-508/HI-509

FIGURE 7A. TEST CIRCUIT

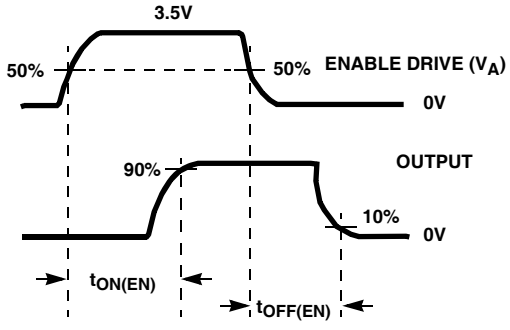


FIGURE 7B. MEASUREMENT POINTS

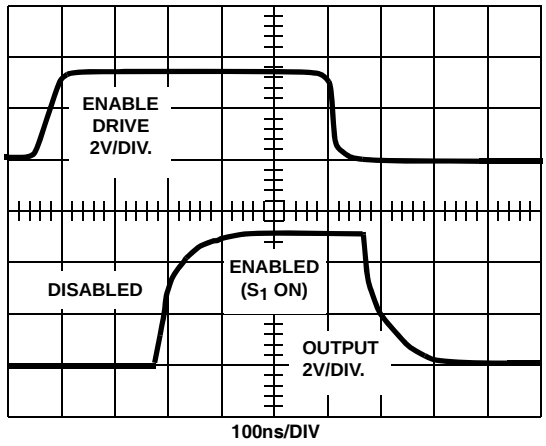


FIGURE 7C. WAVEFORMS

FIGURE 7. ENABLE DELAYS

Typical Performance Curves $T_A = 25°C$, $V_{SUPPLY} = \pm15V$, $V_{AH} = 2.4V$, $V_{AL} = 0.8V$, Unless Otherwise Specified

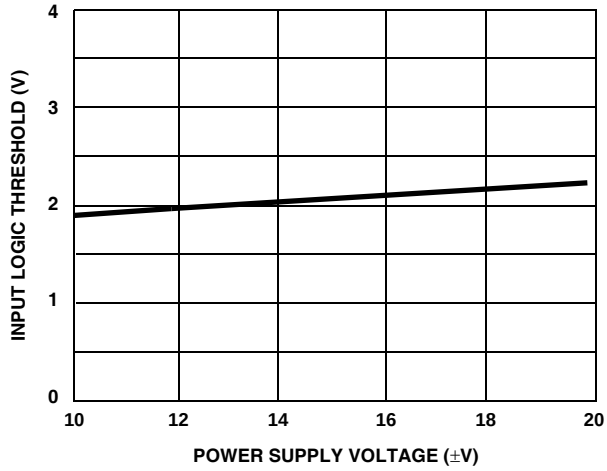


FIGURE 8. LOGIC THRESHOLD vs POWER SUPPLY VOLTAGE

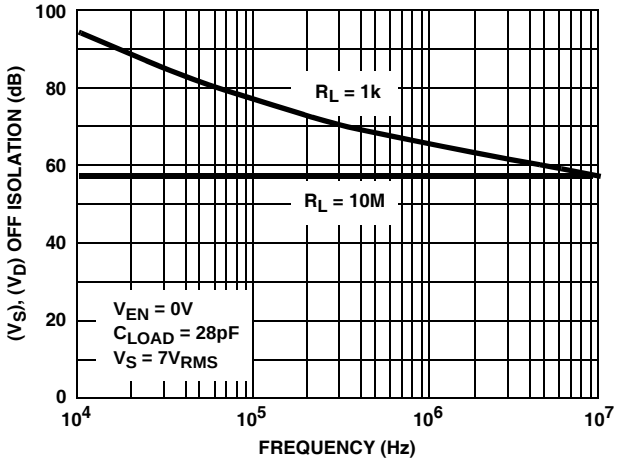


FIGURE 9. OFF ISOLATION vs FREQUENCY

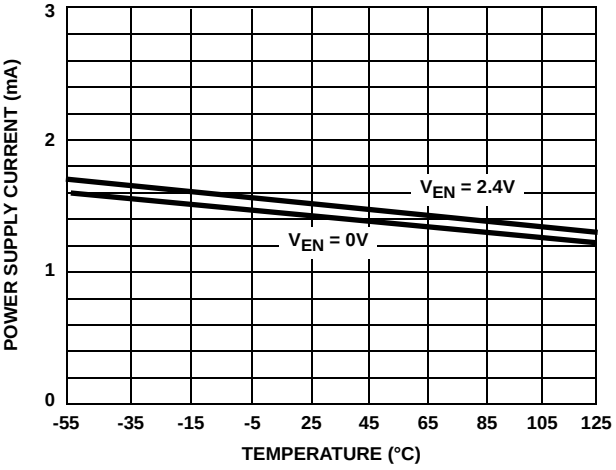


FIGURE 10A. HI-506/HI-507

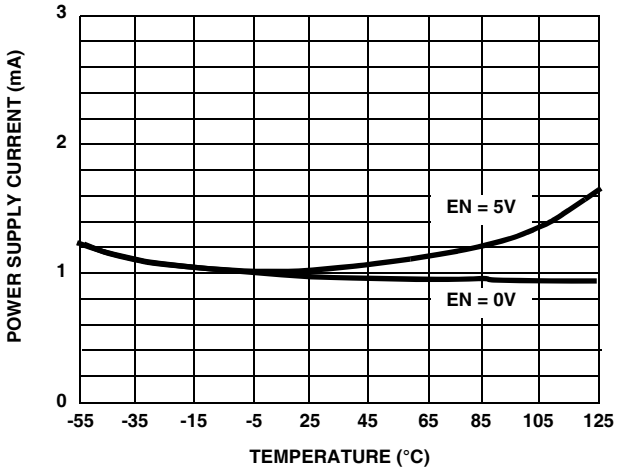


FIGURE 10B. HI-508/HI-509

FIGURE 10. POWER SUPPLY CURRENT vs TEMPERATURE

Die Characteristics

METALLIZATION:

Type: CuAl
Thickness: 16kÅ ±2kÅ

SUBSTRATE POTENTIAL (NOTE):

$-V_{SUPPLY}$

PASSIVATION:

Type: Nitride/Silox
Nitride Thickness: 3.5kÅ ±1kÅ
Silox Thickness: 12kÅ ±2kÅ

WORST CASE CURRENT DENSITY:

1.4×10^5 A/cm^2

TRANSISTOR COUNT:

421

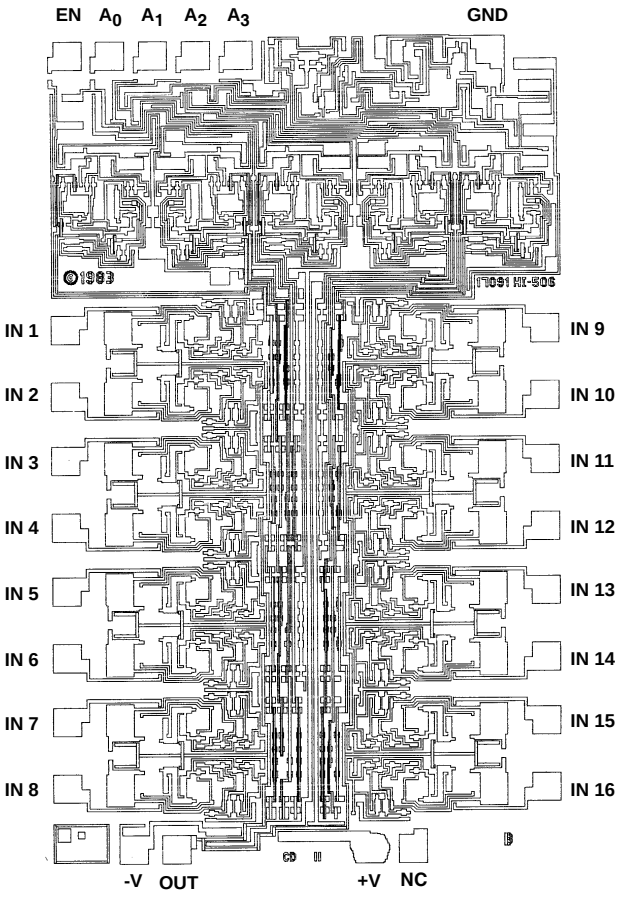
PROCESS:

CMOS-DI

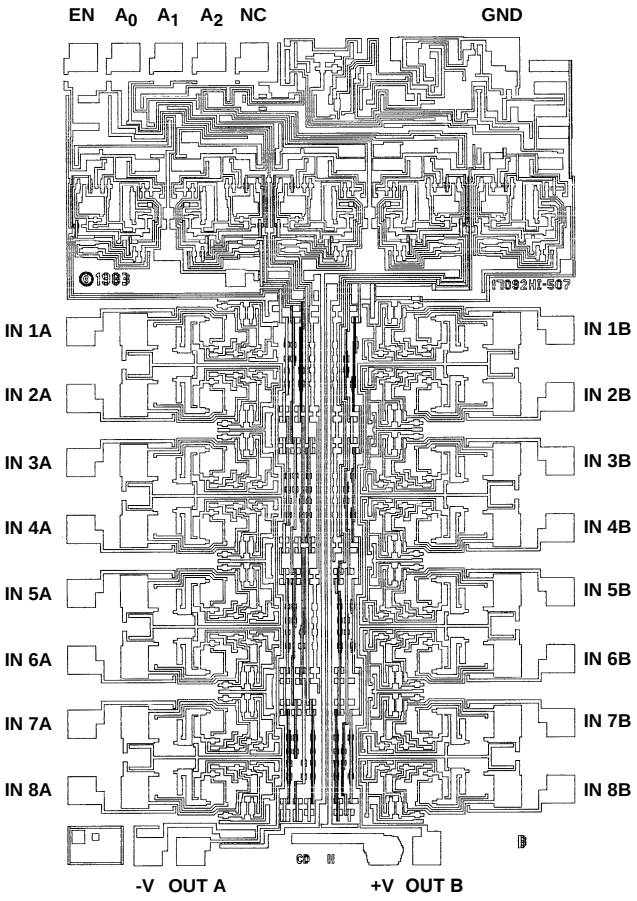
NOTE: The substrate appears resistive to the $-V_{SUPPLY}$ terminal, therefore it may be left floating (Insulating Die Mount) or it may be mounted on a conductor at $-V_{SUPPLY}$ potential.

Metallization Mask Layout

HI-506



HI-507



Die Characteristics

METALLIZATION:

Type: CuAl
Thickness: 16kÅ ±2kÅ

SUBSTRATE POTENTIAL (NOTE):

$-V_{SUPPLY}$

PASSIVATION:

Type: Nitride/Silox
Nitride Thickness: 3.5kÅ ±1kÅ
Silox Thickness: 12kÅ ±2kÅ

WORST CASE CURRENT DENSITY:

1.4×10^5 A/cm^2

TRANSISTOR COUNT:

234

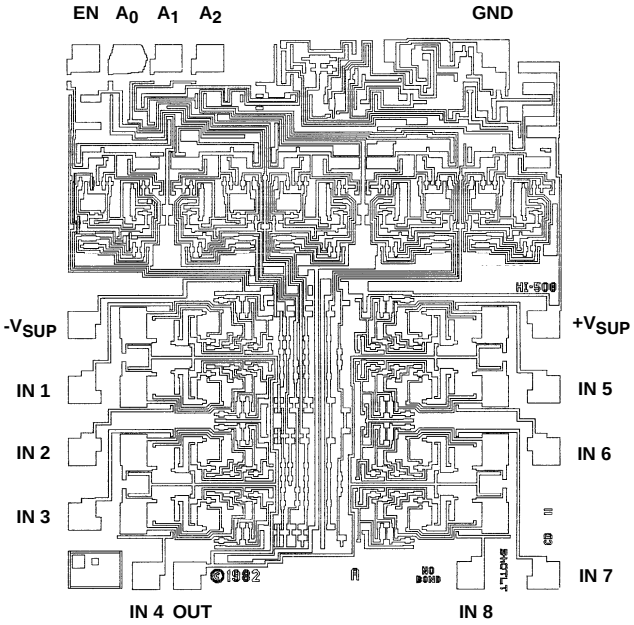
PROCESS:

CMOS-DI

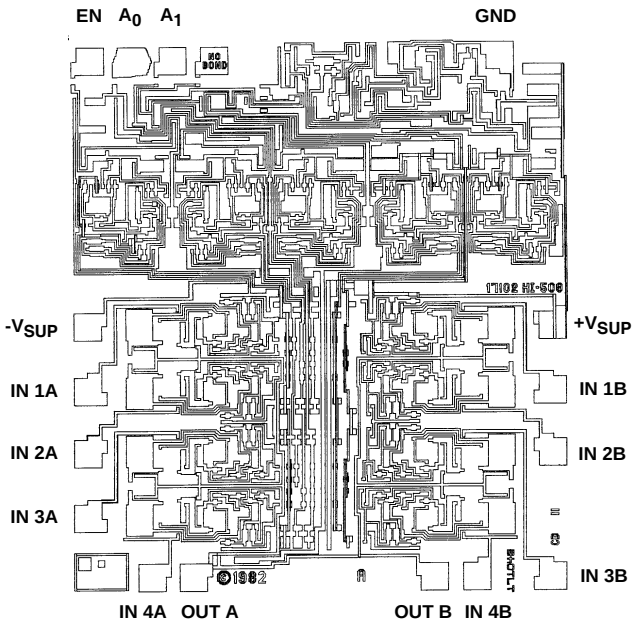
NOTE: The substrate appears resistive to the $-V_{SUPPLY}$ terminal, therefore it may be left floating (Insulating Die Mount) or it may be mounted on a conductor at $-V_{SUPPLY}$ potential.

Metallization Mask Layout

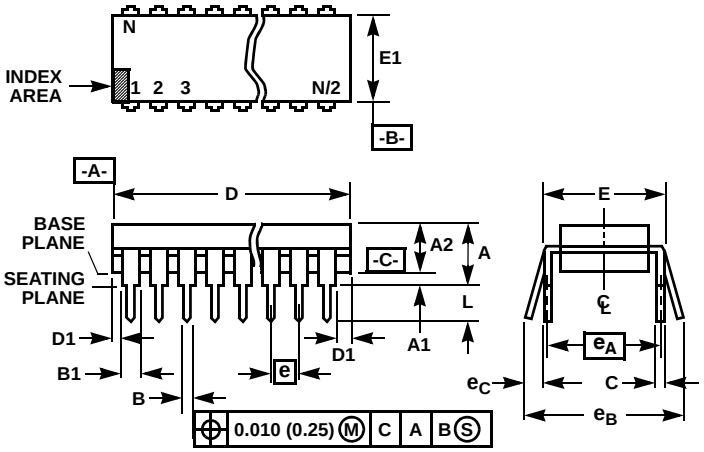
HI-508



HI-509



Dual-In-Line Plastic Packages (PDIP)



NOTES:

1. Controlling Dimensions: INCH. In case of conflict between English and Metric dimensions, the inch dimensions control.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Symbols are defined in the “MO Series Symbol List” in Section 2.2 of Publication No. 95.
4. Dimensions A, A1 and L are measured with the package seated in JEDEC seating plane gauge GS-3.
5. D, D1, and E1 dimensions do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.010 inch (0.25mm).
6. E and e_A are measured with the leads constrained to be perpendicular to datum -C-.
7. e_B and e_C are measured at the lead tips with the leads unconstrained. e_C must be zero or greater.
8. B1 maximum dimensions do not include dambar protrusions. Dambar protrusions shall not exceed 0.010 inch (0.25mm).
9. N is the maximum number of terminal positions.
10. Corner leads (1, N, N/2 and N/2 + 1) for E8.3, E16.3, E18.3, E28.3, E42.6 will have a B1 dimension of 0.030 - 0.045 inch (0.76 - 1.14mm).

E16.3 (JEDEC MS-001-BB ISSUE D)
16 LEAD DUAL-IN-LINE PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.210	-	5.33	4
A1	0.015	-	0.39	-	4
A2	0.115	0.195	2.93	4.95	-
B	0.014	0.022	0.356	0.558	-
B1	0.045	0.070	1.15	1.77	8, 10
C	0.008	0.014	0.204	0.355	-
D	0.735	0.775	18.66	19.68	5
D1	0.005	-	0.13	-	5
E	0.300	0.325	7.62	8.25	6
E1	0.240	0.280	6.10	7.11	5
e	0.100 BSC		2.54 BSC		-
e_A	0.300 BSC		7.62 BSC		6
e_B	-	0.430	-	10.92	7
L	0.115	0.150	2.93	3.81	4
N	16		16		9

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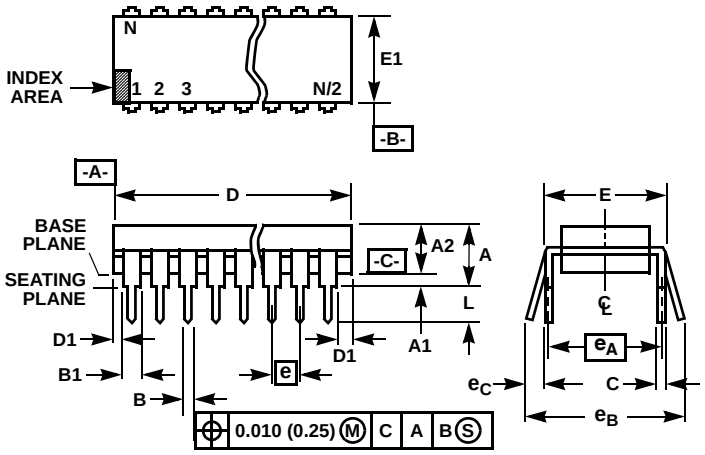
Dual-In-Line Plastic Packages (PDIP)



NOTES:

1. Controlling Dimensions: INCH. In case of conflict between English and Metric dimensions, the inch dimensions control.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Symbols are defined in the “MO Series Symbol List” in Section 2.2 of Publication No. 95.
4. Dimensions A, A1 and L are measured with the package seated in JEDEC seating plane gauge GS-3.
5. D, D1, and E1 dimensions do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.010 inch (0.25mm).
6. E and e_A are measured with the leads constrained to be perpendicular to datum -C-.
7. e_B and e_C are measured at the lead tips with the leads unconstrained. e_C must be zero or greater.
8. B1 maximum dimensions do not include dambar protrusions. Dambar protrusions shall not exceed 0.010 inch (0.25mm).
9. N is the maximum number of terminal positions.
10. Corner leads (1, N, N/2 and N/2 + 1) for E8.3, E16.3, E18.3, E28.3, E42.6 will have a B1 dimension of 0.030 - 0.045 inch (0.76 - 1.14mm).

E28.6 (JEDEC MS-011-AB ISSUE B)
28 LEAD DUAL-IN-LINE PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.250	-	6.35	4
A1	0.015	-	0.39	-	4
A2	0.125	0.195	3.18	4.95	-
B	0.014	0.022	0.356	0.558	-
B1	0.030	0.070	0.77	1.77	8
C	0.008	0.015	0.204	0.381	-
D	1.380	1.565	35.1	39.7	5
D1	0.005	-	0.13	-	5
E	0.600	0.625	15.24	15.87	6
E1	0.485	0.580	12.32	14.73	5
e	0.100 BSC		2.54 BSC		-
e_A	0.600 BSC		15.24 BSC		6
e_B	-	0.700	-	17.78	7
L	0.115	0.200	2.93	5.08	4
N	28		28		9

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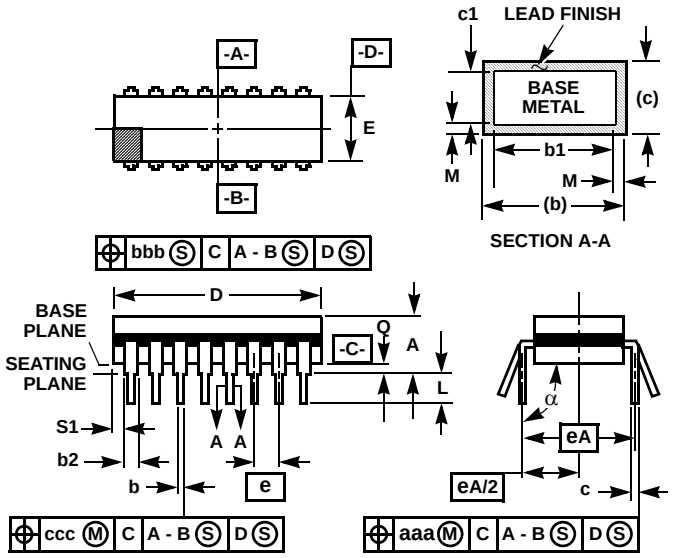
Ceramic Dual-In-Line Frit Seal Packages (CERDIP)



NOTES:

1. Index area: A notch or a pin one identification mark shall be located adjacent to pin one and shall be located within the shaded area shown. The manufacturer's identification shall not be used as a pin one identification mark.
2. The maximum limits of lead dimensions b and c or M shall be measured at the centroid of the finished lead surfaces, when solder dip or tin plate lead finish is applied.
3. Dimensions b1 and c1 apply to lead base metal only. Dimension M applies to lead plating and finish thickness.
4. Corner leads (1, N, N/2, and N/2+1) may be configured with a partial lead paddle. For this configuration dimension b3 replaces dimension b2.
5. This dimension allows for off-center lid, meniscus, and glass overrun.
6. Dimension Q shall be measured from the seating plane to the base plane.
7. Measure dimension S1 at all four corners.
8. N is the maximum number of terminal positions.
9. Dimensioning and tolerancing per ANSI Y14.5M - 1982.
10. Controlling dimension: INCH.

F16.3 MIL-STD-1835 GDIP1-T16 (D-2, CONFIGURATION A)
16 LEAD CERAMIC DUAL-IN-LINE FRIT SEAL PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.200	-	5.08	-
b	0.014	0.026	0.36	0.66	2
b1	0.014	0.023	0.36	0.58	3
b2	0.045	0.065	1.14	1.65	-
b3	0.023	0.045	0.58	1.14	4
c	0.008	0.018	0.20	0.46	2
c1	0.008	0.015	0.20	0.38	3
D	-	0.840	-	21.34	5
E	0.220	0.310	5.59	7.87	5
e	0.100 BSC		2.54 BSC		-
eA	0.300 BSC		7.62 BSC		-
eA/2	0.150 BSC		3.81 BSC		-
L	0.125	0.200	3.18	5.08	-
Q	0.015	0.060	0.38	1.52	6
S1	0.005	-	0.13	-	7
α	90^o	105^o	90^o	105^o	-
aaa	-	0.015	-	0.38	-
bbb	-	0.030	-	0.76	-
ccc	-	0.010	-	0.25	-
M	-	0.0015	-	0.038	2, 3
N	16		16		8

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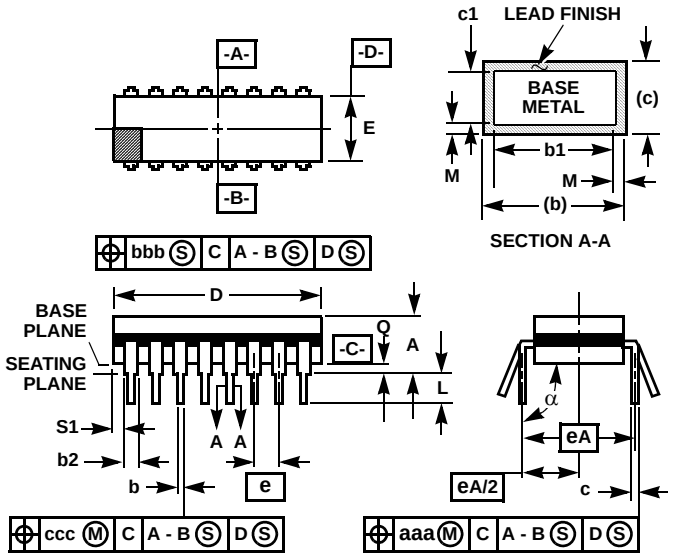
Ceramic Dual-In-Line Frit Seal Packages (CERDIP)



NOTES:

1. Index area: A notch or a pin one identification mark shall be located adjacent to pin one and shall be located within the shaded area shown. The manufacturer's identification shall not be used as a pin one identification mark.
2. The maximum limits of lead dimensions b and c or M shall be measured at the centroid of the finished lead surfaces, when solder dip or tin plate lead finish is applied.
3. Dimensions b1 and c1 apply to lead base metal only. Dimension M applies to lead plating and finish thickness.
4. Corner leads (1, N, N/2, and N/2+1) may be configured with a partial lead paddle. For this configuration dimension b3 replaces dimension b2.
5. This dimension allows for off-center lid, meniscus, and glass overrun.
6. Dimension Q shall be measured from the seating plane to the base plane.
7. Measure dimension S1 at all four corners.
8. N is the maximum number of terminal positions.
9. Dimensioning and tolerancing per ANSI Y14.5M - 1982.
10. Controlling dimension: INCH.

F28.6 MIL-STD-1835 GDIP1-T28 (D-10, CONFIGURATION A)
28 LEAD CERAMIC DUAL-IN-LINE FRIT SEAL PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.232	-	5.92	-
b	0.014	0.026	0.36	0.66	2
b1	0.014	0.023	0.36	0.58	3
b2	0.045	0.065	1.14	1.65	-
b3	0.023	0.045	0.58	1.14	4
c	0.008	0.018	0.20	0.46	2
c1	0.008	0.015	0.20	0.38	3
D	-	1.490	-	37.85	5
E	0.500	0.610	12.70	15.49	5
e	0.100 BSC		2.54 BSC		-
eA	0.600 BSC		15.24 BSC		-
eA/2	0.300 BSC		7.62 BSC		-
L	0.125	0.200	3.18	5.08	-
Q	0.015	0.060	0.38	1.52	6
S1	0.005	-	0.13	-	7
α	90^o	105^o	90^o	105^o	-
aaa	-	0.015	-	0.38	-
bbb	-	0.030	-	0.76	-
ccc	-	0.010	-	0.25	-
M	-	0.0015	-	0.038	2, 3
N	28		28		8

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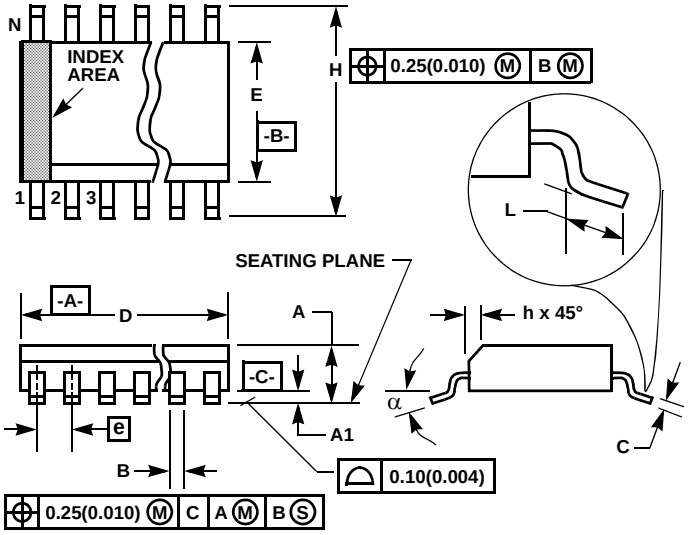
Small Outline Plastic Packages (SOIC)



NOTES:

1. Symbols are defined in the “MO Series Symbol List” in Section 2.2 of Publication Number 95.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Dimension “D” does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
4. Dimension “E” does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.25mm (0.010 inch) per side.
5. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
6. “L” is the length of terminal for soldering to a substrate.
7. “N” is the number of terminal positions.
8. Terminal numbers are shown for reference only.
9. The lead width “B”, as measured 0.36mm (0.014 inch) or greater above the seating plane, shall not exceed a maximum value of 0.61mm (0.024 inch).
10. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact.

M16.15 (JEDEC MS-012-AC ISSUE C)
16 LEAD NARROW BODY SMALL OUTLINE PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.0532	0.0688	1.35	1.75	-
A1	0.0040	0.0098	0.10	0.25	-
B	0.013	0.020	0.33	0.51	9
C	0.0075	0.0098	0.19	0.25	-
D	0.3859	0.3937	9.80	10.00	3
E	0.1497	0.1574	3.80	4.00	4
e	0.050 BSC		1.27 BSC		-
H	0.2284	0.2440	5.80	6.20	-
h	0.0099	0.0196	0.25	0.50	5
L	0.016	0.050	0.40	1.27	6
N	16		16		7
α	0°	8°	0°	8°	-

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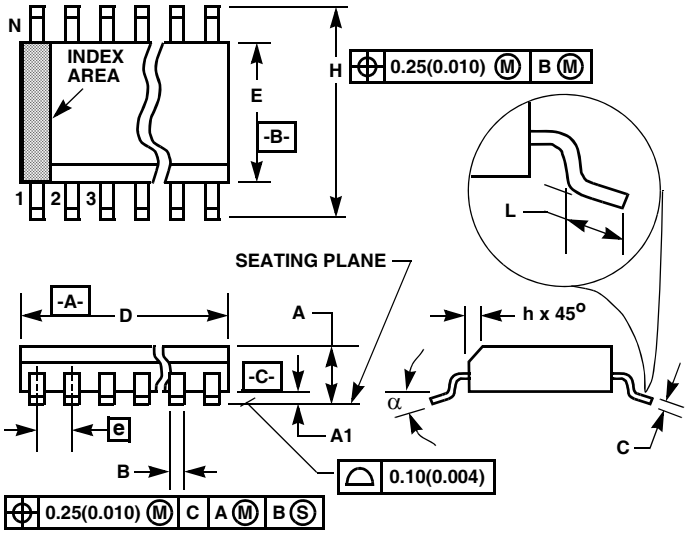
Small Outline Plastic Packages (SOIC)



NOTES:

1. Symbols are defined in the "MO Series Symbol List" in Section 2.2 of Publication Number 95.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Dimension "D" does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
4. Dimension "E" does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.25mm (0.010 inch) per side.
5. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
6. "L" is the length of terminal for soldering to a substrate.
7. "N" is the number of terminal positions.
8. Terminal numbers are shown for reference only.
9. The lead width "B", as measured 0.36mm (0.014 inch) or greater above the seating plane, shall not exceed a maximum value of 0.61mm (0.024 inch)
10. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact.

M28.3 (JEDEC MS-013-AE ISSUE C)
28 LEAD WIDE BODY SMALL OUTLINE PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.0926	0.1043	2.35	2.65	-
A1	0.0040	0.0118	0.10	0.30	-
B	0.013	0.0200	0.33	0.51	9
C	0.0091	0.0125	0.23	0.32	-
D	0.6969	0.7125	17.70	18.10	3
E	0.2914	0.2992	7.40	7.60	4
e	0.05 BSC		1.27 BSC		-
H	0.394	0.419	10.00	10.65	-
h	0.01	0.029	0.25	0.75	5
L	0.016	0.050	0.40	1.27	6
N	28		28		7
α	0^o	8^o	0^o	8^o	-

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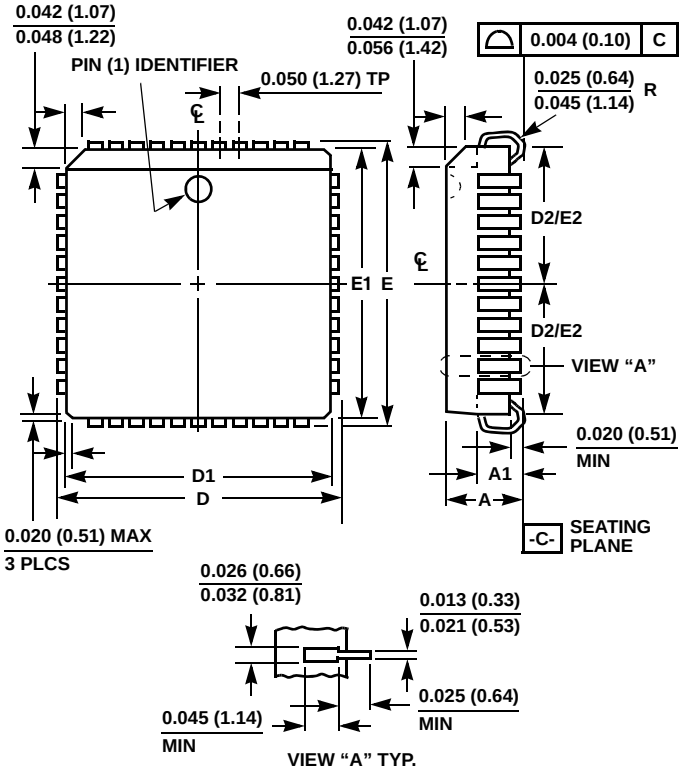
Plastic Leaded Chip Carrier Packages (PLCC)



N20.35 (JEDEC MS-018AA ISSUE A)
20 LEAD PLASTIC LEADED CHIP CARRIER PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.165	0.180	4.20	4.57	-
A1	0.090	0.120	2.29	3.04	-
D	0.385	0.395	9.78	10.03	-
D1	0.350	0.356	8.89	9.04	3
D2	0.141	0.169	3.59	4.29	4, 5
E	0.385	0.395	9.78	10.03	-
E1	0.350	0.356	8.89	9.04	3
E2	0.141	0.169	3.59	4.29	4, 5
N	20		20		6

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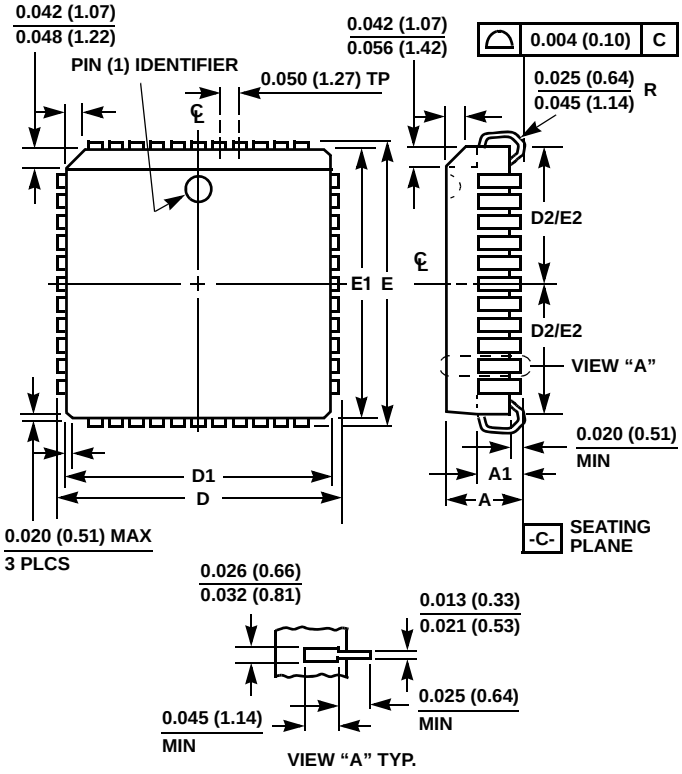
NOTES:

1. Controlling dimension: INCH. Converted millimeter dimensions are not necessarily exact.
2. Dimensions and tolerancing per ANSI Y14.5M-1982.
3. Dimensions D1 and E1 do not include mold protrusions. Allowable mold protrusion is 0.010 inch (0.25mm) per side. Dimensions D1 and E1 include mold mismatch and are measured at the extreme material condition at the body parting line.
4. To be measured at seating plane -C- contact point.
5. Centerline to be determined where center leads exit plastic body.
6. "N" is the number of terminal positions.

Plastic Leaded Chip Carrier Packages (PLCC)



N28.45 (JEDEC MS-018AB ISSUE A)
28 LEAD PLASTIC LEADED CHIP CARRIER PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.165	0.180	4.20	4.57	-
A1	0.090	0.120	2.29	3.04	-
D	0.485	0.495	12.32	12.57	-
D1	0.450	0.456	11.43	11.58	3
D2	0.191	0.219	4.86	5.56	4, 5
E	0.485	0.495	12.32	12.57	-
E1	0.450	0.456	11.43	11.58	3
E2	0.191	0.219	4.86	5.56	4, 5
N	28		28		6

Rev. 2 11/97

NOTES:

1. Controlling dimension: INCH. Converted millimeter dimensions are not necessarily exact.
2. Dimensions and tolerancing per ANSI Y14.5M-1982.
3. Dimensions D1 and E1 do not include mold protrusions. Allowable mold protrusion is 0.010 inch (0.25mm) per side. Dimensions D1 and E1 include mold mismatch and are measured at the extreme material condition at the body parting line.
4. To be measured at seating plane -C- contact point.
5. Centerline to be determined where center leads exit plastic body.
6. "N" is the number of terminal positions.