FINAL COM'L

AmPAL18P8B/AL/A/L

20-Pin Combinatorial TTL Programmable Array Logic

Advanced Micro Devices

DISTINCTIVE CHARACTERISTICS

- **As fast as 15 ns maximum propagation delay**
- **Universal combinatorial architecture**
- **Programmable output polarity**
- **Programmable replacement for high-speed TTL logic**
- **Extensive third-party software and programmer support through FusionPLD partners**
- **20-pin DIP and 20-pin PLCC packages save space**

GENERAL DESCRIPTION

The AmPAL18P8 utilizes Advanced Micro Devices' advanced oxide-isolated bipolar process and fuse-link technology. The devices provide user-programmable logic for replacing conventional SSI/MSI gates and flip-flops at a reduced chip count.

The AmPAL18P8 allows the systems engineer to implement the design on-chip, by opening fuse links to configure AND and OR gates within the device, according to the desired logic function. Complex interconnections between gates, which previously required time-consuming layout, are lifted from the PC board and placed on silicon, where they can be easily modified during prototyping or production.

The PAL device implements the familiar Boolean logic transfer function, the sum of products. The PAL device is a programmable AND array driving a fixed OR array. The AND array is programmed to create custom product terms, while the OR array sums selected terms at the outputs. In addition, the PAL device provides the following options:

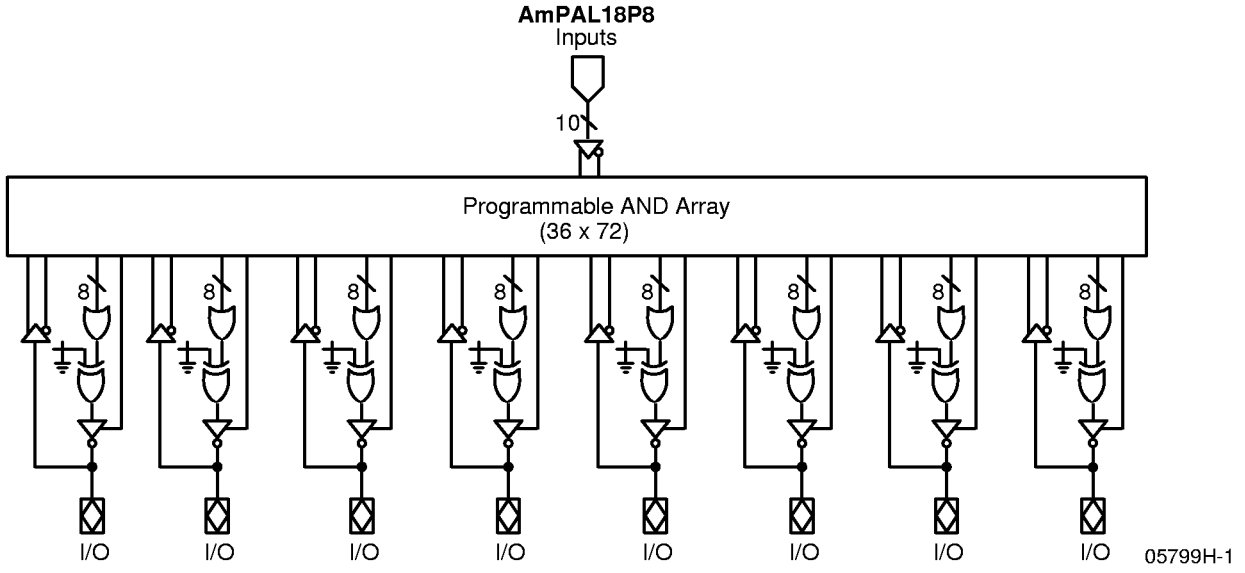
— Variable input/output pin ratio

— Programmable three-state outputs

Product terms with all fuses opened assume the logical HIGH state; product terms connected to both true and complement of any single input assume the logical LOW state. Unused input pins should be tied to V_{CC} or GND.

The entire PAL device family is supported by the FusionPLD partners. The PAL family is programmed on conventional PAL device programmers. Once the PAL device is programmed and verified an additional fuse may be opened to prevent pattern readout. This feature secures proprietary circuits.

BLOCK DIAGRAM



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Issue Date: February 1996

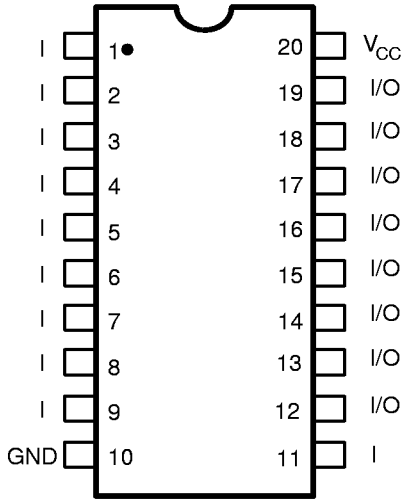
PRODUCT SELECTOR GUIDE

Family	t_{PD} ns (Max)	I_{CC} mA (Max)	I_{OL} mA (Min)
Very High-Speed ("B") Versions	15	180	24
High-Speed ("A") Versions	25	180	24
High-Speed, Half-Power ("AL") Versions	25	90	24
Half-Power ("L") Versions	35	90	24

CONNECTION DIAGRAMS

Top View

DIP



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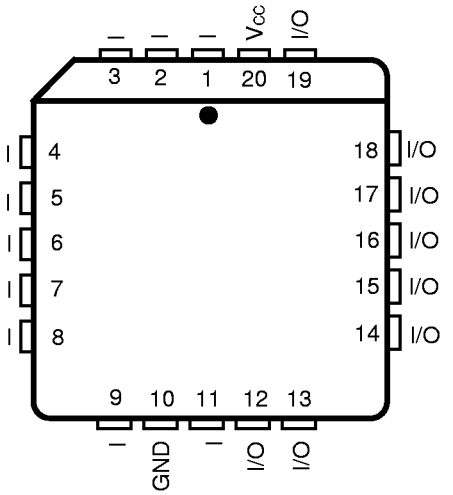
PLCC



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Note:
Pin 1 is marked for orientation.

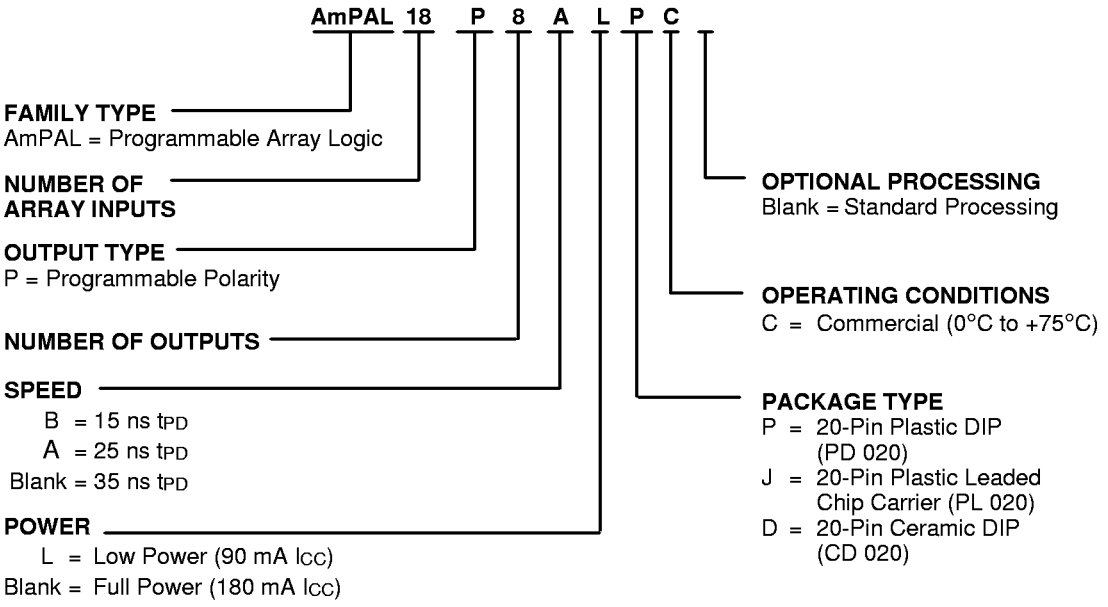
PIN DESIGNATIONS

GND = Ground
I = Input
I/O = Input/Output
V_{CC} = Supply Voltage

ORDERING INFORMATION

Commercial Products

AMD programmable logic products for commercial applications are available with several ordering options. The order number (Valid Combination) is formed by a combination of:



Valid Combinations		
AmPAL18P8	B, AL, A, L	PC, JC, DC

Valid Combinations

Valid Combinations lists configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations and to check on newly released combinations.

FUNCTIONAL DESCRIPTION

All parts are produced with a fuse link at each input to the AND gate array, and connections may be selectively removed by applying appropriate voltages to the circuit. Utilizing an easily-implemented programming algorithm, these products can be rapidly programmed to any customized pattern. Information on approved programmers can be found in the Programmer Reference Guide. Extra test words are pre-programmed during manufacturing to ensure extremely high field programming yields, and provide extra test paths to achieve excellent parametric correlation.

Variable Input/Output Pin Ratio

The AmPAL18P8 has ten dedicated input lines, and all eight combinatorial outputs are I/O pins. Buffers for device inputs have complementary outputs to provide user-programmable input signal polarity. Unused input pins should be tied to V_{CC} or GND.

Programmable Three-State Outputs

Each output has a three-state output buffer with three-state control. A product term controls the buffer, allowing enable and disable to be a function of any product of device inputs or output feedback. The combinatorial output provides a bidirectional I/O pin, and may be configured as a dedicated input if the buffer is always disabled.

Programmable Polarity

The polarity of each output can be active-high or active-low, either to match output signal needs or to reduce product terms. Programmable polarity allows Boolean expressions to be written in their most compact form (true or inverted), and the output can still be of the desired polarity. It can also save "DeMorganizing" efforts.

Selection is through a programmable fuse which controls an exclusive-OR gate at the output of the AND/OR logic. The output is active high if the fuse is 1 (programmed) and active low if the fuse is 0 (intact).

Security Fuse

After programming and verification, an AmPAL18P8 design can be secured by programming the security fuse. Once programmed, this fuse defeats readback of the internal programmed pattern by a device programmer, securing proprietary designs from competitors. When the security fuse is programmed, the array will read as if every fuse is programmed.

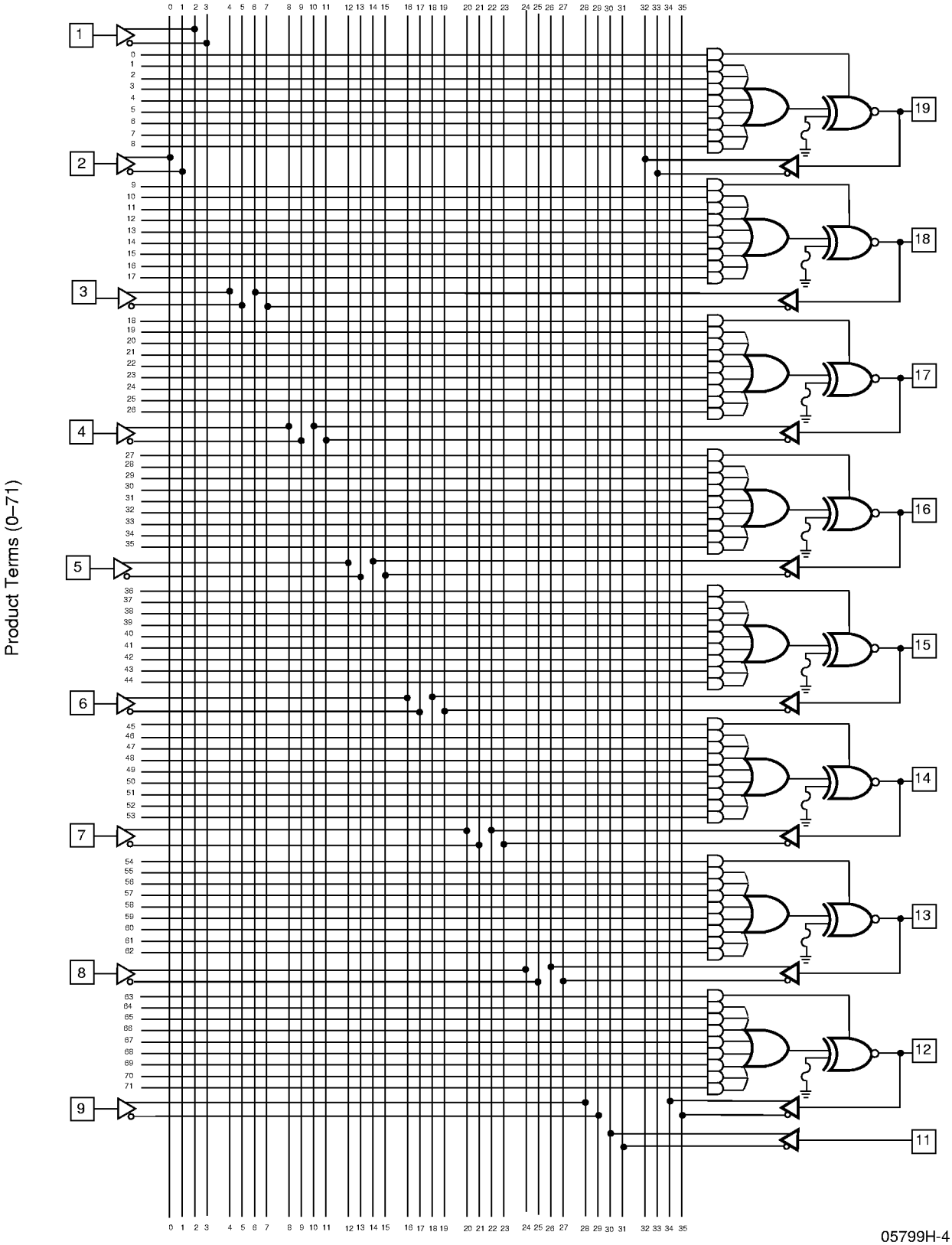
Quality and Testability

The AmPAL18P8 offers a very high level of built-in quality. Extra programmable fuses provide a means of verifying performance of all AC and DC parameters. In addition, this verifies complete programmability and functionality of the device to provide the highest programming yields and post-programming functional yields in the industry.

Technology

The AmPAL18P8 is fabricated with AMD's diffusion-isolated bipolar process. This process reduces parasitic capacitances and minimum geometries to provide higher performance. The array connections are formed with proven PtSi fuses for reliable operation.

LOGIC DIAGRAM



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ABSOLUTE MAXIMUM RATINGS

Storage Temperature . . . . . –65°C to +150°C

Ambient Temperature
With Power Applied . . . . . –55°C to +125°C

Supply Voltage with
Respect to Ground . . . . . –0.5 V to +7.0 V

DC Input Voltage . . . . . –0.5 V to +5.5 V

DC Input Current . . . . . –30 mA to +5 mA

DC I/O Pin Voltage . . . . . –0.5 V to V_{CC} Max

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability. Programming conditions may differ.

OPERATING RANGES

Commercial (C) Devices

Ambient Temperature (T_A)
Operating in Free Air . . . . . 0°C to +75°C

Supply Voltage (V_{CC})
with Respect to Ground . . . . . +4.75 V to +5.25 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over COMMERCIAL operating ranges unless otherwise specified

Parameter Symbol	Parameter Description	Test Conditions		Min	Max	Unit
V_{OH}	Output HIGH Voltage	I_{OH} = –3.2 mA V_{IN} = V_{IH} or V_{IL} V_{CC} = Min		2.4		V
V_{OL}	Output LOW Voltage	I_{OL} = 24 mA V_{IN} = V_{IH} or V_{IL} V_{CC} = Min			0.5	V
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for all Inputs (Note 1)		2.0		V
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for all Inputs (Note 1)			0.8	V
V_I	Input Clamp Voltage	I_{IN} = –18 mA, V_{CC} = Min			–1.2	V
I_{IH}	Input HIGH Current	V_{IN} = 2.7 V, V_{CC} = Max (Note 2)			25	µA
I_{IL}	Input LOW Current	V_{IN} = 0.4 V, V_{CC} = Max (Note 2)			–100	µA
I_I	Maximum Input Current	V_{IN} = 5.5 V, V_{CC} = Max			1	mA
I_{OZH}	Off-State Output Leakage Current HIGH	V_{OUT} = 2.7 V, V_{CC} = Max V_{IN} = V_{IH} or V_{IL} (Note 2)			100	µA
I_{OZL}	Off-State Output Leakage Current LOW	V_{OUT} = 0.4 V, V_{CC} = Max V_{IN} = V_{IH} or V_{IL} (Note 2)			–250	µA
I_{SC}	Output Short-Circuit Current	V_{OUT} = 0.5 V, V_{CC} = Max (Note 3)		–30	–90	mA
I_{CC}	Supply Current	V_{IN} = 0 V, Outputs Open (I_{OUT} = 0 mA) V_{CC} = Max	B, A		180	mA
			AL		90	mA

Notes:

1. *These are absolute values with respect to device ground and all overshoots due to system and/or tester noise are included.*
2. *I/O pin leakage is the worst case of I_{IL} and I_{OZL} (or I_{IH} and I_{OZH}).*
3. *Not more than one output should be shorted at a time. Duration of the short-circuit should not exceed one second. V_{OUT} = 0.5 V has been chosen to avoid test problems caused by tester ground degradation.*

CAPACITANCE (Note 1)

Parameter Symbol	Parameter Description	Test Conditions		Typ	Unit
C_{IN}	Input Capacitance	V_{IN} = 2.0 V	V_{CC} = 5.0 V T_A = +25°C f = 1 MHz	6	pF
C_{OUT}	Output Capacitance	V_{OUT} = 2.0 V		9	

Note:

1. *These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where capacitance may be affected.*

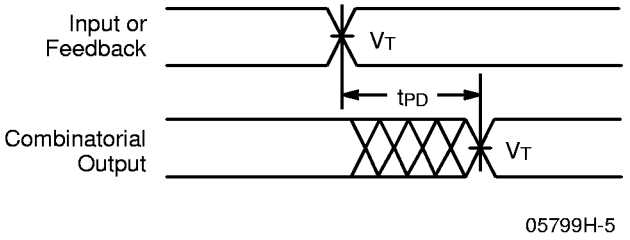
SWITCHING CHARACTERISTICS over COMMERCIAL operating ranges (Note 2)

Parameter Symbol	Parameter Description	B		A, AL		L		Unit
		Min	Max	Min	Max	Min	Max	
t_{PD}	Input or Feedback to Combinatorial Output		15		25		35	ns
t_{EA}	Input to Output Enable Using Product Term Control		15		25		35	ns
t_{ER}	Input to Output Disable Using Product Term Control		15		25		35	ns

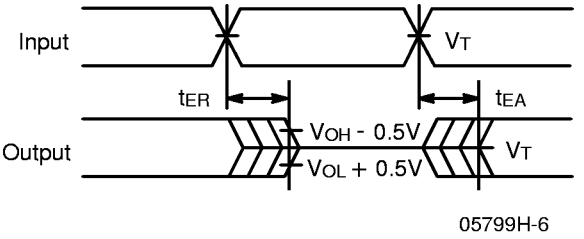
Note:

2. *See Switching Test Circuit for test conditions.*

SWITCHING WAVEFORMS



Combinatorial Output

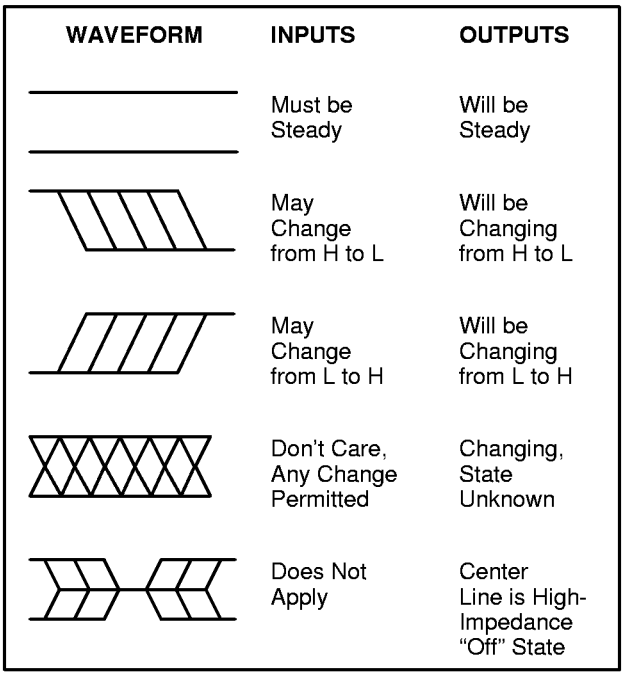


Input to Output Disable/Enable

Notes:

1. *V_T = 1.5 V*
2. *Input pulse amplitude 0 V to 3.0 V*
3. *Input rise and fall times 2 ns–5 ns typical.*

KEY TO SWITCHING WAVEFORMS



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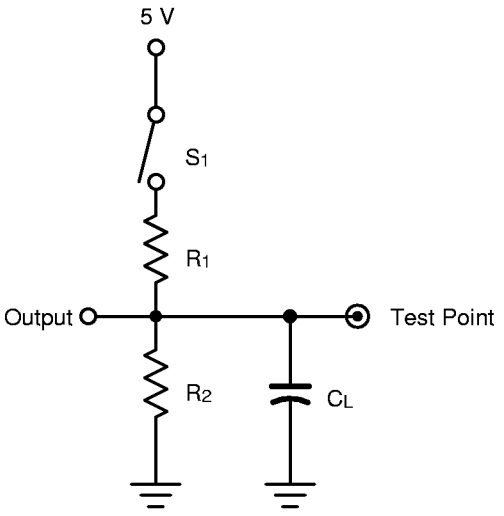
SWITCHING TEST CIRCUIT



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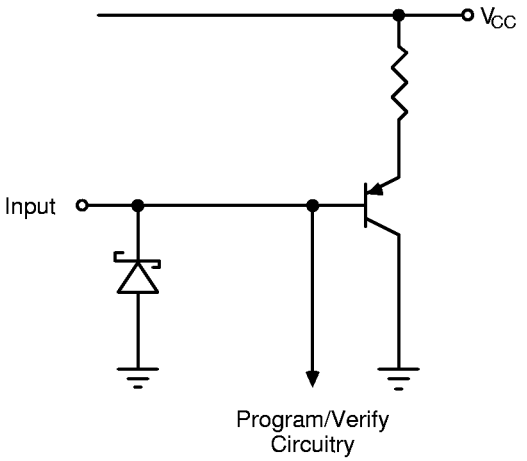
Specification	S_1	C_L	R_1	R_2	Measured Output Value
t_{PD}	Closed	50 pF	200 Ω	390 Ω	1.5 V
t_{EA}	Z → H: Open Z → L: Closed				1.5 V
t_{ER}	H → Z: Open L → Z: Closed	5 pF			H → Z: V_{OH} – 0.5 V L → Z: V_{OL} + 0.5 V

INPUT/OUTPUT EQUIVALENT SCHEMATICS



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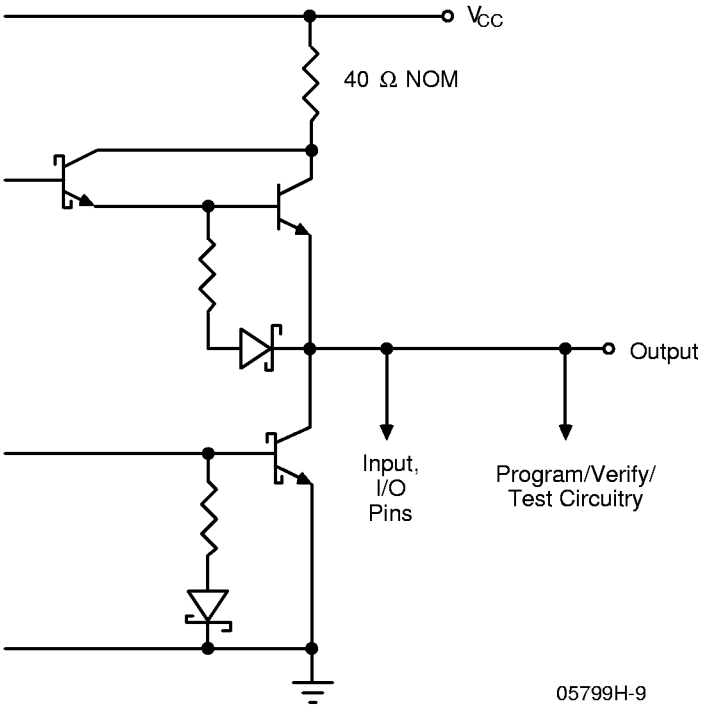
Typical Input



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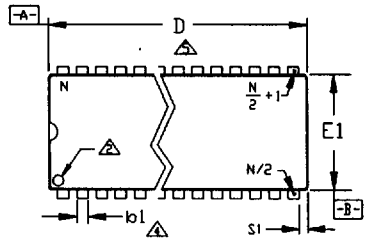
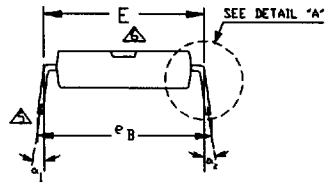
Typical Output

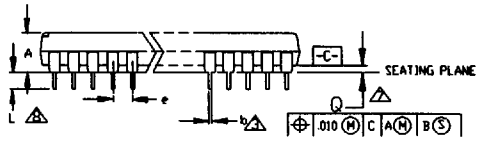
▶Plastic Dual In Line (PDIP) Packages



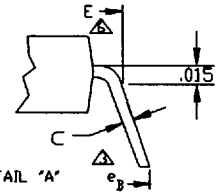
TOP VIEW



END VIEW



SIDE VIEW



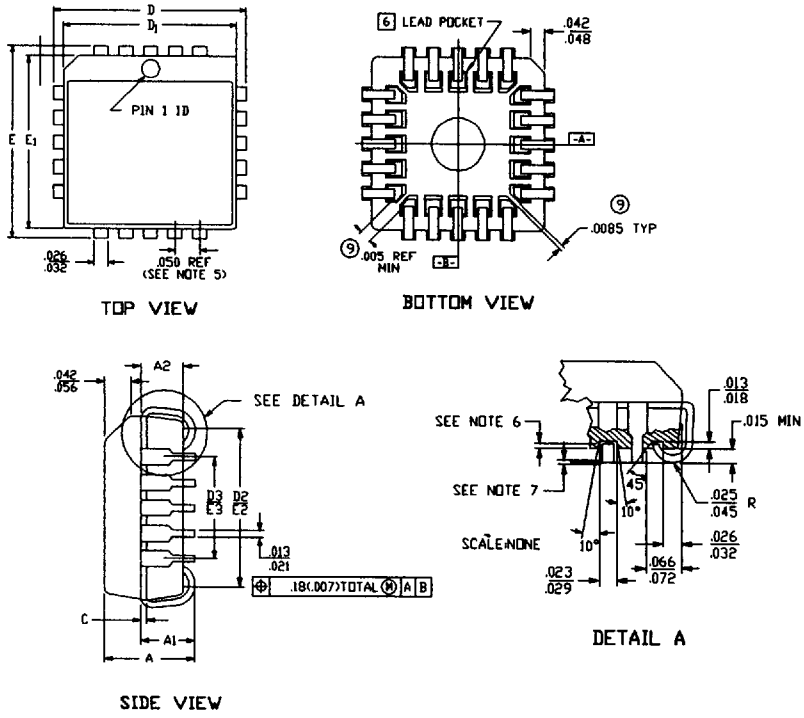
DIMENSION CODES	AMD PACKAGE TYPE & LEADCOUNT (JEDEC DRAWING NUMBER)									
	PD 008		PD 014		PD 016		PD 018		PD 020	
	(MS-001(D)BA)		(MS-001(D)AA)		(MS-001(D)BB)		(MS-001(D)AC)		(MS-001(D)AD)	
	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX
A	0.140	0.200	0.140	0.200	0.140	0.200	0.140	0.200	0.140	0.200
b	0.014	0.022	0.014	0.022	0.014	0.022	0.014	0.022	0.014	0.022
b1	0.045	0.065	0.045	0.065	0.045	0.065	0.045	0.065	0.045	0.065
C	0.008	0.015	0.008	0.015	0.008	0.015	0.008	0.015	0.008	0.015
D	0.375	0.395	0.745	0.760	0.745	0.760	0.890	0.920	1.010	1.040
E1	0.240	0.280	0.240	0.280	0.240	0.280	0.240	0.280	0.240	0.280
E	0.300	0.325	0.300	0.325	0.300	0.325	0.300	0.325	0.300	0.325
e	0.090	0.110	0.090	0.110	0.090	0.110	0.090	0.110	0.090	0.110
L	0.120	0.160	0.120	0.160	0.120	0.160	0.120	0.160	0.120	0.160
Q	0.015	0.060	0.015	0.060	0.015	0.060	0.017	0.060	0.015	0.060
S1	0.005	—	0.005	—	0.005	—	0.005	—	0.005	—
e_b	0.330	0.430	0.330	0.430	0.330	0.430	0.330	0.430	0.330	0.430
$(\alpha_1 - \alpha_2)$	0°	10°	0°	10°	0°	10°	0°	10°	0°	10°
(α_1, α_2)	0°	15°	0°	15°	0°	15°	0°	15°	0°	15°
N	8		14		16		18		20	

Notes:

1. All dimensions are in inches.
2. A notch, tab, or pin one identification mark shall be located adjacent to the device pin one.
3. Lead thickness increases by a maximum of 0.003 inch when a the solder lead finish is applied.
4. The minimum limit for this dimension in a PD 016 package is 0.030 inch in the four corner leads.
5. These dimensions do not include mold flash or protrusion.
6. This dimension is measured from the outside of the leads and 0.015 inch below the plane of the package exit, as defined by the top of the lead.
7. This dimension is measured from the seating plane to the base plane.
8. This dimension is measured from the seating plane (or from the lowest point of the lead shoulder width that measures 0.040 inch) to the lead tip.
9. The difference between these two dimensions should not exceed 7°.
10. When standoff has radii, the seating plane location is defined where the lead width equals 0.040 inch.
11. PD is AMD's internal designator for a plastic dual-in-line package.

▶ Plastic Leaded Chip Carrier (PLCC) Packages

Square Packages

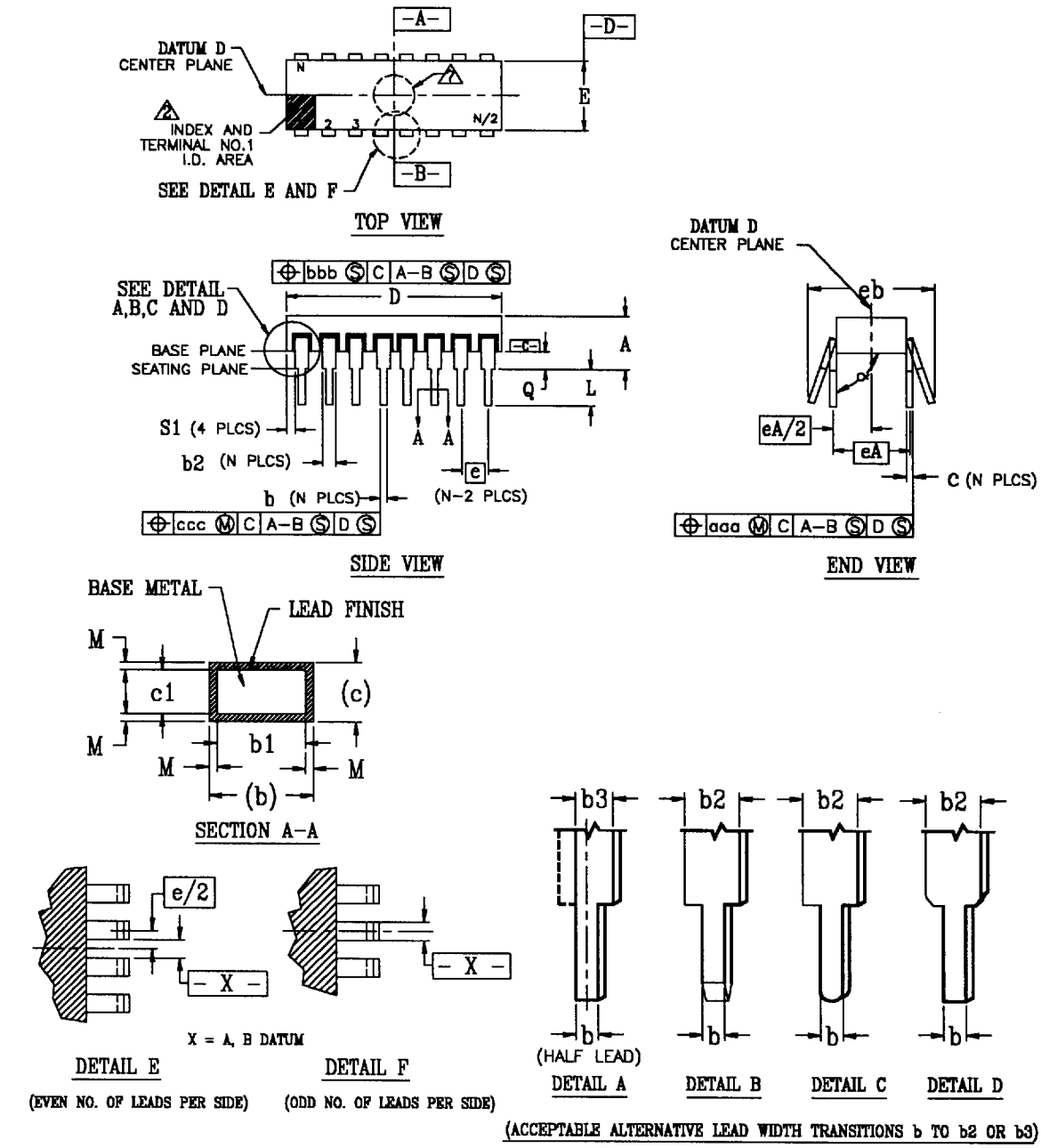


DIMENSION CODES	AMD PACKAGE TYPE & LEADCOUNT (JEDEC DRAWING NUMBER)											
	PL 020		PL 028, PLH028		PL 044		PL 052		PL 068, PLH068		PL 084, PLH084	
	(MS-018(A)AA)		(MS-018(A)AB)		(MS-018(A)AC)		(MO-047(A)AD)		(MO-047(B)AE)		(MO-047(B)AF)	
	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX
A	0.165	0.180	0.165	0.180	0.165	0.180	0.165	0.180	0.165	0.180	0.165	0.180
A1	0.090	0.120	0.090	0.120	0.090	0.120	0.090	0.130	0.090	0.130	0.090	0.130
A2	0.062	0.083	0.062	0.083	0.062	0.083	0.062	0.083	0.062	0.083	0.062	0.083
D, E	0.385	0.395	0.485	0.495	0.685	0.695	0.785	0.795	0.985	0.995	1.185	1.195
D1, E1	0.350	0.356	0.450	0.456	0.650	0.656	0.750	0.756	0.950	0.956	1.150	1.156
D2, E2	0.290	0.330	0.390	0.430	0.590	0.630	0.690	0.730	0.890	0.930	1.090	1.130
D3, E3	0.200 REF		0.300 REF		0.500 REF		0.600 REF		0.800 REF		1.000 REF	
C	0.009	0.015	0.009	0.015	0.009	0.015	0.009	0.015	0.007	0.013	0.007	0.013

Notes:

1. All dimensions are in inches.
2. Dimensions "D" and "E" are measured from the outermost point.
3. Dimensions "D1" and "E1" do not include corner mold flash. Allowable corner mold flash is 0.010 inch.
4. Dimensions "A, A1, D2, and E2" are measured from the points of contact to the base plane.
5. Lead spacing as measured from the center-line to the center-line shall be within ±0.005 inch.
6. J-bend lead tips should be located inside the "pockets."
7. Lead coplanarity shall be within 0.004 inch as measured from the seating plane.
8. Lead tweeze shall be within 0.0045 inch on each side as measured from a vertical flat plane.
9. The lead pocket may be rectangular (as shown) or oval. If the corner lead pockets are connected, then 0.005-inch minimum lead spacing is required.
10. PL is AMD's internal abbreviation for a PLCC. PLH refers to one that has been thermally enhanced with an embedded heat spreader.

▶ Ceramic Dual In Line (CDIP) Packages



(see table of dimensions on next page)

▶ Ceramic Dual In Line (CDIP) Packages

DIMENSION CODES	AMD PACKAGE TYPE & LEADCOUNT											
	CD 014		CD 016		CD 018		CD 020		CDV 020		CD3 022	
	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX
A	0.140	0.200	0.140	0.200	0.140	0.200	0.140	0.200	0.140	0.200	0.140	0.200
b	0.014	0.026	0.014	0.026	0.014	0.026	0.014	0.026	0.014	0.026	0.014	0.026
b1	0.014	0.023	0.014	0.023	0.014	0.023	0.014	0.023	0.014	0.023	0.014	0.023
b2	0.045	0.065	0.045	0.065	0.045	0.065	0.045	0.065	0.045	0.065	0.045	0.065
b3	0.023	0.045	0.023	0.045	0.023	0.045	0.023	0.045	0.023	0.045	0.023	0.045
C	0.008	0.018	0.008	0.018	0.008	0.018	0.008	0.018	0.008	0.018	0.008	0.018
C1	0.008	0.015	0.008	0.015	0.008	0.015	0.008	0.015	0.008	0.015	0.008	0.015
D	0.745	0.785	0.745	0.785	0.875	0.925	0.935	0.975	0.935	0.975	1.055	1.110
E	0.240	0.310	0.240	0.310	0.280	0.310	0.280	0.310	0.280	0.310	0.280	0.310
e	0.100 BASIC		0.100 BASIC		0.100 BASIC		0.100 BASIC		0.100 BASIC		0.100 BASIC	
eA	0.300 BASIC		0.300 BASIC		0.300 BASIC		0.300 BASIC		0.300 BASIC		0.300 BASIC	
eA/2	0.150 BASIC		0.150 BASIC		0.150 BASIC		0.150 BASIC		0.150 BASIC		0.150 BASIC	
eb	—	0.400	—	0.400	—	0.400	—	0.400	—	0.400	—	0.400
L	0.125	0.200	0.125	0.200	0.125	0.200	0.125	0.200	0.125	0.200	0.125	0.200
M	—	0.0015	—	0.0015	—	0.0015	—	0.0015	—	0.0015	—	0.0015
Q	0.015	0.060	0.015	0.060	0.015	0.060	0.015	0.060	0.015	0.060	0.015	0.060
S1	0.005	—	0.005	—	0.005	—	0.005	—	0.005	—	0.005	—
aaa	—	0.015	—	0.015	—	0.015	—	0.015	—	0.015	—	0.015
bbb	—	0.030	—	0.030	—	0.030	—	0.030	—	0.030	—	0.030
ccc	—	0.010	—	0.010	—	0.010	—	0.010	—	0.010	—	0.010
α	94°	105°	94°	105°	94°	105°	94°	105°	94°	105°	94°	105°
N	14		16		18		20		20		22	
MIL-STD 1835 Case Outline[10]	D-1		D-2		D-6		D-8		D-8		D-7	

Notes:

1. All dimensions are in inches.
2. A notch, tab, or pin-one identification mark shall be located adjacent to pin one within the shaded area.
3. Dimensions "D" and "E" allow for off-center lid meniscus and glass overrun.
4. Dimensions "A" and "Q" are measured from the seating plane when the component is inserted into a 0.0415-inch minimum or 0.043-inch maximum gauge-hole socket.
5. Dimension "L" is measured from the seating plane to the lead tips.
6. For dimension "e," each lead spacing shall be located within ± 0.010 inch of its true position.
7. This area may be a round, square, or rectangular shaped ultraviolet (UV) glass window in ceramic DIP packages for erasable memory products (designated as CDV).
8. Dimension "D" does not include units with bumper tape or clips.
9. CD is AMD's internal designator for a ceramic dual-in-line package. CD3 and CD4 indicate that the package width varies from the standard width for that pin-count. CDV means the package cap has a view window. CDE is a CD3 with a view window.
10. When "NL" is listed as the MIL-STD 1835 reference, the package is not listed in MIL-STD 1835.