HARRIS SEMICONDUCTOR

HI5703

December 1997

10-Bit, 40 MSPS A/D Converter

Features

- Sampling Rate . . . . . 40 MSPS
- 8.55 Bits Guaranteed at f_{IN} = 10MHz
- Low Power
- Wide Full Power Input Bandwidth 250MHz
- On Chip Sample and Hold
- Fully Differential or Single-Ended Analog Input
- Single Supply Voltage . . . . . +5V
- TTL Compatible Interface
- 3.3V Digital Outputs Available

Applications

- Professional Video Digitizing
- Medical Imaging
- Digital Communication Systems
- High Speed Data Acquisition
- Additional Reference Documents
  - AN9534 Using the HI5703 Evaluation Board
  - AN9413 Driving the Analog Input of the HI5702
  - AN9214 Using Harris High Speed A/D Converters

Description

The HI5703 is a monolithic, 10-bit, analog-to-digital converter fabricated in Harris's BiCMOS process. It is designed for high speed applications where wide bandwidth and low power consumption are essential. Its 40 MSPS speed is made possible by a fully differential pipeline architecture with an internal sample and hold.

The HI5703 has excellent dynamic performance while consuming only 400mW power at 40 MSPS. Data output latches are provided which present valid data to the output bus with a latency of 7 clock cycles. It is pin-to-pin compatible with the HI5702.

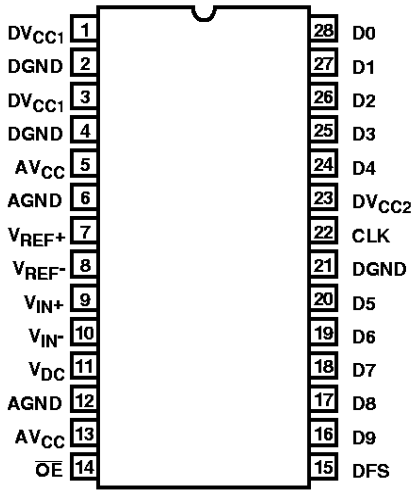
For lower power consumption or internal reference, please refer to the HI5746 or HI5767.

Ordering Information

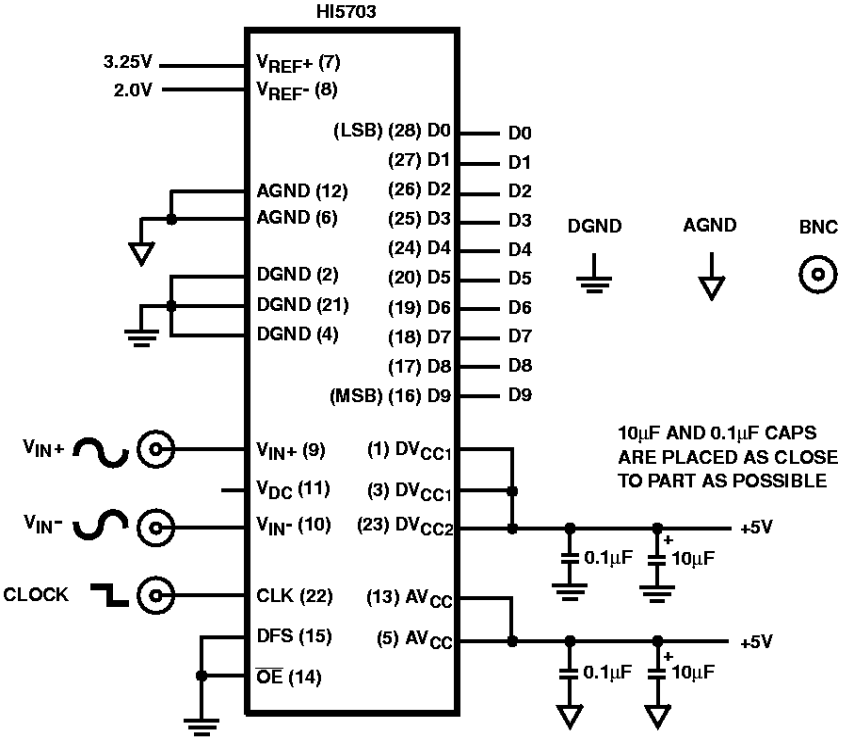
PART NUMBER	TEMP. RANGE (^{o}C)	PACKAGE	PKG. NO.
HI5703KCB	0 to 70	28 Ld SOIC (W)	M28.3
HI5703EVAL	25	Evaluation Board	

Pinout

HI5703
(SOIC)
TOP VIEW



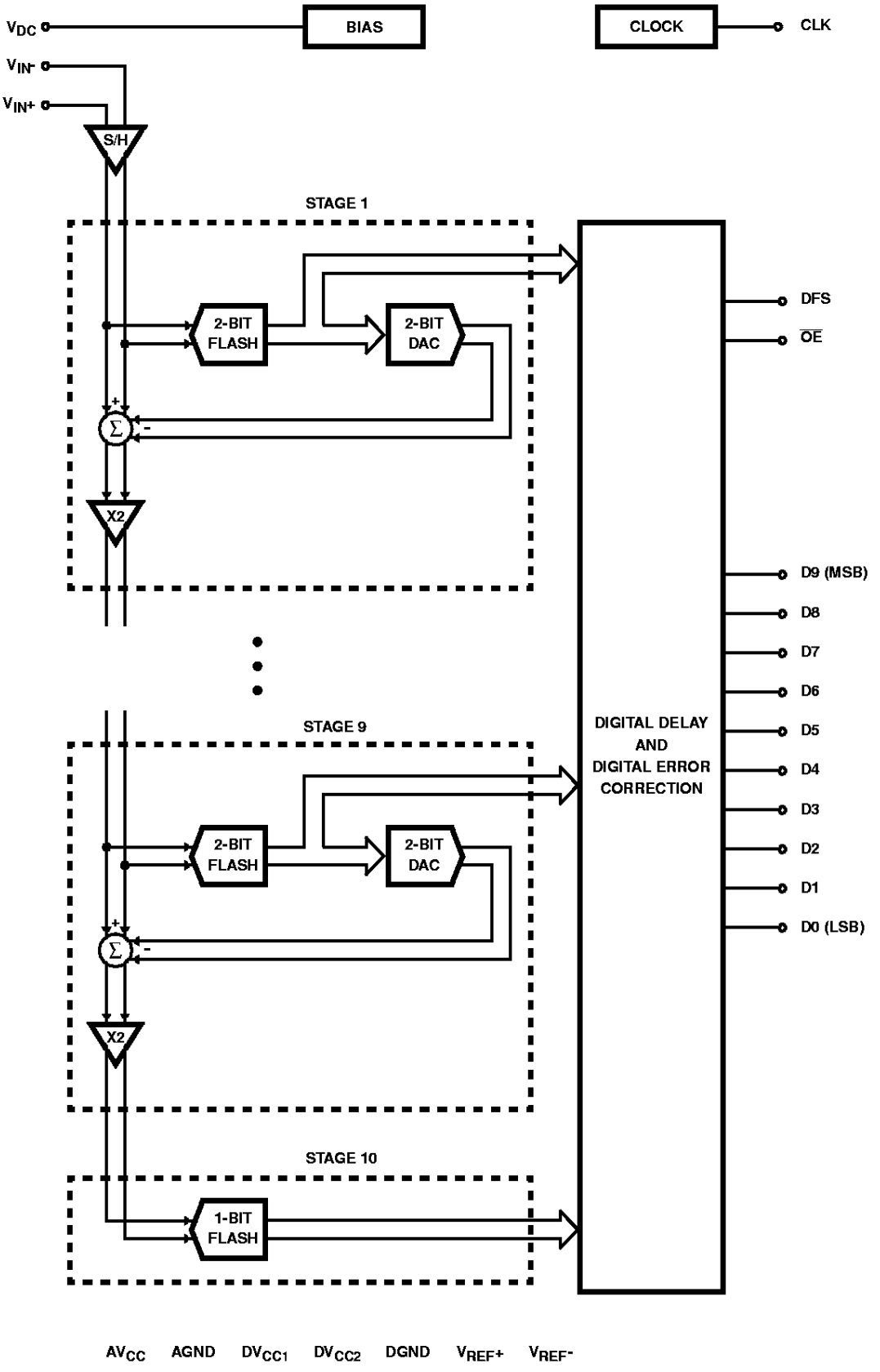
Typical Application Schematic



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.

File Number **3950.6**

Functional Block Diagram



Absolute Maximum Ratings $T_A = 25^oC$

Supply Voltage, AV_{CC} or DV_{CC} to AGND or DGND . . . . . +6V
DGND to AGND 0.3V
Digital I/O Pins . . . . . DGND to DV_{CC}
Analog I/O Pins. . . . . AGND to AV_{CC}

Operating Conditions

Temperature Range, HI5703KCB. . . . . .0^oC to 70^oC

Thermal Information

Thermal Resistance (Typical, Note 1)	θ_{JA} ($^oC/W$)
SOIC Package	70

Maximum Junction Temperature . . . . . 150^oC
Maximum Storage Temperature Range . . . . . -65^oC to 150^oC
Maximum Lead Temperature (Soldering 10s) . . . . . 300^oC
(SOIC - Lead Tips Only)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

1. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications

$AV_{CC} = DV_{CC1} = DV_{CC2} = +5.0V$; $V_{REF}+ = 3.25V$; $V_{REF}- = 2.0V$; $f_S = 36$ MSPS at 50% Duty Cycle; $C_L = 20pF$; $T_A = 25^oC$; Differential Analog Input; Unless Otherwise Specified

PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNITS
ACCURACY					
Resolution		10	-	-	Bits
Integral Linearity Error, INL	f_{IN} = DC	-	±1	±2.0	LSB
Differential Linearity Error, DNL (Guaranteed No Missing Codes)	f_{IN} = DC	-	±0.5	±1	LSB
Offset Error, V_{OS}	f_{IN} = DC	-	4	-	LSB
Full Scale Error, FSE	f_{IN} = DC	-	1	-	LSB
DYNAMIC CHARACTERISTICS					
Minimum Conversion Rate	No Missing Codes	-	0.5	1	MSPS
Maximum Conversion Rate	No Missing Codes	40	-	-	MSPS
Effective Number of Bits, ENOB	f_{IN} = 1MHz	-	9.2	-	Bits
	f_{IN} = 5MHz	-	9.2	-	Bits
	f_{IN} = 10MHz	8.55	8.9	-	Bits
Signal to Noise and Distortion Ratio, SINAD = $\frac{\text{RMS Signal}}{\text{RMS Noise + Distortion}}$	f_{IN} = 1MHz	-	57	-	dB
	f_{IN} = 5MHz	-	57	-	dB
	f_{IN} = 10MHz	53.2	55	-	dB
Signal to Noise Ratio, SNR = $\frac{\text{RMS Signal}}{\text{RMS Noise}}$	f_{IN} = 1MHz	-	58	-	dB
	f_{IN} = 5MHz	-	58	-	dB
	f_{IN} = 10MHz	53.2	57	-	dB
Total Harmonic Distortion, THD	f_{IN} = 1MHz	-	-64	-	dBc
	f_{IN} = 5MHz	-	-63	-	dBc
	f_{IN} = 10MHz	-	-60	-	dBc
2nd Harmonic Distortion	f_{IN} = 1MHz	-	-75	-	dBc
	f_{IN} = 5MHz	-	-75	-	dBc
	f_{IN} = 10MHz	-	-73	-	dBc
3rd Harmonic Distortion	f_{IN} = 1MHz	-	-66	-	dBc
	f_{IN} = 5MHz	-	-64	-	dBc
	f_{IN} = 10MHz	-	-63	-	dBc
Spurious Free Dynamic Range, SFDR	f_{IN} = 1MHz	-	66	-	dBc
	f_{IN} = 5MHz	-	64	-	dBc
	f_{IN} = 10MHz	54	63	-	dBc
Intermodulation Distortion, IMD	f_1 = 1MHz, f_2 = 1.02MHz	-	-59	-	dBc
Differential Gain Error	f_S = 17.72MHz, 6 Step, Mod Ramp	-	0.5	-	%
Differential Phase Error	f_S = 17.72MHz, 6 Step, Mod Ramp	-	0.1	-	Degree
Transient Response		-	1	-	Cycle
Over-Voltage Recovery	0.2V Overdrive	-	1	-	Cycle

Electrical Specifications $AV_{CC} = DV_{CC1} = DV_{CC2} = +5.0V$; $V_{REF}+ = 3.25V$; $V_{REF}- = 2.0V$; $f_S = 36$ MSPS at 50% Duty Cycle; $C_L = 20pF$; $T_A = 25^oC$; Differential Analog Input; Unless Otherwise Specified **(Continued)**

PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNITS
ANALOG INPUT					
Maximum Peak-to-Peak Differential Analog Input Range ($V_{IN+} - V_{IN-}$)		-	±1.25	-	V
Maximum Peak-to-Peak Single-Ended Analog Input Range		-	2.5	-	V
Analog Input Resistance, R_{IN}	(Note 3)	-	1	-	MΩ
Analog Input Capacitance, C_{IN}		-	7	-	pF
Analog Input Bias Current, I_{B+} or I_{B-}	(Note 3)	-10	-	+10	µA
Differential Analog Input Bias Current $I_{B\ DIFF} = (I_{B+} - I_{B-})$		-	±0.5	-	µA
Analog Input Common Mode Voltage Range $(V_{IN+} + V_{IN-}) / 2$	Differential Mode (Note 1)	0.625	-	4.375	V
Full Power Input Bandwidth (FPBW)		-	250	-	MHz
REFERENCE INPUT					
Total Reference Resistance, R_L		300	400	500	Ω
Reference Current		2.5	3.125	4.2	mA
Positive Reference Voltage Input, $V_{REF}+$	(Note 2)	-	3.25	3.3	V
Negative Reference Voltage Input, $V_{REF}-$	(Note 2)	1.95	2.0	-	V
Reference Common Mode Voltage $(V_{REF}+ + V_{REF}-) / 2$	(Note 2)	2.575	2.625	2.675	V
DC BIAS VOLTAGE					
DC Bias Voltage Output, V_{DC}		-	2.8	-	V
Max Output Current		-	-	1	mA
DIGITAL INPUTS					
Input Logic High Voltage, V_{IH}		2.0	-	-	V
Input Logic Low Voltage, V_{IL}		-	-	0.8	V
Input Logic High Current, I_{IH}	$V_{IH} = 5V$	-	-	10.0	µA
Input Logic Low Current, I_{IL}	$V_{IL} = 0V$	-	-	10.0	µA
Input Capacitance, C_{IN}		-	7	-	pF
DIGITAL OUTPUTS					
Output Logic Sink Current, I_{OL}	$V_O = 0.4V$; $DV_{CC2} = 5V$	1.6	-	-	mA
Output Logic Source Current, I_{OH}	$V_O = 2.4V$; $DV_{CC2} = 5V$	-0.2	-	-	mA
Output Three-State Leakage Current, I_{OZ}	$V_O = 0/5V$; $DV_{CC2} = 5V$	-	±1	±10	µA
Output Logic Sink Current, I_{OL}	$V_O = 0.4V$; $DV_{CC2} = 3.3V$	1.6	-	-	mA
Output Logic Source Current, I_{OH}	$V_O = 2.4V$; $DV_{CC2} = 3.3V$	-0.2	-	-	mA
Output Three-State Leakage Current, I_{OZ}	$V_O = 0/3.3V$; $DV_{CC2} = 3.3V$	-	±1	±10	µA
Output Capacitance, C_{OUT}		-	5	-	pF
TIMING CHARACTERISTICS					
Aperture Delay, t_{AP}		-	5	-	ns
Aperture Jitter, t_{AJ}		-	5	-	ps
Data Output Delay, t_{OD}		-	7	-	ns
	$AV_{CC} = DV_{CC1} = 5V \pm 10\%$, $DV_{CC2} = 3.3V \pm 5\%$, $0^oC \le T_A \le 70^oC$	5	7	18	ns
Data Output Hold, t_H		-	4	-	ns
Data Output Enable Time, t_{EN}		-	7	-	ns
Data Output Enable Time, t_{DIS}		-	7	-	ns
Clock Pulse Width (Low)	40 MSPS Clock	11.875	12.5	13.125	ns
Clock Pulse Width (High)	40 MSPS Clock	11.875	12.5	13.125	ns

Electrical Specifications

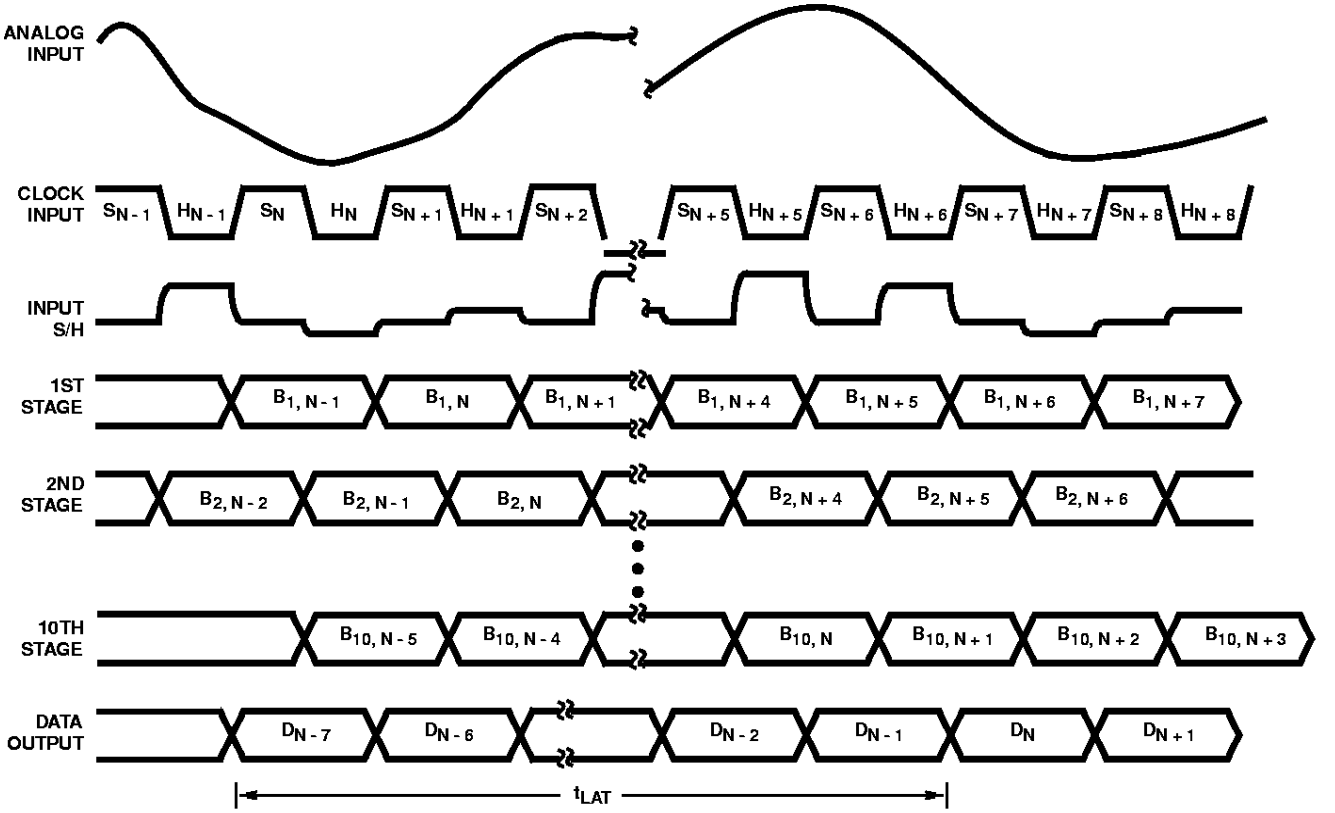
AV_{CC} = DV_{CC1} = DV_{CC2} = +5.0V; V_{REF}+ = 3.25V; V_{REF}- = 2.0V; f_S = 36 MSPS at 50% Duty Cycle; C_L = 20pF; T_A = 25°C; Differential Analog Input; Unless Otherwise Specified **(Continued)**

PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNITS
Data Latency, t_{LAT}	For a Valid Sample (Note 2)	-	-	7	Cycles
Power-Up Initialization	Data Invalid Time (Note 2)	-	-	20	Cycles
POWER SUPPLY CHARACTERISTICS					
Analog Supply Voltage, AV_{CC}		4.75	5.0	5.25	V
Digital Supply Voltage, DV_{CC1}		4.75	5.0	5.25	V
Digital Output Supply Voltage, DV_{CC2}	At 3.30V	3.135	3.3	3.465	V
	At 5.0V	4.75	5.0	5.25	V
Total Supply Current, I_{CC}	V_{IN}+ - V_{IN}- = +1.25V and DFS = "0"	-	80	-	mA
Analog Supply Current, AI_{CC}	V_{IN}+ - V_{IN}- = +1.25V and DFS = "0"	-	48	-	mA
Digital Supply Current, DI_{CC1}	V_{IN}+ - V_{IN}- = +1.25V and DFS = "0"	-	30	-	mA
Digital Output Supply Current, DI_{CC2}	V_{IN}+ - V_{IN}- = +1.25V and DFS = "0"	-	2	-	mA
Power Dissipation	V_{IN}+ - V_{IN}- = +1.25V and DFS = "0"	-	400	-	mW
Offset Error Sensitivity, ΔV_{OS}	AV_{CC} or DV_{CC} = 5V ±5%	-	±1.5	-	LSB
Full Scale Error Sensitivity, ΔFSE	AV_{CC} or DV_{CC} = 5V ±5%	-	±0.2	-	LSB

NOTES:

2. Parameter guaranteed by design or characterization and not production tested.
3. With the clock low and DC input.

Timing Waveforms



NOTES:

4. S_N: N-th sampling period.
5. H_N: N-th holding period.
6. $B_{M, N}$: M-th stage digital output corresponding to N-th sampled input.
7. D_N: Final data output corresponding to N-th sampled input.

FIGURE 1. HI5703 INTERNAL CIRCUIT TIMING

Timing Waveforms (Continued)

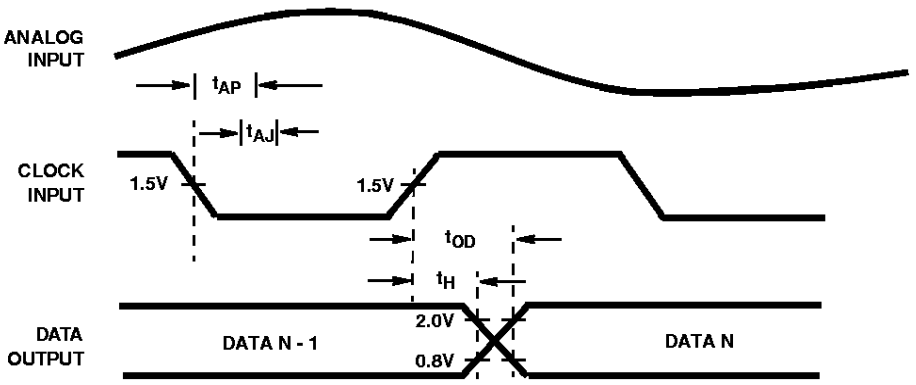


FIGURE 2. INPUT-TO-OUTPUT TIMING

Typical Performance Curves

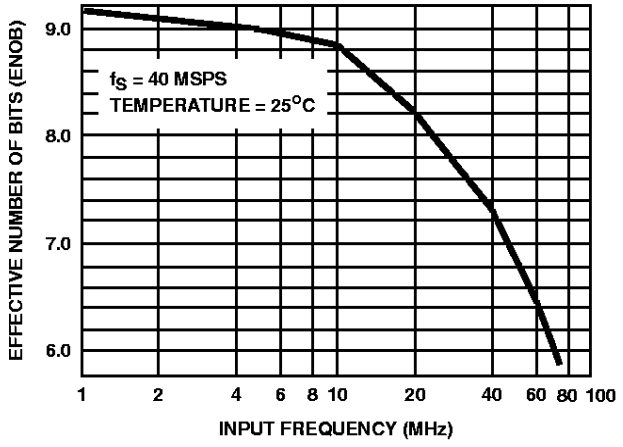
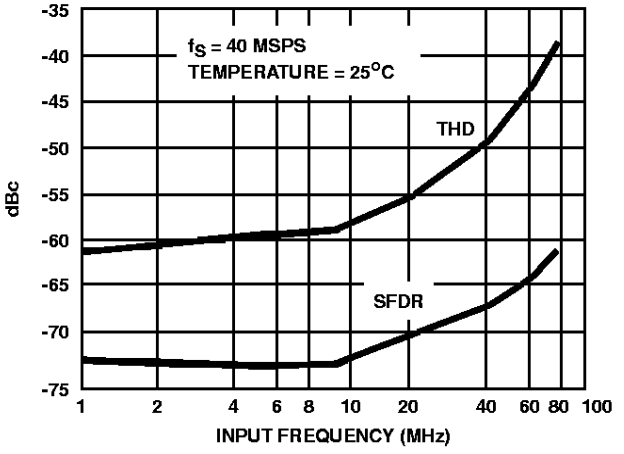


FIGURE 3. EFFECTIVE NUMBER OF BITS (ENOB) vs INPUT FREQUENCY



NOTE: SFDR depicted here does not include any harmonic distortion.

FIGURE 4. TOTAL HARMONIC DISTORTION (THD) AND SPURIOUS FREE DYNAMIC RANGE (SFDR) vs INPUT FREQUENCY

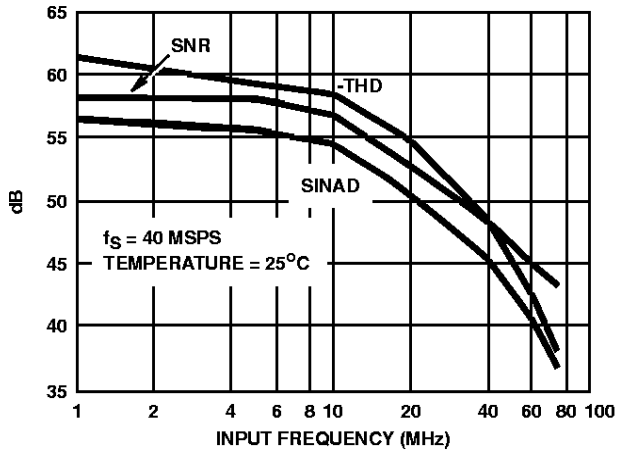


FIGURE 5. SINAD, SNR, AND -THD vs INPUT FREQUENCY

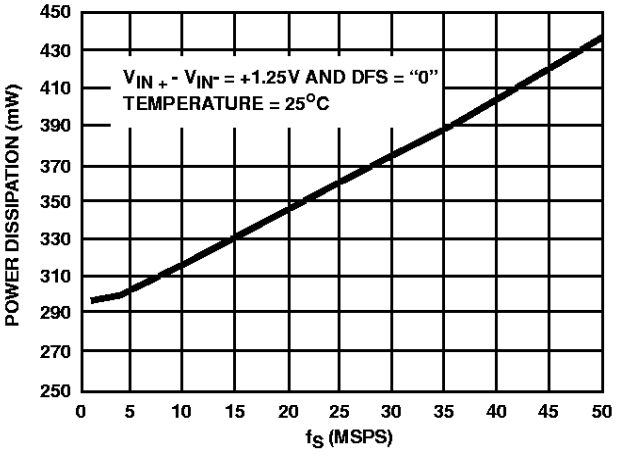


FIGURE 6. POWER DISSIPATION vs SAMPLE FREQUENCY