CY7C1370B
CY7C1372B

512K × 36/1M × 18 Pipelined SRAM with NoBL™ Architecture

Features

- **Zero Bus Latency, no dead cycles between Write and Read cycles**
- **Fast clock speed: 200, 167, 150, and 133 MHz**
- **Fast access time: 3.0, 3.4, 3.8, and 4.2 ns**
- **Internally synchronized registered outputs eliminate the need to control OE**
- **Single 3.3V –5% and +10% power supply V_{DD}**
- **Separate V_{DDQ} for 3.3V or 2.5V I/O**
- **Single WE (Read/Write) control pin**
- **Positive clock-edge triggered address, data, and control signal registers for fully pipelined applications**
- **Interleaved or linear four-word burst capability**
- **Individual byte Write (BWSa–BWSd) control (may be tied LOW)**
- **CEN pin to enable clock and suspend operations**
- **Three chip enables for simple depth expansion**
- **JTAG boundary scan (BGA package only)**
- **Available in 119-ball bump BGA and 100-pin TQFP packages**
- **Automatic power down available using ZZ mode or CE deselect**

Functional Description

The CY7C1370B and CY7C1372B SRAMs are designed to eliminate dead cycles when transitions from Read to Write or vice versa. These SRAMs are optimized for 100 percent bus utilization and achieve Zero Bus Latency™. They integrate 524,288 × 36 and 1,048,576 × 18 SRAM cells, respectively, with advanced synchronous peripheral circuitry and a 2-bit counter for internal burst operation. The Synchronous Burst SRAM family employs high-speed, low-power CMOS designs using advanced single-layer polysilicon, three-layer metal technology. Each memory cell consists of six transistors.

All synchronous inputs are gated by registers controlled by a positive-edge-triggered Clock input (CLK). The synchronous inputs include all addresses, all data inputs, depth-expansion Chip Enables ($\overline{CE_1}$, CE_2, and $\overline{CE_3}$), cycle start input (ADV/$\overline{LD}$), Clock enable ($\overline{CEN}$), byte Write Enables (BWSa, $\overline{BWSb}$, $\overline{BWSc}$, and $\overline{BWSd}$), and Read-Write Control ($\overline{WE}$). $\overline{BWSc}$ and $\overline{BWSd}$ apply to CY7C1370B only.

Address and control signals are applied to the SRAM during one clock cycle, and two cycles later, its associated data occurs, either Read or Write.

A Clock enable ($\overline{CEN}$) pin allows operation of the CY7C1370B/CY7C1372B to be suspended as long as necessary. All synchronous inputs are ignored when $\overline{CEN}$ is HIGH and the internal device registers will hold their previous values.

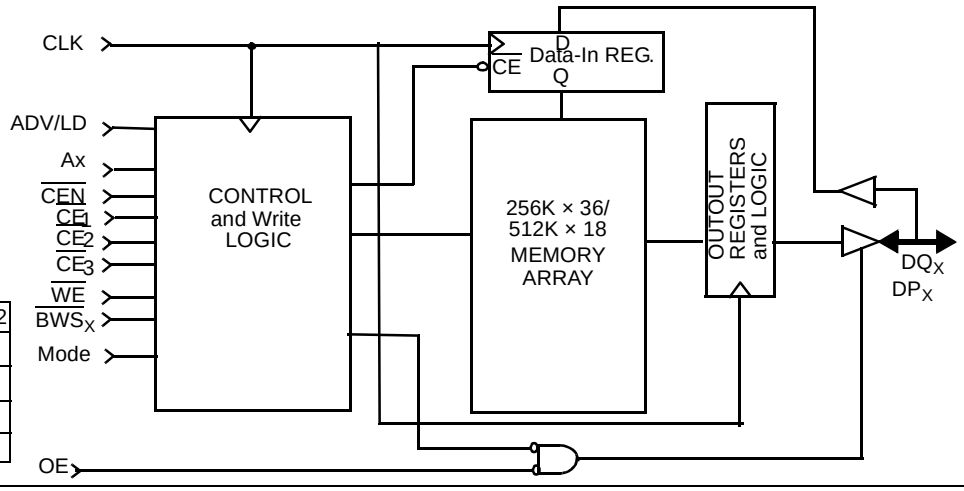
There are three chip enable pins ($\overline{CE_1}$, CE_2, $\overline{CE_3}$) that allow the user to deselect the device when desired. If any one of these three are not active when ADV/$\overline{LD}$ is LOW, no new memory operation can be initiated and any burst cycle in progress is stopped. However, any pending data transfers (Read or Write) will be completed. The data bus will be in high-impedance state two cycles after the chip is deselected or a Write cycle is initiated.

The CY7C1370B and CY7C1372B have an on-chip two-bit burst counter. In the burst mode, the CY7C1370B and CY7C1372B provide four cycles of data for a single address presented to the SRAM. The order of the burst sequence is defined by the MODE input pin. The MODE pin selects between linear and interleaved burst sequence. The ADV/$\overline{LD}$ signal is used to load a new external address (ADV/$\overline{LD}$ = LOW) or increment the internal burst counter (ADV/$\overline{LD}$ = HIGH)

Output enable ($\overline{OE}$) and burst sequence select (MODE) are the asynchronous signals. $\overline{OE}$ can be used to disable the outputs at any given time. ZZ may be tied to LOW if it is not used.

Four pins are used to implement JTAG test capabilities. The JTAG circuitry is used to serially shift data to and from the device. JTAG inputs use LVTTL/LVCMOS levels to shift data during this testing mode of operation.

Logic Block Diagram



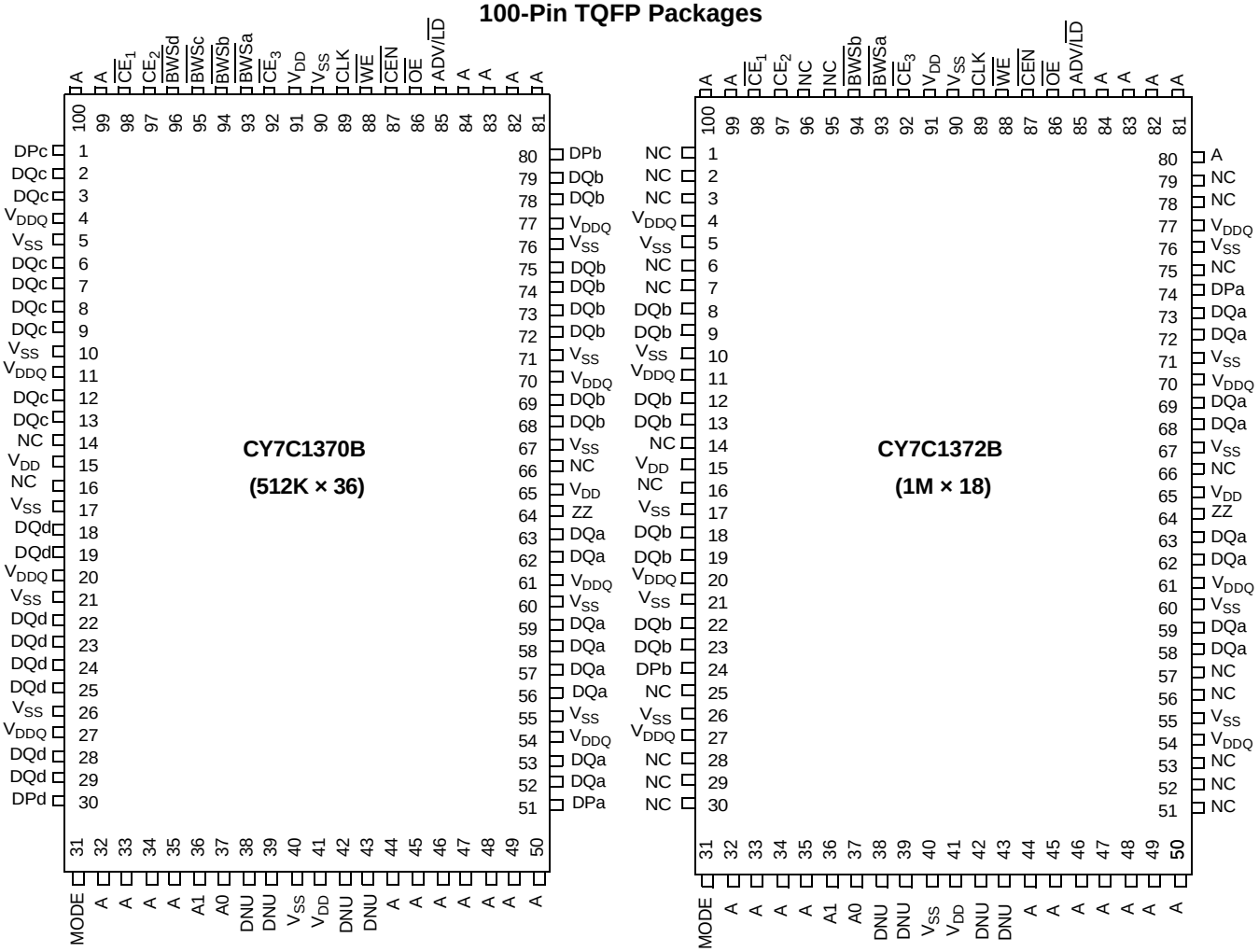
	CY7C1370	CY7C1372
A_X	X = 18:0	X = 19:0
DQ_X	X = a, b, c, d	X = a, b
DP_X	X = a, b, c, d	X = a, b
$\overline{BWS_X}$	X = a, b, c, d	X = a, b

Selection Guide

		200 MHz	167 MHz	150 MHz	133 MHz	Unit
Maximum Access Time		3.0	3.4	3.8	4.2	ns
Maximum Operating Current	Commercial	315	285	265	245	mA
Maximum CMOS Standby Current		20	20	20	20	mA

Pin Configurations

100-Pin TQFP Packages



Pin Configurations (continued)

119-ball Bump BGA

CY7C1370B (512K × 36) – 7 × 17 BGA

	1	2	3	4	5	6	7
A	V_{DDQ}	A	A	A	A	A	V_{DDQ}
B	NC	CE_2	A	ADV/$\overline{LD}$	A	$\overline{CE_3}$	NC
C	NC	A	A	V_{DD}	A	A	NC
D	DQc	DPc	V_{SS}	NC	V_{SS}	DPb	DQb
E	DQc	DQc	V_{SS}	$\overline{CE_1}$	V_{SS}	DQb	DQb
F	V_{DDQ}	DQc	V_{SS}	$\overline{OE}$	V_{SS}	DQb	V_{DDQ}
G	DQc	DQc	$\overline{BWSc}$	A	$\overline{BWSb}$	DQb	DQb
H	DQc	DQc	V_{SS}	$\overline{WE}$	V_{SS}	DQ_b	DQb
J	V_{DDQ}	V_{DD}	NC	V_{DD}	NC	V_{DD}	V_{DDQ}
K	DQd	DQd	V_{SS}	CLK	V_{SS}	DQa	DQa
L	DQd	DQd	$\overline{BWSd}$	NC	$\overline{BWSa}$	DQa	DQa
M	V_{DDQ}	DQd	V_{SS}	$\overline{CEN}$	V_{SS}	DQa	V_{DDQ}
N	DQd	DQd	V_{SS}	A1	V_{SS}	DQa	DQa
P	DQd	DPd	V_{SS}	A0	V_{SS}	DPa	DQa
R	NC	A	MODE	V_{DD}	NC	A	NC
T	NC	64M	A	A	A	32M	ZZ
U	V_{DDQ}	TMS	TDI	TCK	TDO	NC	V_{DDQ}

CY7C1372B (1M × 18) – 7 × 17 BGA

	1	2	3	4	5	6	7
A	V_{DDQ}	A	A	A	A	A	V_{DDQ}
B	NC	CE_2	A	ADV/$\overline{LD}$	A	$\overline{CE_3}$	NC
C	NC	A	A	V_{DD}	A	A	NC
D	DQb	NC	V_{SS}	NC	V_{SS}	DPa	NC
E	NC	DQb	V_{SS}	$\overline{CE_1}$	V_{SS}	NC	DQa
F	V_{DDQ}	NC	V_{SS}	$\overline{OE}$	V_{SS}	DQa	V_{DDQ}
G	NC	DQb	$\overline{BWSb}$	A	V_{SS}	NC	DQa
H	DQb	NC	V_{SS}	$\overline{WE}$	V_{SS}	DQa	NC
J	V_{DDQ}	V_{DD}	NC	V_{DD}	NC	V_{DD}	V_{DDQ}
K	NC	DQb	V_{SS}	CLK	V_{SS}	NC	DQa
L	DQb	NC	V_{SS}	NC	$\overline{BWSa}$	DQa	NC
M	V_{DDQ}	DQb	V_{SS}	$\overline{CEN}$	V_{SS}	NC	V_{DDQ}
N	DQb	NC	V_{SS}	A1	V_{SS}	DQa	NC
P	NC	DPb	V_{SS}	A0	V_{SS}	NC	DQa
R	NC	A	MODE	V_{DD}	NC	A	NC
T	64M	A	A	32M	A	A	ZZ
U	V_{DDQ}	TMS	TDI	TCK	TDO	NC	V_{DDQ}

Pin Configurations (continued)

165-ball Bump FBGA

CY7C1370B (512K × 36) – 11 × 15 FBGA

	1	2	3	4	5	6	7	8	9	10	11
A	NC	A	$\overline{CE_1}$	$\overline{BWSc}$	$\overline{BWSb}$	$\overline{CE_3}$	$\overline{CEN}$	ADV/$\overline{LD}$	A	A	NC
B	NC	A	CE_2	$\overline{BWSd}$	$\overline{BWSa}$	CLK	$\overline{WE}$	$\overline{OE}$	A	A	128M
C	DPc	NC	V_{DDQ}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{DDQ}	NC	DPb
D	DQc	DQc	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	DQb	DQb
E	DQc	DQc	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	DQb	DQb
F	DQc	DQc	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	DQb	DQb
G	DQc	DQc	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	DQb	DQb
H	NC	V_{DD}	NC	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	NC	NC	ZZ
J	DQd	DQd	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	DQa	DQa
K	DQd	DQd	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	DQa	DQa
L	DQd	DQd	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	DQa	DQa
M	DQd	DQd	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	DQa	DQa
N	DPd	NC	V_{DDQ}	V_{SS}	NC	NC	NC	V_{SS}	V_{DDQ}	NC	DPa
P	NC	64M	A	A	TDI	A1	TDO	A	A	A	NC
R	MODE	32M	A	A	TMS	A0	TCK	A	A	A	A

CY7C1372B (1M × 18) – 11 × 15 FBGA

	1	2	3	4	5	6	7	8	9	10	11
A	NC	A	$\overline{CE_1}$	$\overline{BWSb}$	NC	$\overline{CE_3}$	$\overline{CEN}$	ADV/$\overline{LD}$	A	A	A
B	NC	A	CE_2	NC	$\overline{BWSa}$	CLK	$\overline{WE}$	$\overline{OE}$	A	A	128M
C	NC	NC	V_{DDQ}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{DDQ}	NC	DPa
D	NC	DQb	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	NC	DQa
E	NC	DQb	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	NC	DQa
F	NC	DQb	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	NC	DQa
G	NC	DQb	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	NC	DQa
H	NC	V_{DD}	NC	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	NC	NC	ZZ
J	DQb	NC	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	DQa	NC
K	DQb	NC	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	DQa	NC
L	DQb	NC	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	DQa	NC
M	DQb	NC	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	DQa	NC
N	DPb	NC	V_{DDQ}	V_{SS}	NC	NC	NC	V_{SS}	V_{DDQ}	NC	NC
P	NC	64M	A	A	TDI	A1	TDO	A	A	A	NC
R	MODE	32M	A	A	TMS	A0	TCK	A	A	A	A

Pin Definitions

Name	I/O Type	Description
A0 A1 A	Input-Synchronous	**Address inputs used to select one of the 524,288/1,048576 address locations**. Sampled at the rising edge of the CLK.
$\overline{BWS}$a $\overline{BWS}$b $\overline{BWS}$c $\overline{BWS}$d	Input-Synchronous	**Byte Write Select inputs, active LOW**. Qualified with $\overline{WE}$ to conduct writes to the SRAM. Sampled on the rising edge of CLK. $\overline{BWS}$a controls DQa and DPa, $\overline{BWS}$b controls DQb and DPb, BWSc controls DQc and DPc, BWSd controls DQd and DPd.
$\overline{WE}$	Input-Synchronous	**Write enable input, active LOW**. Sampled on the rising edge of CLK if $\overline{CEN}$ is active LOW. This signal must be asserted LOW to initiate a Write sequence.
ADV/$\overline{LD}$	Input-Synchronous	**Advance/Load input used to advance the on-chip address counter or load a new address**. When HIGH (and $\overline{CEN}$ is asserted LOW) the internal burst counter is advanced. When LOW, a new address can be loaded into the device for an access. After being deselected, ADV/$\overline{LD}$ should be driven LOW in order to load a new address.
CLK	Input-Clock	**Clock input**. Used to capture all synchronous inputs to the device. CLK is qualified with $\overline{CEN}$. CLK is only recognized if $\overline{CEN}$ is active LOW.
$\overline{CE}_1$	Input-Synchronous	**Chip enable 1 input, active LOW**. Sampled on the rising edge of CLK. Used in conjunction with CE_2 and $\overline{CE}_3$ to select/deselect the device.
CE_2	Input-Synchronous	**Chip enable 2 input, active HIGH**. Sampled on the rising edge of CLK. Used in conjunction with $\overline{CE}_1$ and $\overline{CE}_3$ to select/deselect the device.
$\overline{CE}_3$	Input-Synchronous	**Chip enable 3 input, active LOW**. Sampled on the rising edge of CLK. Used in conjunction with $\overline{CE}_1$ and CE_2 to select/deselect the device.
$\overline{OE}$	Input-Asynchronous	**Output enable, active LOW**. Combined with the synchronous logic block inside the device to control the direction of the I/O pins. When LOW, the I/O pins are allowed to behave as outputs. When deasserted HIGH, I/O pins are three-stated, and act as input data pins. $\overline{OE}$ is masked during the data portion of a Write sequence, during the first clock when emerging from a deselected state and when the device has been deselected.
$\overline{CEN}$	Input-Synchronous	**Clock enable input, active LOW**. When asserted LOW the clock signal is recognized by the SRAM. When deasserted HIGH the clock signal is masked. Since deasserting $\overline{CEN}$ does not deselect the device, $\overline{CEN}$ can be used to extend the previous cycle when required.
DQa DQb DQc DQd	I/O-Synchronous	**Bidirectional Data I/O lines**. As inputs, they feed into an on-chip data register that is triggered by the rising edge of CLK. As outputs, they deliver the data contained in the memory location specified by A_X during the previous clock rise of the Read cycle. The direction of the pins is controlled by $\overline{OE}$ and the internal control logic. When $\overline{OE}$ is asserted LOW, the pins can behave as outputs. When HIGH, DQa–DQd are placed in a three-state condition. The outputs are automatically three-stated during the data portion of a Write sequence, during the first clock when emerging from a deselected state, and when the device is deselected, regardless of the state of $\overline{OE}$.DQ a, b, c and d are eight-bits wide.
DPa DPb DPc DPd	I/O-Synchronous	**Bidirectional Data Parity I/O lines**. Functionally, these signals are identical to DQ[31:0]. During Write sequences, DPa is controlled by $\overline{BWS}$a, DPb is controlled by $\overline{BWS}$b, DPc is controlled by $\overline{BWS}$c, and DPd is controlled by $\overline{BWS}$d.DP a, b, c and d are one-bit wide
ZZ	Input-Asynchronous	**ZZ "sleep" input**. This active HIGH input places the device in a non-time critical "sleep" condition with data integrity preserved.
MODE	Input Pin	**Mode input**. Selects the burst order of the device. Tied HIGH selects the interleaved burst order. Pulled LOW selects the linear burst order. **MODE should not change states during operation.** When left floating MODE will default HIGH, to an interleaved burst order.
V_{DD}	Power Supply	**Power supply inputs to the core of the device**.
V_{DDQ}	I/O Power Supply	**Power supply for the I/O circuitry**.
TDO	JTAG serial output Synchronous	**Serial data-out to the JTAG circuit**. Delivers data on the negative edge of TCK (BGA only).

Pin Definitions

Name	I/O Type	Description
TDI	JTAG serial input Synchronous	**Serial data-In to the JTAG circuit**. Sampled on the rising edge of TCK.(BGA Only)
TMS	Test Mode Select Synchronous	**This pin controls the Test Access Port (TAP) state machine**. Sampled on the rising edge of TCK (BGA only).
TCK	JTAG serial clock	**Serial clock to the JTAG circuit** (BGA only).
32M 64M 128M	–	**No connects**. Reserved for address expansion. Pins are not internally connected.
V_{SS}	Ground	**Ground for the device**. Should be connected to ground of the system.
NC	–	**No connects**. Pins are not internally connected.
DNU	–	**Do not use pins**.

Introduction

Functional Overview

The CY7C1370B/CY7C1372B are synchronous-pipelined Burst NoBL™ SRAMs designed specifically to eliminate wait states during Write/Read transitions. All synchronous inputs pass through input registers controlled by the rising edge of the clock. The clock signal is qualified with the $\overline{CEN}$ input signal. If $\overline{CEN}$ is HIGH, the clock signal is not recognized and all internal states are maintained. All synchronous operations are qualified with $\overline{CEN}$. All data outputs pass through output registers controlled by the rising edge of the clock. Maximum access delay from the clock rise (t_{CO}) is 3.8 ns (150-MHz device).

Accesses can be initiated by asserting all three Chip Enables ($\overline{CE_1}$, CE_2, $\overline{CE_3}$) active at the rising edge of the clock. If the $\overline{CEN}$ is active LOW and ADV/$\overline{LD}$ is asserted LOW, the address presented to the device will be latched. The access can either be a Read or Write operation, depending on the status of the Write enable ($\overline{WE}$). $\overline{BWS_{[d:a]}}$ can be used to conduct byte Write operations.

Write operations are qualified by the Write enable ($\overline{WE}$). All writes are simplified with on-chip synchronous self-timed write circuitry.

Three synchronous $\overline{CE_1}$, CE_2, $\overline{CE_3}$ and an asynchronous $\overline{OE}$ simplify depth expansion. All operations (Reads, Writes, and Deselects) are pipelined. ADV/$\overline{LD}$ should be driven LOW once the device has been deselected in order to load a new address for the next operation.

Single Read Accesses

A Read access is initiated when the following conditions are satisfied at clock rise: (1) $\overline{CEN}$ is asserted LOW, (2) $\overline{CE_1}$, CE_2, and $\overline{CE_3}$ are ALL asserted active, (3) the Write enable input signal $\overline{WE}$ is deasserted HIGH, and (4) ADV/$\overline{LD}$ is asserted LOW. The address presented to the address inputs is latched into the Address Register and presented to the memory core and control logic. The control logic determines that a Read access is in progress and allows the requested data to propagate to the input of the output register. At the rising edge of the next clock the requested data is allowed to propagate through the output register and onto the data bus within 3.8 ns (150-MHz device) provided $\overline{OE}$ is active LOW. After the first clock of the Read access the output buffers are controlled by $\overline{OE}$ and the internal control logic. $\overline{OE}$ must be driven LOW in order for the device to drive out the requested data. During the second clock, a subsequent operation (Read/Write/Deselect) can be initiated. Deselecting the device is also pipelined. Therefore, when the SRAM is deselected at clock rise by one of the chip enable signals, its output will three-state following the next clock rise.

Burst Read Accesses

The CY7C1370B/CY7C1372B have on-chip burst counters that allow the user the ability to supply a single address and conduct up to four Reads without reasserting the address inputs. ADV/$\overline{LD}$ must be driven LOW in order to load a new address into the SRAM, as described in the Single Read Access section above. The sequence of the burst counter is determined by the MODE input signal. A LOW input on MODE selects a linear burst mode, a HIGH selects an interleaved burst sequence. Both burst counters use A0 and A1 in the burst sequence, and will wrap-around when incremented sufficiently. A HIGH input on ADV/$\overline{LD}$ will increment the internal burst counter regardless of the state of chip enables inputs or $\overline{WE}$. $\overline{WE}$ is latched at the beginning of a burst cycle. Therefore, the type of access (Read or Write) is maintained throughout the burst sequence.

Single Write Accesses

Write access are initiated when the following conditions are satisfied at clock rise: (1) $\overline{CEN}$ is asserted LOW, (2) $\overline{CE_1}$, CE_2, and $\overline{CE_3}$ are ALL asserted active, and (3) the Write signal $\overline{WE}$ is asserted LOW. The address presented to A_x is loaded into the Address Register. The Write signals are latched into the Control Logic block.

On the subsequent clock rise the data lines are automatically three-stated regardless of the state of the $\overline{OE}$ input signal. This allows the external logic to present the data on DQ and DQP ($DQ_{a,b,c,d}$/$DP_{a,b,c,d}$ for CY7C1370B and $DQ_{a,b}$/$DP_{a,b}$ for CY7C1372B). In addition, the address for the subsequent access (Read/Write/Deselect) is latched into the Address Register (provided that the appropriate control signals are asserted).

On the next clock rise the data presented to DQ and DP ($DQ_{a,b,c,d}$/$DP_{a,b,c,d}$ for CY7C1370B and $DQ_{a,b}$/$DP_{a,b}$ for CY7C1372B) (or a subset for byte Write operations, see Write Cycle Description table for details) inputs is latched into the device and the Write is complete.

The data written during the Write operation is controlled by $\overline{BWS}$ ($\overline{BWS_{a,b,c,d}}$ for CY7C1370B and $\overline{BWS_{a,b}}$ for CY7C1372B) signals. The CY7C1370B/CY7C1372B provides byte Write capability that is described in the Write Cycle Description table. Asserting the Write enable input ($\overline{WE}$) with the selected Byte Write Select ($\overline{BWS}$) input will selectively write to only the desired bytes. Bytes not selected during a byte Write operation will remain unaltered. A synchronous self-timed Write mechanism has been provided to simplify Write operations. Byte Write capability has been included in order to greatly simplify Read/Modify/Write sequences, which can be reduced to simple byte Write operations.

Because the CY7C1370B/CY7C1372B is a common I/O device, data should not be driven into the device while the outputs are active. The $\overline{OE}$ can be deasserted HIGH before presenting data to the DQ and DP ($DQ_{a,b,c,d}$/$DP_{a,b,c,d}$ for CY7C1370B and $DQ_{a,b}$/$DP_{a,b}$ for CY7C1372B) inputs. Doing so will three-state the output drivers. As a safety precaution, DQ and DP ($DQ_{a,b,c,d}$/$DP_{a,b,c,d}$ for CY7C1370B and $DQ_{a,b}$/$DP_{a,b}$ for CY7C1372B) are automatically three-stated during the data portion of a Write cycle, regardless of the state of $\overline{OE}$.

Burst Write Accesses

The CY7C1370B/CY7C1372B has an on-chip burst counter that allows the user the ability to supply a single address and conduct up to four Write operations without reasserting the address inputs. ADV/$\overline{LD}$ must be driven LOW in order to load the initial address, as described in the Single Write Access section above. When ADV/$\overline{LD}$ is driven HIGH on the subsequent clock rise, the chip enables ($\overline{CE_1}$, CE_2, and $\overline{CE_3}$) and $\overline{WE}$ inputs are ignored and the burst counter is incremented. The correct $\overline{BWS}$ ($\overline{BWS_{a,b,c,d}}$ for CY7C1370B and $\overline{BWS_{a,b}}$ for CY7C1372B) inputs must be driven in each cycle of the burst Write in order to write the correct bytes of data.

Cycle Description Truth Table[1, 2, 3, 4, 5, 6]

Operation	Address Used	$\overline{CE}$	$\overline{CEN}$	ADV/ LD/	$\overline{WE}$	$\overline{BWS_X}$	CLK	Comments
Deselected	External	1	0	L	X	X	L–H	I/Os three-state following next recognized clock.
Suspend	–	X	1	X	X	X	L–H	Clock ignored, all operations suspended.
Begin Read	External	0	0	0	1	X	L–H	Address latched.
Begin Write	External	0	0	0	0	Valid	L–H	Address latched, data presented two valid clocks later.
Burst Read Operation	Internal	X	0	1	X	X	L–H	Burst Read operation. Previous access was a Read operation. Addresses incremented internally in conjunction with the state of Mode.
Burst Write Operation	Internal	X	0	1	X	Valid	L–H	Burst Write operation. Previous access was a Write operation. Addresses incremented internally in conjunction with the state of MODE. Bytes written are determined by $\overline{BWS}_{[d:a]}$.

Interleaved Burst Sequence

First Address	Second Address	Third Address	Fourth Address
A[1:0]	A[1:0]	A[1:0]	A[1:0]
00	01	10	11
01	00	11	10
10	11	00	01
11	10	01	00

Linear Burst Sequence

First Address	Second Address	Third Address	Fourth Address
A[1:0]	A[1:0]	A[1:0]	A[1:0]
00	01	10	11
01	10	11	00
10	11	00	01
11	00	01	10

Notes:
1. X = “Don't Care,” 1 = Logic HIGH, 0 = Logic LOW, $\overline{CE}$ stands for ALL Chip Enables active. $\overline{BWS}_X$ = 0 signifies at least one byte Write Select is active; $\overline{BWS}_X$ = Valid signifies that the desired byte Write selects are asserted. See Write Cycle Description table for details.
2. Write is defined by $\overline{WE}$ and $\overline{BWS}_X$. See Write Cycle Description table for details.
3. The DQ and DP pins are controlled by the current cycle and the $\overline{OE}$ signal.
4. CEN = 1 inserts wait states.
5. Device will power-up deselected and the I/Os in a three-state condition, regardless of $\overline{OE}$.
6. OE assumed LOW.

Sleep Mode

The ZZ input pin is an asynchronous input. Asserting ZZ places the SRAM in a power conservation “sleep” mode. Two clock cycles are required to enter into or exit from this “sleep” mode. While in this mode, data integrity is guaranteed. Accesses pending when entering the “sleep” mode are not considered valid nor is the completion of the operation guaranteed. The device must be deselected prior to entering the “sleep” mode. $\overline{CE}$s, $\overline{ADSP}$, and $\overline{ADSC}$ must remain inactive for the duration of t_{ZZREC} after the ZZ input returns LOW.

ZZ Mode Electrical Characteristics

Parameter	Description	Test Conditions	Min.	Max.	Unit
I_{DDZZ}	Sleep mode standby current	ZZ ≥ V_{DD} – 0.2V		20	mA
t_{ZZS}	Device operation to ZZ	ZZ ≥ V_{DD} – 0.2V		$2t_{CYC}$	ns
t_{ZZREC}	ZZ recovery time	ZZ ≤ 0.2V	$2t_{CYC}$		ns

Write Cycle Descriptions[1, 2]

Function (CY7C1370B)	$\overline{WE}$	$\overline{BWS_d}$	$\overline{BWS_c}$	$\overline{BWS_b}$	$\overline{BWS_a}$
Read	1	X	X	X	X
Write - No bytes written	0	1	1	1	1
Write Byte 0 - (DQa and DPa)	0	1	1	1	0
Write Byte 1 - (DQb and DPb)	0	1	1	0	1
Write Bytes 1, 0	0	1	1	0	0
Write Byte 2 - (DQc and DPc)	0	1	0	1	1
Write Bytes 2, 0	0	1	0	1	0
Write Bytes 2, 1	0	1	0	0	1
Write Bytes 2, 1, 0	0	1	0	0	0
Write Byte 3 - (DQd and DPd)	0	0	1	1	1
Write Bytes 3, 0	0	0	1	1	0
Write Bytes 3, 1	0	0	1	0	1
Write Bytes 3, 1, 0	0	0	1	0	0
Write Bytes 3, 2	0	0	0	1	1
Write Bytes 3, 2, 0	0	0	0	1	0
Write Bytes 3, 2, 1	0	0	0	0	1
Write All Bytes	0	0	0	0	0

Function (CY7C1372B)	$\overline{WE}$	$\overline{BWS_b}$	$\overline{BWS_a}$
Read	1	x	x
Write - No Bytes Written	0	1	1
Write Byte 0 - (DQa and DPa)	0	1	0
Write Byte 1 - (DQb and DPb)	0	0	1
Write Both Bytes	0	0	0

IEEE 1149.1 Serial Boundary Scan (JTAG)

The CY7C1370B/CY7C1372B incorporates a serial boundary scan Test Access Port (TAP) in the BGA package only. The TQFP package does not offer this functionality. This port operates in accordance with IEEE Standard 1149.1–1900, but does not have the set of functions required for full 1149.1 compliance. These functions from the IEEE specification are excluded because their inclusion places an added delay in the critical speed path of the SRAM. Note that the TAP controller functions in a manner that does not conflict with the operation of other devices using fully 1149.1-compliant TAPs. The TAP operates using JEDEC standard 3.3V I/O logic levels.

Disabling the JTAG Feature

It is possible to operate the SRAM without using the JTAG feature. To disable the TAP controller, TCK must be tied LOW (V_{SS}) to prevent clocking of the device. TDI and TMS are internally pulled up and may be unconnected. They may alternately be connected to V_{DD} through a pull-up resistor. TDO should be left unconnected. Upon power-up, the device will come up in a reset state which will not interfere with the operation of the device.

Test Access Port—Test Clock

The test clock is used only with the TAP controller. All inputs are captured on the rising edge of TCK. All outputs are driven from the falling edge of TCK.

Test Mode Select

The TMS input is used to give commands to the TAP controller and is sampled on the rising edge of TCK. It is allowable to leave this pin unconnected if the TAP is not used. The pin is pulled up internally, resulting in a logic HIGH level.

Test Data-In (TDI)

The TDI pin is used to serially input information into the registers and can be connected to the input of any of the registers. The register between TDI and TDO is chosen by the instruction that is loaded into the TAP instruction register. For information on loading the instruction register, see the TAP Controller State Diagram. TDI is internally pulled up and can be unconnected if the TAP is unused in an application. TDI is connected to the most significant bit (MSB) on any register.

Test Data-Out (TDO)

The TDO output pin is used to serially clock data-out from the registers. The output is active depending upon the current state of the TAP state machine (see TAP Controller State Diagram). The output changes on the falling edge of TCK. TDO is connected to the least significant bit (LSB) of any register.

Performing a TAP Reset

A Reset is performed by forcing TMS HIGH (V_{DD}) for five rising edges of TCK. This RESET does not affect the operation of the SRAM and may be performed while the SRAM is operating. At power-up, the TAP is reset internally to ensure that TDO comes up in a High-Z state.

TAP Registers

Registers are connected between the TDI and TDO pins and allow data to be scanned into and out of the SRAM test circuitry. Only one register can be selected at a time through the instruction registers. Data is serially loaded into the TDI pin on the rising edge of TCK. Data is output on the TDO pin on the falling edge of TCK.

Instruction Register

Three-bit instructions can be serially loaded into the instruction register. This register is loaded when it is placed between the TDI and TDO pins as shown in the TAP Controller Block Diagram. Upon power-up, the instruction register is loaded with the IDCODE instruction. It is also loaded with the IDCODE instruction if the controller is placed in a reset state as described in the previous section.

When the TAP controller is in the CaptureIR state, the two least significant bits are loaded with a binary “01” pattern to allow for fault isolation of the board level serial test path.

Bypass Register

To save time when serially shifting data through registers, it is sometimes advantageous to skip certain states. The bypass register is a single-bit register that can be placed between TDI and TDO pins. This allows data to be shifted through the SRAM with minimal delay. The bypass register is set LOW (V_{SS}) when the BYPASS instruction is executed.

Boundary Scan Register

The boundary scan register is connected to all the I/O pins on the SRAM. Several no connect (NC) pins are also included in the scan register to reserve pins for higher density devices. The ×36 configuration has a 70-bit-long register, and the ×18 configuration has a 51-bit-long register.

The boundary scan register is loaded with the contents of the RAM I/O ring when the TAP controller is in the Capture-DR state and is then placed between the TDI and TDO pins when the controller is moved to the Shift-DR state. The EXTEST, SAMPLE/PRELOAD and SAMPLE Z instructions can be used to capture the contents of the I/O ring.

The Boundary Scan Order tables show the order in which the bits are connected. Each bit corresponds to one of the bumps on the SRAM package. The MSB of the register is connected to TDI, and the LSB is connected to TDO.

Identification (ID) Register

The ID register is loaded with a vendor-specific, 32-bit code during the Capture-DR state when the IDCODE command is loaded in the instruction register. The IDCODE is hardwired into the SRAM and can be shifted out when the TAP controller is in the Shift-DR state. The ID register has a vendor code and other information described in the Identification Register Definitions table.

TAP Instruction Set

Eight different instructions are possible with the three-bit instruction register. All combinations are listed in the Instruction Code table. Three of these instructions are listed as RESERVED and should not be used. The other five instructions are described in detail below.

The TAP controller used in this SRAM is not fully compliant with the 1149.1 convention because some of the mandatory 1149.1 instructions are not fully implemented. The TAP controller cannot be used to load address, data, or control signals into the SRAM and cannot preload the I/O buffers. The

SRAM does not implement the 1149.1 commands EXTEST or INTEST or the PRELOAD portion of SAMPLE/PRELOAD; rather it performs a capture of the I/O ring when these instructions are executed.

Instructions are loaded into the TAP controller during the Shift-IR state when the instruction register is placed between TDI and TDO. During this state, instructions are shifted through the instruction register through the TDI and TDO pins. To execute the instruction once it is shifted in, the TAP controller needs to be moved into the Update-IR state.

EXTEST

EXTEST is a mandatory 1149.1 instruction which is to be executed whenever the instruction register is loaded with all 0s. EXTEST is not implemented in the TAP controller, and therefore this device is not compliant with the 1149.1 standard.

The TAP controller does recognize an all-0 instruction. When an EXTEST instruction is loaded into the instruction register, the SRAM responds as if a SAMPLE/PRELOAD instruction has been loaded. There is one difference between the two instructions. Unlike the SAMPLE/PRELOAD instruction, EXTEST places the SRAM outputs in a High-Z state.

IDCODE

The IDCODE instruction causes a vendor-specific, 32-bit code to be loaded into the instruction register. It also places the instruction register between the TDI and TDO pins and allows the IDCODE to be shifted out of the device when the TAP controller enters the Shift-DR state. The IDCODE instruction is loaded into the instruction register upon power-up or whenever the TAP controller is given a test logic reset state.

SAMPLE Z

The SAMPLE Z instruction causes the boundary scan register to be connected between the TDI and TDO pins when the TAP controller is in a Shift-DR state. It also places all SRAM outputs into a High-Z state.

SAMPLE/PRELOAD

SAMPLE/PRELOAD is a 1149.1 mandatory instruction. The PRELOAD portion of this instruction is not implemented, so the TAP controller is not fully 1149.1-compliant.

When the SAMPLE/PRELOAD instructions are loaded into the instruction register and the TAP controller is in the Capture-DR state, a snapshot of data on the inputs and output pins is captured in the boundary scan register.

The user must be aware that the TAP controller clock can only operate at a frequency up to 10 MHz, while the SRAM clock operates more than an order of magnitude faster. Because there is a large difference in the clock frequencies, it is possible that during the Capture-DR state, an input or output will undergo a transition. The TAP may then try to capture a signal while in transition (metastable state). This will not harm the device, but there is no guarantee as to the value that will be captured. Repeatable results may not be possible.

To guarantee that the boundary scan register will capture the correct value of a signal, the SRAM signal must be stabilized long enough to meet the TAP controller's capture set-up plus hold times (t_{CS} and t_{CH}). The SRAM clock input might not be captured correctly if there is no way in a design to stop (or slow) the clock during a SAMPLE/PRELOAD instruction. If this is an issue, it is still possible to capture all other signals and simply ignore the value of the CK and CK# captured in the boundary scan register.

Once the data is captured, it is possible to shift out the data by putting the TAP into the Shift-DR state. This places the boundary scan register between the TDI and TDO pins.

Note that since the PRELOAD part of the command is not implemented, putting the TAP into the Update to the Update-DR state while performing a SAMPLE/PRELOAD instruction will have the same effect as the Pause-DR command.

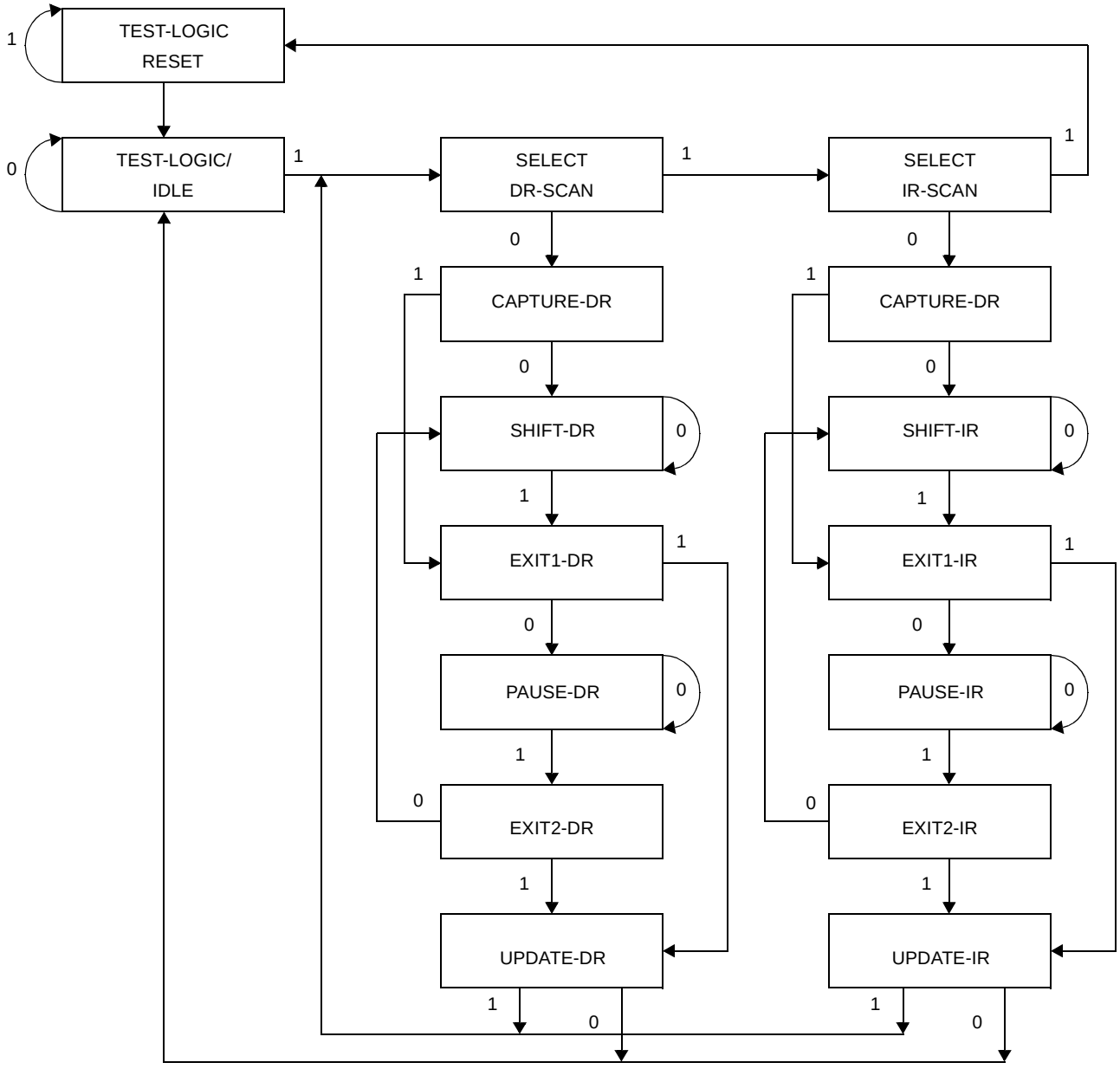
Bypass

When the BYPASS instruction is loaded in the instruction register and the TAP is placed in a Shift-DR state, the bypass register is placed between the TDI and TDO pins. The advantage of the BYPASS instruction is that it shortens the boundary scan path when multiple devices are connected together on a board.

Reserved

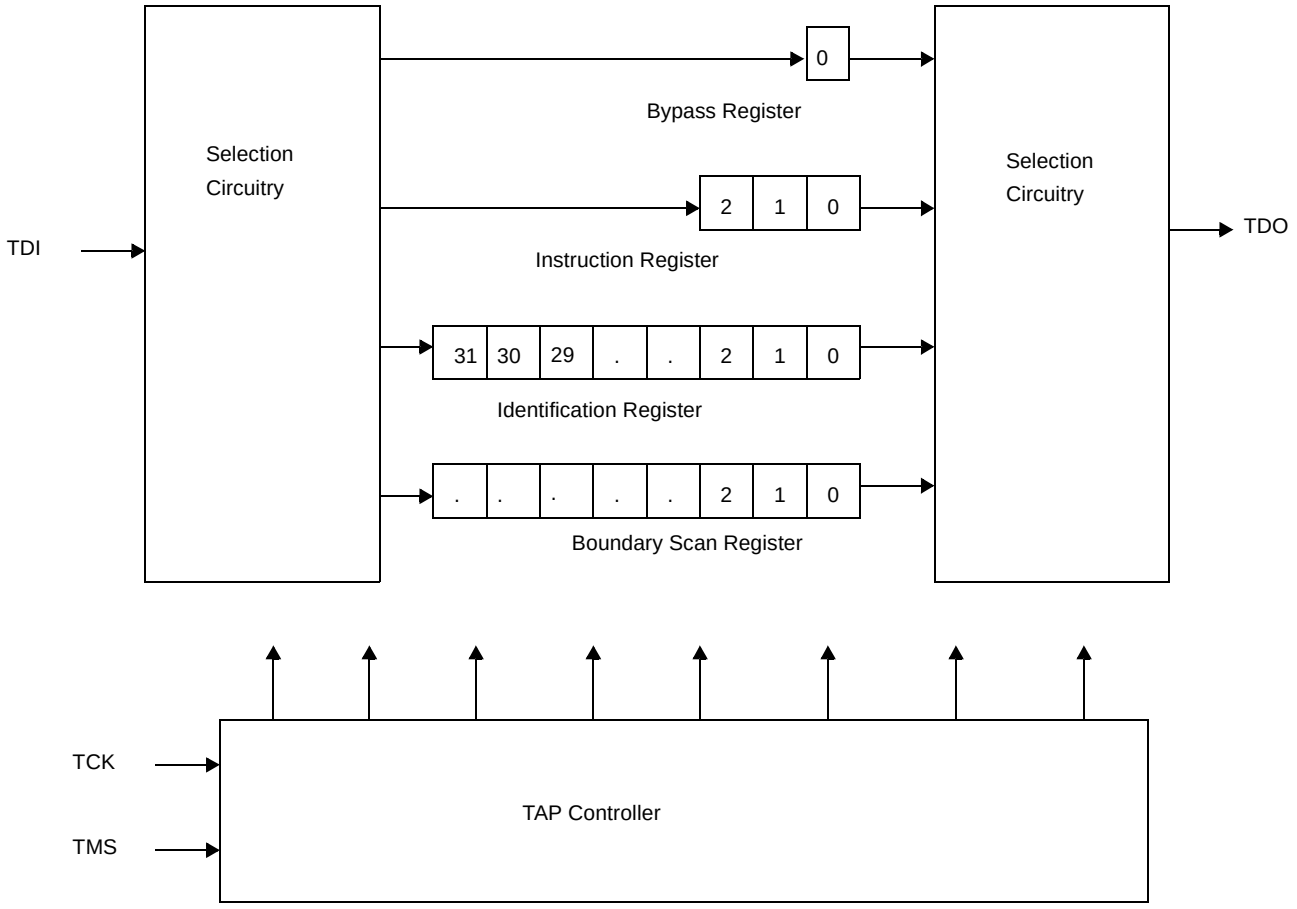
These instructions are not implemented but are reserved for future use. Do not use these instructions.

TAP Controller State Diagram



Note:
7. The 0/1 next to each state represents the value at TMS at the rising edge of TCK.

TAP Controller Block Diagram



TAP Electrical Characteristics Over the Operating Range[8, 9]

Parameter	Description	Test Conditions	Min.	Max.	Unit
V_{OH1}	Output HIGH Voltage	I_{OH} = –4.0 mA	2.4		V
V_{OH2}	Output HIGH Voltage	I_{OH} = –100 µA	V_{DD} – 0.2		V
V_{OL1}	Output LOW Voltage	I_{OL} = 8.0 mA		0.4	V
V_{OL2}	Output LOW Voltage	I_{OL} = 100 µA		0.2	V
V_{IH}	Input HIGH Voltage		1.7	V_{DD} + 0.3	V
V_{IL}	Input LOW Voltage		–0.5	0.7	V
I_X	Input Load Current	GND ≤ V_I ≤ V_{DDQ}	–5	5	µA

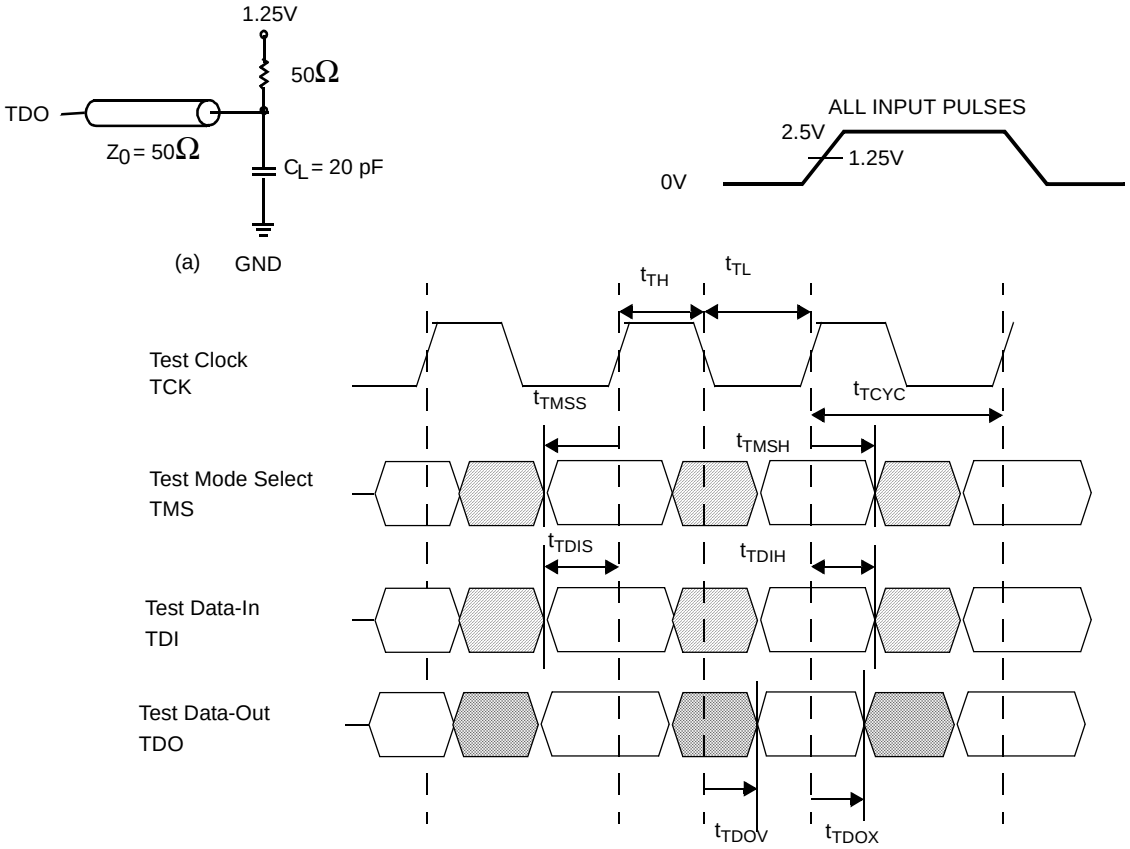
Notes:
8. All Voltage referenced to Ground.
9. Overshoot: $V_{IH}(AC) \leq V_{DD}+1.5V$ for $t \leq t_{TCYC}/2$, Undershoot: $V_{IL}(AC) \leq 0.5V$ for $t \leq t_{TCYC}/2$, Power-up: $V_{IH}<2.6V$ and $V_{DD}<2.4V$ and $V_{DDQ}<1.4V$ for $t<200$ ms.

TAP AC Switching Characteristics Over the Operating Range[10, 11]

Parameter	Description	Min.	Max	Unit
t_{TCYC}	TCK Clock Cycle Time	100		ns
t_{TF}	TCK Clock Frequency		10	MHz
t_{TH}	TCK Clock HIGH	40		ns
t_{TL}	TCK Clock LOW	40		ns
Set-up Times				
t_{TMSS}	TMS Set-up to TCK Clock Rise	10		ns
t_{TDIS}	TDI Set-up to TCK Clock Rise	10		ns
t_{CS}	Capture Set-up to TCK Rise	10		ns
Hold Times				
t_{TMSH}	TMS Hold after TCK Clock Rise	10		ns
t_{TDIH}	TDI Hold after Clock Rise	10		ns
t_{CH}	Capture Hold after clock rise	10		ns
Output Times				
t_{TDOV}	TCK Clock LOW to TDO Valid		20	ns
t_{TDOX}	TCK Clock LOW to TDO Invalid	0		ns

Notes:
10. t_{CS} and t_{CH} refer to the set-up and hold time requirements of latching data from the boundary scan register.
11. Test conditions are specified using the load in TAP AC test conditions. t_R/t_F = 1 ns.

TAP Timing and Test Conditions



Identification Register Definitions

Instruction Field	512K × 36	1M × 18	Description
Revision Number (31:28)	xxxx	xxxx	Reserved for version number
Device Depth (27:23)	00111	01000	Defines depth of SRAM. 512K or 1M
Device Width (22:18)	00100	00011	Defines width of the SRAM. ×36 or ×18
Cypress Device ID (17:12)	xxxxx	xxxxx	Reserved for future use
Cypress JEDEC ID (11:1)	00011100100	00011100100	Allows unique identification of SRAM vendor

Scan Register sizes

Register Name	Bit Size (×18)	Bit Size (×36)
Instruction	3	3
Bypass	1	1
ID	32	32
Boundary Scan	51	70

Identification Codes

Instruction	Code	Description
EXTEST	000	Captures the I/O ring contents. Places the boundary scan register between the TDI and TDO. Forces all SRAM outputs to High-Z state. This instruction is not 1149.1-compliant.
IDCODE	001	Loads the ID register with the vendor ID code and places the register between TDI and TDO. This operation does not affect SRAM operation.
SAMPLE Z	010	Captures the I/O contents. Places the boundary scan register between TDI and TDO. Forces all SRAM output drivers to a High-Z state.
RESERVED	011	Do Not Use. This instruction is reserved for future use.
SAMPLE/PRELOAD	100	Captures the I/O ring contents. Places the boundary scan register between TDI and TDO. Does not affect the SRAM operation. This instruction does not implement 1149.1 preload function and is therefore not 1149.1-compliant.
RESERVED	101	Do Not Use. This instruction is reserved for future use.
RESERVED	110	Do Not Use. This instruction is reserved for future use.
BYPASS	111	Places the bypass register between TDI and TDO. This operation does not affect SRAM operation.

Boundary Scan Order (512K × 36)

Bit #	Signal Name	Bump ID	Bit #	Signal Name	Bump ID
1	A	2R	36	$\overline{CE}_3$	6B
2	A	3T	37	$\overline{BWS}$a	5L
3	A	4T	38	$\overline{BWS}$b	5G
4	A	5T	39	$\overline{BWS}$c	3G
5	A	6R	40	$\overline{BWS}$d	3L
6	A	3B	41	CE_2	2B
7	A	5B	42	$\overline{CE}_1$	4E
8	DPa	6P	43	A	3A
9	DQa	7N	44	A	2A
10	DQa	6M	45	DPc	2D
11	DQa	7L	46	DQc	1E
12	DQa	6K	47	DQc	2F
13	DQa	7P	48	DQc	1G
14	DQa	6N	49	DQc	1D
15	DQa	6L	50	DQc	1D
16	DQa	7K	51	DQc	2E
17	NC	7T	52	DQc	2G
18	DQb	6H	53	DQc	1H
19	DQb	7G	54	$\overline{SN}$	5R
20	DQb	6F	55	DQd	2K
21	DQb	7E	56	DQd	1L
22	DQb	6D	57	DQd	2M
23	DQb	7H	58	DQd	1N
24	DQb	6G	59	DQd	2P
25	DQb	6E	60	DQd	1K
26	DPb	7D	61	DQd	2L
27	A	6A	62	DQd	2N
28	A	5A	63	DPd	1P
29	A	4G	64	MODE	3R
30	A	4A	65	A	2C
31	ADV/$\overline{LD}$	4B	66	A	3C
32	OE#	4F	67	A	5C
33	CEN#	4M	68	A	6C
34	WE#	4H	69	A1	4N
35	CLK	4K	70	A0	4P

Boundary Scan Order (1M × 18)

Bit #	Signal Name	Bump ID	Bit #	Signal Name	Bump ID
1	A	2R	36	DQb	2E
2	A	2T	37	DQb	2G
3	A	3T	38	DQb	1H
4	A	5T	39	$\overline{SN}$	5R
5	A	6R	40	DQb	2K
6	A	3B	41	DQb	1L
7	A	5B	42	DQb	2M
8	DQa	7P	43	DQb	1N
9	DQa	6N	44	DPb	2P
10	DQa	6L	45	MODE	3R
11	DQa	7K	46	A	2C
12	NC	7T	47	A	3C
13	DQa	6H	48	A	5C
14	DQa	7G	49	A	6C
15	DQa	6F	50	A1	4N
16	DQa	7E	51	A0	4P
17	DPa	6D			
18	A	6T			
19	A	6A			
20	A	5A			
21	A	4G			
22	A	4A			
23	ADV/$\overline{LD}$	4B			
24	$\overline{OE}$	4F			
25	$\overline{CEN}$	4M			
26	$\overline{WE}$	4H			
27	CLK	4K			
28	$\overline{CE}_3$	6B			
29	$\overline{BWS}$a	5L			
30	$\overline{BWS}$b	3G			
31	CE_2	2B			
32	$\overline{CE}_1$	4E			
33	A	3A			
34	A	2A			
35	DQb	1D			

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... –65°C to +150°C

Ambient Temperature with Power Applied..... –55°C to +125°C

Supply Voltage on V_{DD} Relative to GND ..... –0.5V to +4.6V

DC Voltage Applied to Outputs in High Z State[13]..... –0.5V to V_{DDQ} + 0.5V

DC Input Voltage[13]..... –0.5V to V_{DDQ} + 0.5V

Current into Outputs (LOW) ..... 20 mA

Static Discharge Voltage..... >1500V (per MIL-STD-883, Method 3015)

Latch-Up Current..... >200 mA

Operating Range

Range	Ambient Temperature[12]	V_{DD}[15]	V_{DDQ}[15]
Commercial	0°C to +70°C	3.3V	2.5V – 5%
Industrial	–40°C to +85°C	–5%/+10%	3.3V + 10%

Electrical Characteristics Over the Operating Range[14]

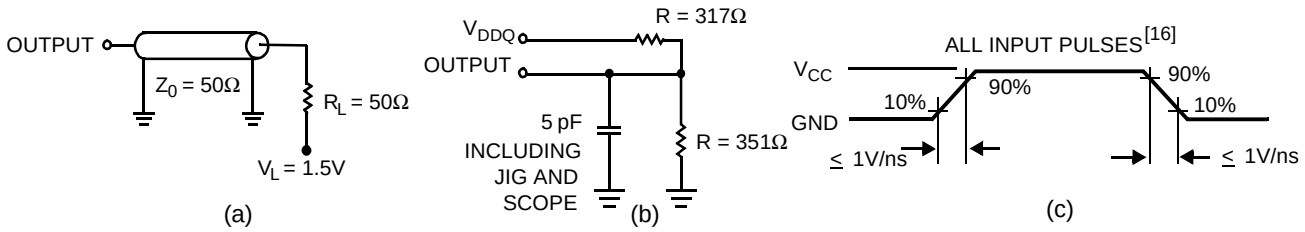
Parameter	Description	Test Conditions		Min.	Max.	Unit
V_{DD}	Power Supply Voltage			3.135	3.63	V
V_{DDQ}	I/O Supply Voltage			2.375	V_{DD}	V
V_{OH}	Output HIGH Voltage	V_{DD} = Min., I_{OH} = –1.0 mA	V_{DDQ} = 2.5V	2.0		V
		V_{DD} = Min., I_{OH} = –4.0 mA	V_{DDQ} = 3.3V	2.4		V
V_{OL}	Output LOW Voltage	V_{DD} = Min., I_{OL} = 1.0 mA	V_{DDQ} = 2.5V		0.4	V
		V_{DD} = Min., I_{OL} = 8.0 mA	V_{DDQ} = 3.3V		0.4	V
V_{IH}	Input HIGH Voltage		V_{DDQ} = 3.3V	2	V_{DD}+0.5	V
			V_{DDQ} = 2.5V	1.7	V_{DD}+0.5	V
V_{IL}	Input LOW Voltage		V_{DDQ} = 3.3V	–0.3	0.8	V
			V_{DDQ} = 2.5V	–0.3	0.7	V
I_X	Input Load Current	GND ≤ V_I ≤ V_{DDQ}			5	µA
	Input Current of MODE			–30	30	µA
	Input Current of ZZ	Input = V_{SS}		–30	30	µA
I_{OZ}	Output Leakage Current	GND ≤ V_I ≤ V_{DDQ}, Output Disabled			5	µA
I_{DD}	V_{DD} Operating Supply	V_{DD} = Max., I_{OUT} = 0 mA, f = f_{MAX} = 1/t_{CYC}	5.0-ns cycle, 200 MHz		315	mA
			6.0-ns cycle, 167 MHz		285	mA
			6.7-ns cycle, 150 MHz		265	mA
			7.5-ns cycle, 133 MHz		245	mA
I_{SB1}	Automatic CE Power-Down Current—TTL Inputs	Max. V_{DD}, Device Deselected, V_{IN} ≥ V_{IH} or V_{IN} ≤ V_{IL} f = f_{MAX} = 1/t_{CYC}	5.0-ns cycle, 200 MHz		140	mA
			6.0-ns cycle, 167 MHz		120	mA
			6.7-ns cycle, 150 MHz		110	mA
			7.5-ns cycle, 133 MHz		105	mA
I_{SB2}	Automatic CE Power-Down Current—CMOS Inputs	Max. V_{DD}, Device Deselected, V_{IN} ≤ 0.3V or V_{IN} ≥ V_{DDQ} – 0.3V, f = 0	All speed grades		20	mA
I_{SB3}	Automatic CE Power-Down Current—CMOS Inputs	Max. V_{DD}, Device Deselected, V_{IN} ≤ 0.3V or V_{IN} ≥ V_{DDQ} – 0.3V, f = 0	6.0-ns cycle, 200 MHz		110	mA
			6.0-ns cycle, 167 MHz		100	mA
			6.7-ns cycle, 150 MHz		90	mA
			7.5-ns cycle, 133 MHz		85	mA
I_{SB4}	Automatic CS Power-Down Current—TTL Inputs	Max. V_{DD}, Device Deselected, V_{IN} ≥ V_{IH} or V_{IN} ≤ V_{IL}, f = 0	All Speeds		50	mA

Notes:
12. T_A is the case temperature.
13. Minimum voltage equals -2.0V for pulse durations of less than 20 ns.
14. The load used for V_{OH} and V_{OL} testing is shown in figure (b) of the A/C test conditions.
15. Power Supply ramp up should be monotonic.

Capacitance[17]

Parameter	Description	Test Conditions	Max.	Unit
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{DD} = V_{DDQ} = 3.3V	3	pF
C_{CLK}	Clock Input Capacitance		3	pF
$C_{I/O}$	I/O Capacitance		3	pF

AC Test Loads and Waveforms



Thermal Resistance[17]

Description	Test Conditions	Q_{JA} (Junction to Ambient)	Q_{JC} (Junction to Case)	Unit
119 BGA	Still Air, soldered on a 114.3 × 101.6 × 1.57 mm3, 2-layer board	41.54	6.33	°C/W
165 FBGA		44.51	2.38	°C/W
100-pin TQFP	Still Air, soldered on a 4.25 × 1.125 inch, 4-layer printed circuit board	25	9	°C/W

Notes:
16. Input waveform should have a slew rate of ≥ 1 V/ns.
17. Tested initially and after any design or process change that may affect these parameters.

Switching Characteristics Over the Operating Range[18]

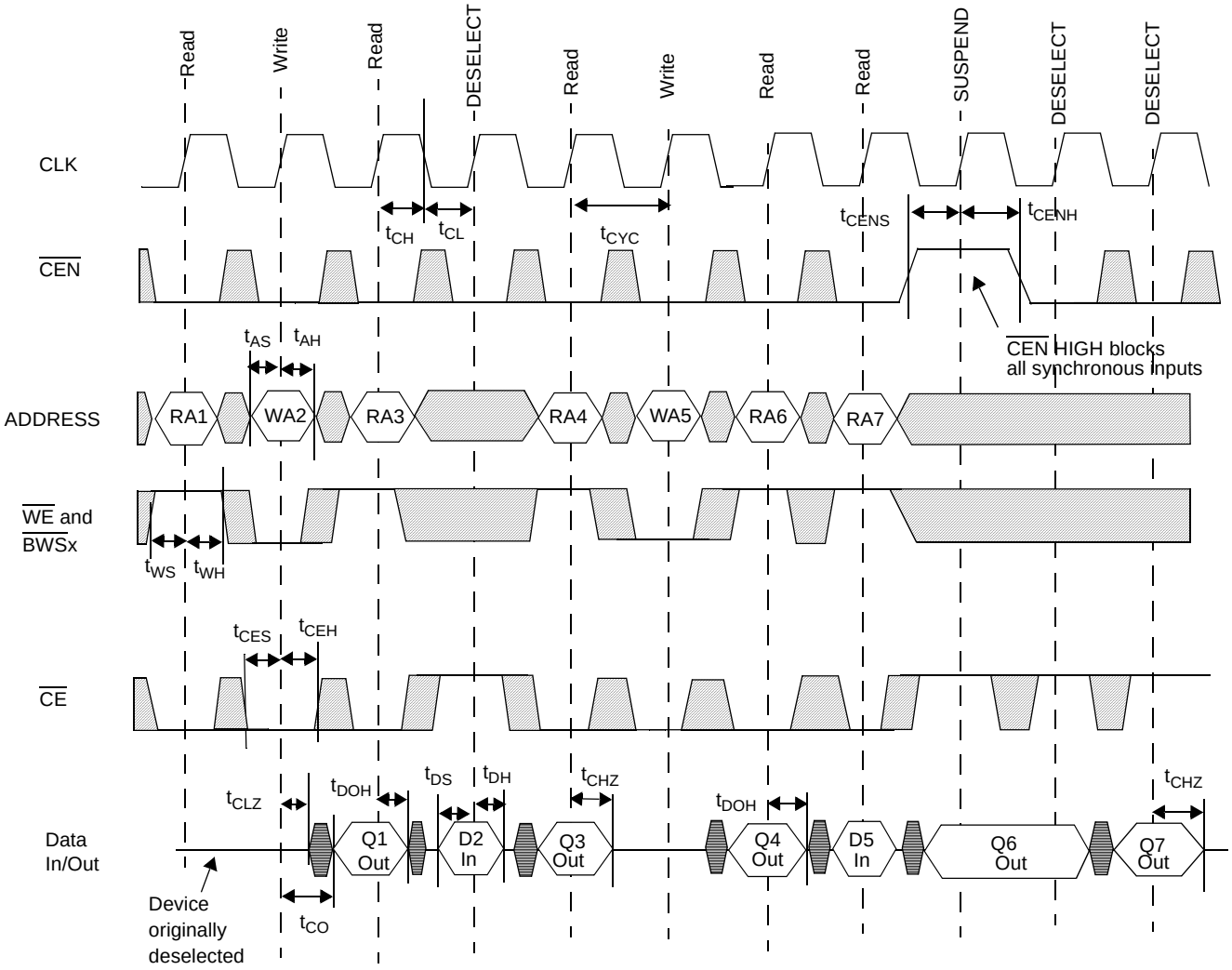
Parameter	Description	-200		-166		-150		-133		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Clock										
t_{CYC}	Clock Cycle Time	5		6.0		6.7		7.5		ns
t_{CH}	Clock HIGH	1.8		2.1		2.3		2.5		ns
t_{CL}	Clock LOW	1.8		2.1		2.3		2.5		ns
Output Times										
t_{CO}	Data Output Valid After CLK Rise		3.0		3.4		3.8		4.2	ns
t_{EOV}	$\overline{OE}$ LOW to Output Valid[17, 19, 21]		3.0		3.4		3.8		4.2	ns
t_{DOH}	Data Output Hold After CLK Rise	1.3		1.3		1.3		1.3		ns
t_{CHZ}	Clock to High-Z[17, 18, 19, 20, 21]		3.0		3.0		3.0		3.5	ns
t_{CLZ}	Clock to Low-Z[17, 18, 19, 20, 21]	1.3		1.3		1.3		1.3		ns
t_{EOHZ}	$\overline{OE}$ HIGH to Output High-Z[18, 19, 21]		4.0		4.0		4.0		4.0	ns
t_{EOLZ}	$\overline{OE}$ LOW to Output Low-Z[18, 19, 21]	0		0		0		0		ns
Set-up Times										
t_{AS}	Address Set-up Before CLK Rise	1.4		1.5		1.5		1.5		ns
t_{DS}	Data Input Set-up Before CLK Rise	1.4		1.5		1.5		1.5		ns
t_{CENS}	$\overline{CEN}$ Set-up Before CLK Rise	1.4		1.5		1.5		1.5		ns
t_{WES}	$\overline{WE}$, $\overline{BWS}_x$ Set-up Before CLK Rise	1.4		1.5		1.5		1.5		ns
t_{ALS}	ADV/$\overline{LD}$ Set-up Before CLK Rise	1.4		1.5		1.5		1.5		ns
t_{CES}	Chip Select Set-up	1.4		1.5		1.5		1.5		ns
Hold Times										
t_{AH}	Address Hold After CLK Rise	0.4		0.5		0.5		0.5		ns
t_{DH}	Data Input Hold After CLK Rise	0.4		0.5		0.5		0.5		ns
t_{CENH}	$\overline{CEN}$ Hold After CLK Rise	0.4		0.5		0.5		0.5		ns
t_{WEH}	$\overline{WE}$, $\overline{BW}_x$ Hold After CLK Rise	0.4		0.5		0.5		0.5		ns
t_{ALH}	ADV/$\overline{LD}$ Hold after CLK Rise	0.4		0.5		0.5		0.5		ns
t_{CEH}	Chip Select Hold After CLK Rise	0.4		0.5		0.5		0.5		ns

Notes:

18. Unless otherwise noted, test conditions assume signal transition time of 2.5 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V, and output loading of the specified I_{OL}/I_{OH} and load capacitance. Shown in (a), (b), and (c) of AC Test Loads.
19. t_{CHZ}, t_{CLZ}, t_{OEV}, t_{EOLZ}, and t_{EOHZ} are specified with AC test conditions shown in part (a) of AC Test Loads. Transition is measured ± 200 mV from steady-state voltage.
20. At any given voltage and temperature, t_{EOHZ} is less than t_{EOLZ} and t_{CHZ} is less than t_{CLZ} to eliminate bus contention between SRAMs when sharing the same data bus. These specifications do not imply a bus contention condition, but reflect parameters guaranteed over worst-case user conditions. Device is designed to achieve High-Z prior to Low-Z under the same system conditions.
21. This parameter is sampled and not 100% tested.

Switching Waveforms

Read/Write/DESELECT Sequence

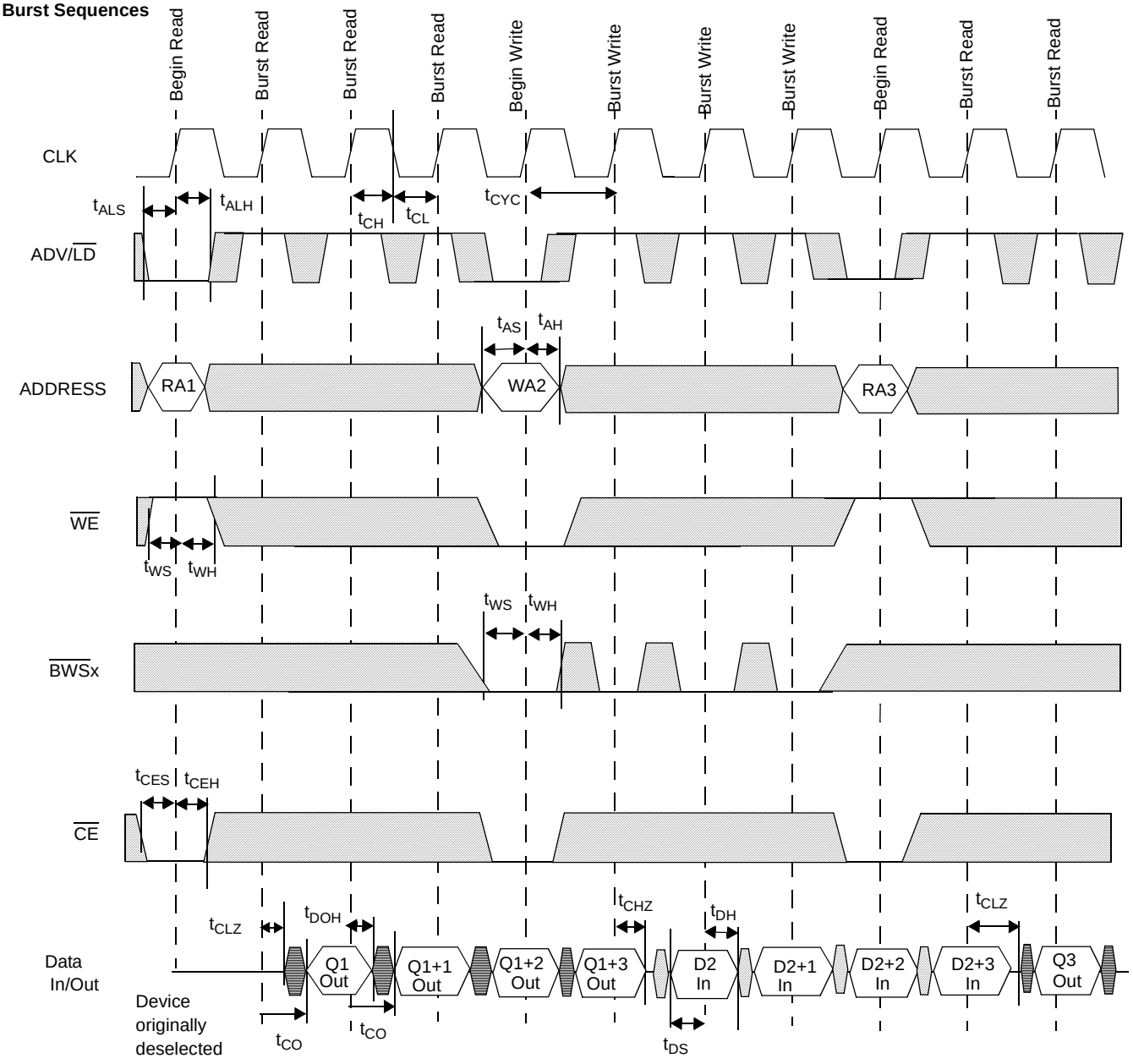


The combination of $\overline{WE}$ and $\overline{BWS}_x$ (x = a, b, c, d for CY7C1370B and x = a, b for CY7C1372B) define a Write cycle (see Write Cycle Description table). $\overline{CE}$ is the combination of $\overline{CE}_1$, CE_2, and $\overline{CE}_3$. All chip enables need to be active in order to select the device. Any chip enable can deselect the device. RAx stands for Read Address X, WAx Write Address X, Dx stands for Data-in for location X, Qx stands for Data-out for location X. ADV/$\overline{LD}$ held LOW. $\overline{OE}$ held LOW.

= Don't Care = Undefined

Switching Waveforms (continued)

Burst Sequences

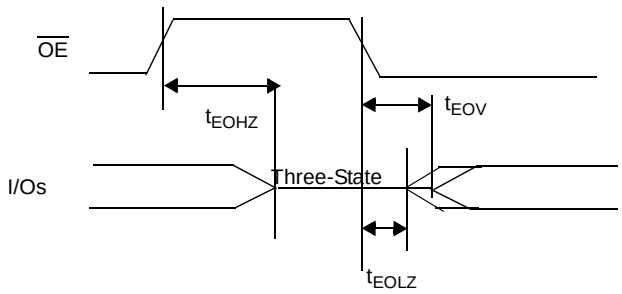


The combination of $\overline{WE}$ and $\overline{BWS}_x$ (x = a, b c, d) define a Write cycle (see Write Cycle Description table). $\overline{CE}$ is the combination of $\overline{CE}_1$, CE_2, and $\overline{CE}_3$. All chip enables need to be active in order to select the device. Any chip enable can deselect the device. RAx stands for Read Address X, WA stands for Write Address X, Dx stands for Data-in for location X, Qx stands for Data-out for location X. $\overline{CEN}$ held LOW. During burst writes, byte writes can be conducted by asserting the appropriate $\overline{BWS}_x$ input signals. Burst order determined by the state of the MODE input. $\overline{CEN}$ held LOW. $\overline{OE}$ held LOW.

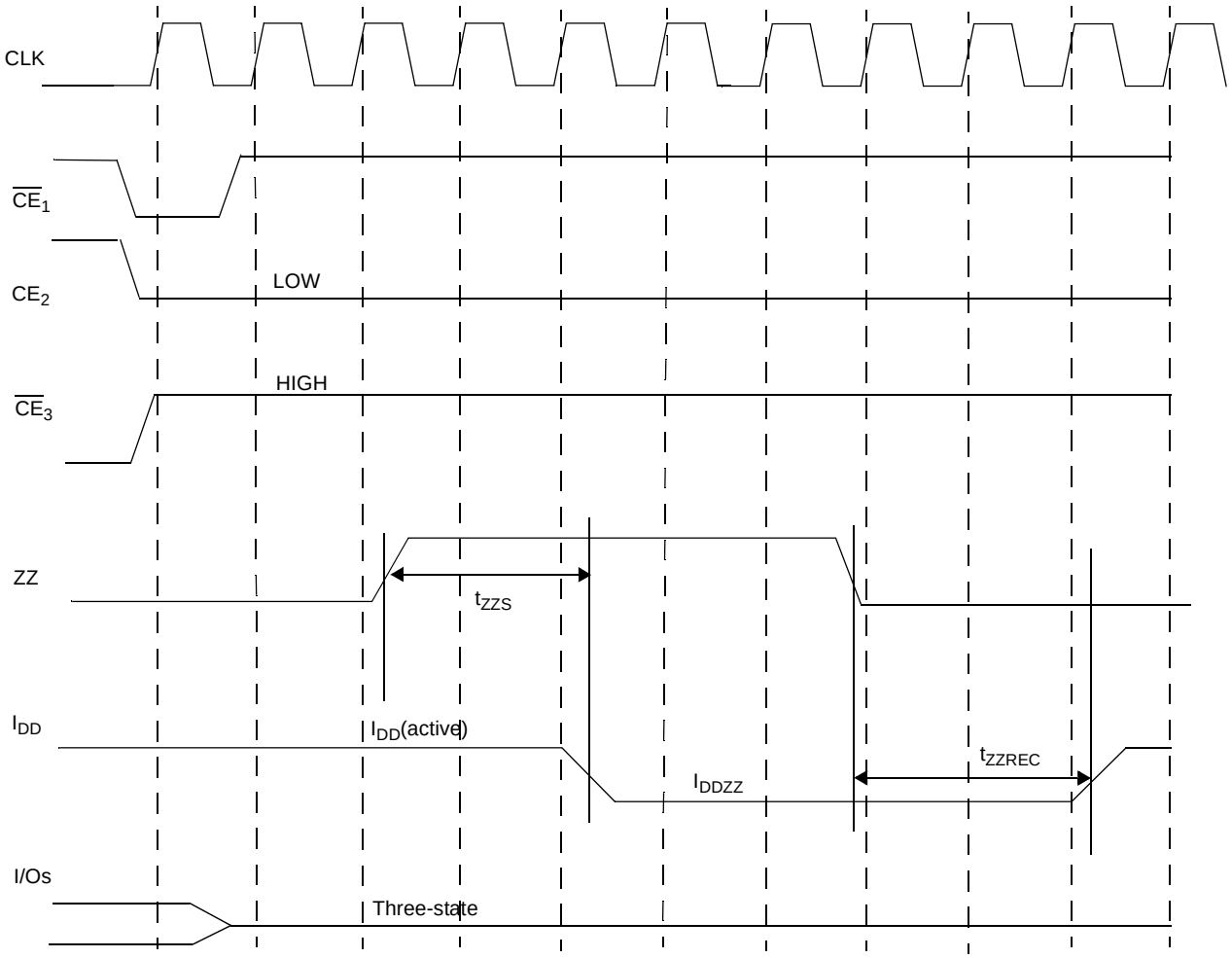
= Don't Care = Undefined

Switching Waveforms (continued)

$\overline{OE}$ Timing



ZZ Mode Timing[22, 23]



Note:
22. Device must be deselected when entering ZZ mode. See Cycle Descriptions Table for all possible signal conditions to deselect the device.
23. I/Os are in three-state when exiting ZZ sleep mode.

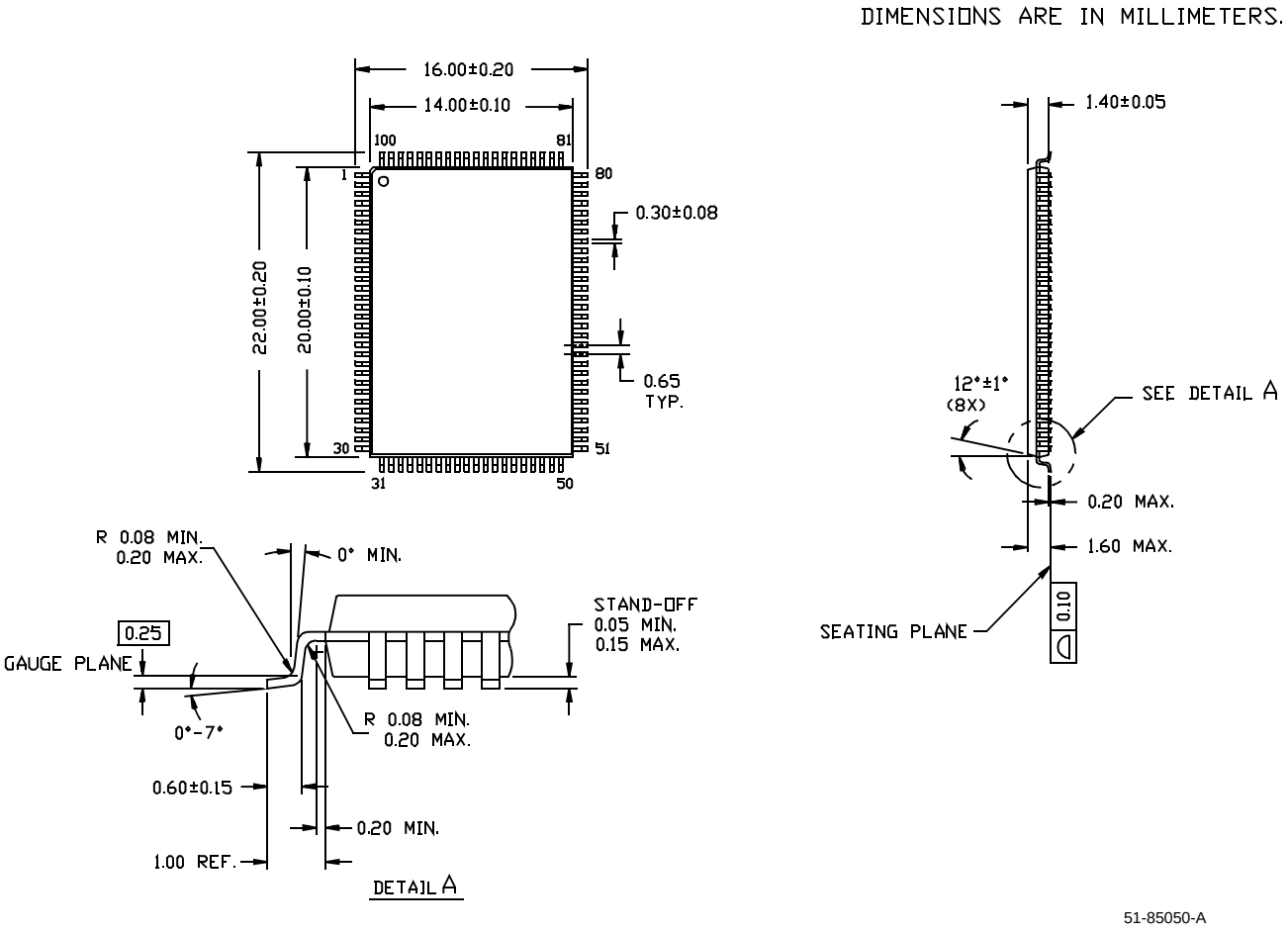
Ordering Information

Speed (MHz)	Ordering Code	Package Name	Package Type	Operating Range
200	CY7C1370B-200AC CY7C1372B-200AC	A101	100-lead Thin Quad Flat Pack	Commercial
	CY7C1370B-200BGC CY7C1372B-200BGC	BG119	119 PBGA	
	CY7C1370B-200BZC CY7C1372B-200BZC	BA165A	165 FBGA	
167	CY7C1370B-167AC CY7C1372B-167AC	A101	100-lead Thin Quad Flat Pack	
	CY7C1370B-167BGC CY7C1372B-167BGC	BG119	119 PBGA	
	CY7C1370B-167BZC CY7C1372B-167BZC	BA165A	165 FBGA	
150	CY7C1370B-150AC CY7C1372B-150AC	A101	100-lead Thin Quad Flat Pack	
	CY7C1370B-150BGC CY7C1372B-150BGC	BG119	119 PBGA	
	CY7C1370B-150BZC CY7C1372B-150BZC	BA165A	165 FBGA	
133	CY7C1370B-133AC CY7C1372B-133AC	A101	100-lead Thin Quad Flat Pack	
	CY7C1370B-133BGC CY7C1372B-133BGC	BG119	119 PBGA	
	CY7C1370B-133BZC CY7C1372B-133BZC	BA165A	165 FBGA	
167	CY7C1370B-167AI CY7C1372B-167AI	A101	100-lead Thin Quad Flat Pack	Industrial
	CY7C1370B-167BGI CY7C1372B-167BGI	BG119	119 BGA	
	CY7C1370B-167BZI CY7C1372B-167BZI	BA165A	165 FBGA	
150	CY7C1370B-150AI CY7C1372B-150AI	A101	100-lead Thin Quad Flat Pack	
	CY7C1370B-150BGI CY7C1372B-150BGI	BG119	119 BGA	
	CY7C1370B-150BZI CY7C1372B-150BZI	BA165A	165 FBGA	
133	CY7C1370B-133AI CY7C1372B-133AI	A101	100-lead Thin Quad Flat Pack	
	CY7C1370B-133BGI CY7C1372B-133BGI	BG119	119 PBGA	
	CY7C1370B-133BZI CY7C1372B-133BZI	BA165A	165 FBGA	

Shaded areas contain advance information.

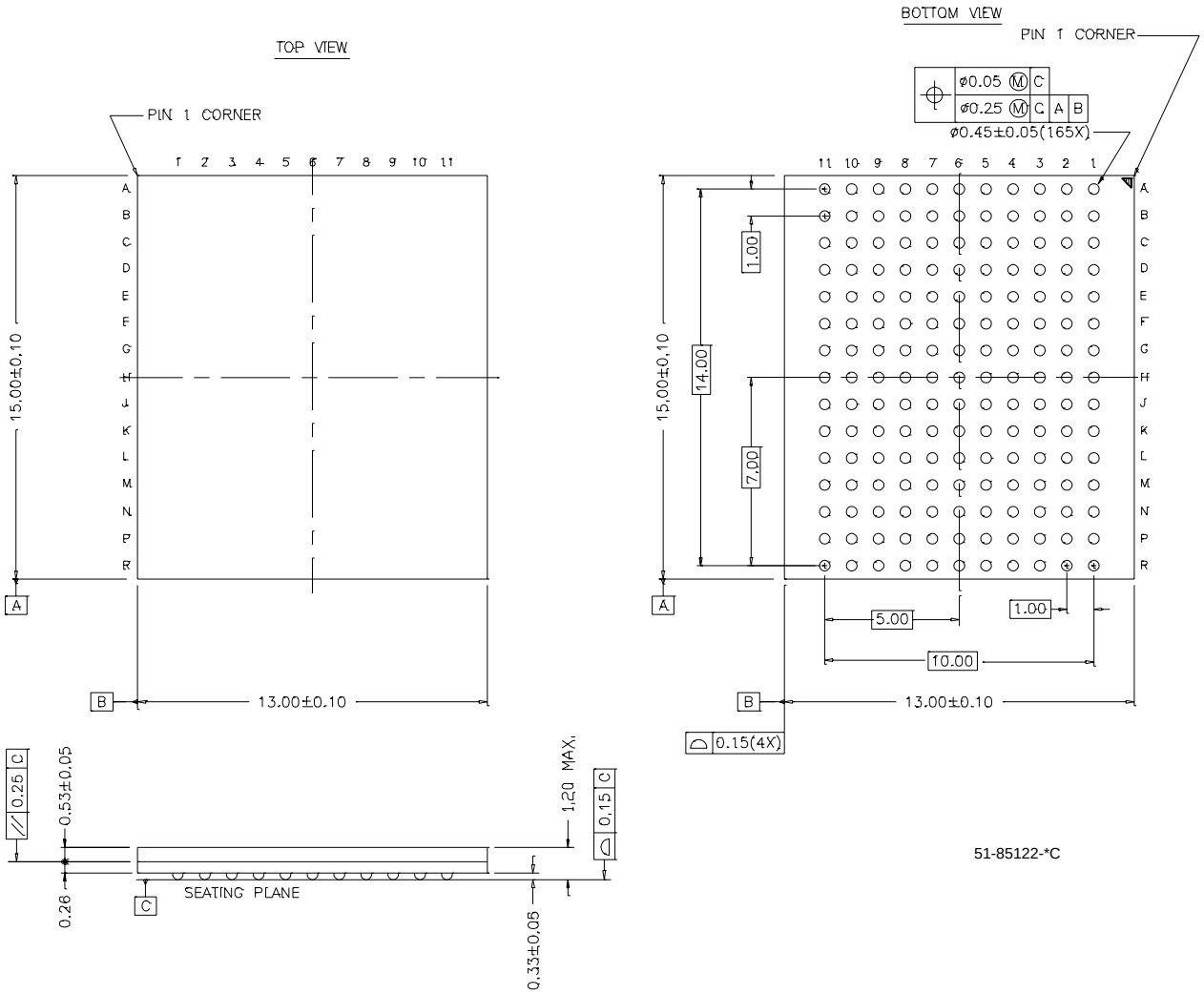
Package Diagrams

100-Pin Thin Plastic Quad Flatpack (14 x 20 x 1.4 mm) A101



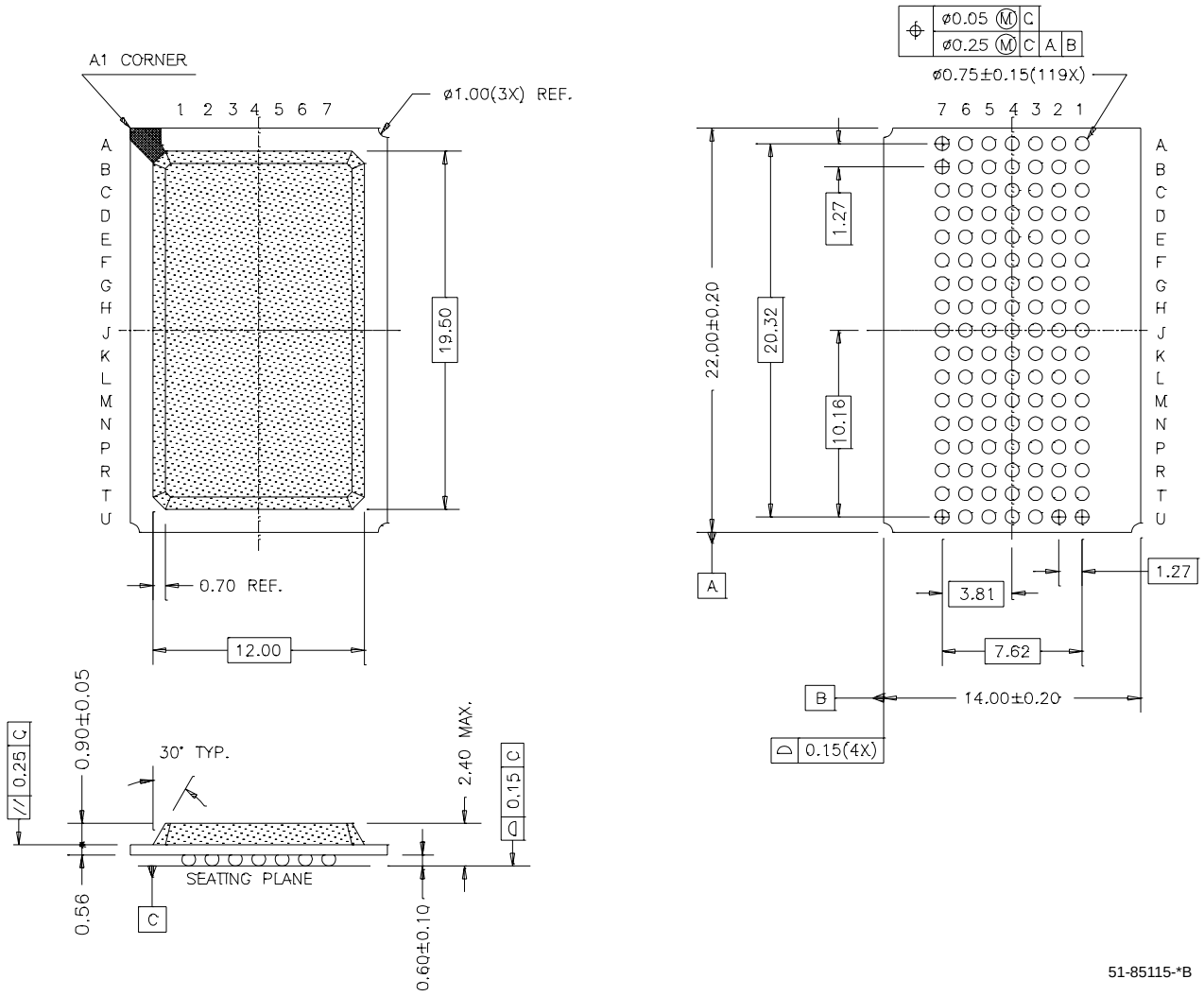
Package Diagrams (continued)

165-Ball FBGA (13 x 15 x 1.2 mm) BB165A



Package Diagrams (continued)

119-Lead PBGA (14 x 22 x 2.4 mm) BG119



Document History Page

Document Title: CY7C1370B/CY7C1372B 512K x 36/1M X 18 Pipelined SRAM with NoBL™ Architecture Document Number: 38-05197				
REV.	**ECN NO.**	**ISSUE DATE**	**ORIG. OF CHANGE**	**DESCRIPTION OF CHANGE**
**	112033	12/09/01	DSG	Change from Spec number: 38-01070 to 38-05197
*A	116852	08/19/02	CJM	Changed V_{DDQ} - Max = 3.63 to V_{DD} Added V_{IH} - Max = V_{DD}+0.5 Changed t_{DOH} from 1.5 to 1.3 ns
*B	121531	11/19/02	DSG	Updated package diagrams 51-85115 (BG119) to rev. *B and 51-85122 (BB165A) to rev. *C
*C	123127	01/18/03	RBI	Add power up requirments to operating range information