

## M27C64

### 64K (8K x 8) CHMOS Erasable PROM

The Intel M27C64 is a 5V only, 65,536-bit ultraviolet erasable and electrically programmable read-only memory (EPROM). The M27C64 employs advanced CHMOS II-E Circuitry for systems requiring low power, high performance speeds, and immunity to noise.

The M27C64 offers extremely low power consumption compared to typical 64K EPROMS. The maximum active current is 25 mA while the maximum standby current is only 140  $\mu$ A. The standby mode lowers power consumption without increasing access time.

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#### Rochester Electronics Manufactured Components

Rochester branded components are manufactured using either die/wafers purchased from the original suppliers or Rochester wafers recreated from the original IP. All recreations are done with the approval of the OCM.

Parts are tested using original factory test programs or Rochester developed test solutions to guarantee product meets or exceeds the OCM data sheet.

#### Quality Overview

- ISO-9001
- AS9120 certification
- Qualified Manufacturers List (QML) MIL-PRF-38535
  - Class Q Military
  - Class V Space Level
- Qualified Suppliers List of Distributors (QSLD)
  - Rochester is a critical supplier to DLA and meets all industry and DLA standards.

Rochester Electronics, LLC is committed to supplying products that satisfy customer expectations for quality and are equal to those originally supplied by industry manufacturers.

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*The original manufacturer's datasheet accompanying this document reflects the performance and specifications of the Rochester manufactured version of this device. Rochester Electronics guarantees the performance of its semiconductor products to the original OEM specifications. 'Typical' values are for reference purposes only. Certain minimum or maximum ratings may be based on product characterization, design, simulation, or sample testing.*



# M27C64

## 64K (8K x 8) CHMOS UV ERASABLE PROM

Military

- **Fast Access Times:**
  - M27C64-20 200 ns
  - M27C64-25 250 ns
  - M27C64-35 350 ns
- **CHMOS II-E\* Technology**
- **Extremely Low Power Consumption**
  - 25 mA Maximum Active
  - 140  $\mu$ A Maximum Standby
- **Two-Line Control**
- **Fast Programming**
  - intelligent Programming™ Algorithm
  - Quick-Pulse Programming™ Algorithm
- **Intelligent Identifier™ Mode**
  - Automated Programming Operations
- **Compatible With M2764A**
- **Maximum Latch-Up Immunity**
- **Military Temperature Range:**
  - 55°C to +125°C (T<sub>C</sub>)

The Intel M27C64 is a 5V only, 65,536-bit ultraviolet erasable and electrically programmable read-only memory (EPROM). The M27C64 employs advanced CHMOS II-E Circuitry for systems requiring low power, high performance speeds, and immunity to noise.

Several advanced features have been designed into the M27C64 that allow fast and reliable programming—Quick-Pulse Programming™, the intelligent Programming™ Algorithm and the intelligent Identifier™ Mode. Programming equipment that takes advantage of these innovations will electronically identify the M27C64 and then rapidly program it using an efficient programming method.

The M27C64 also offers extremely low power consumption compared to typical 64K EPROMS. The maximum active current is 25 mA while the maximum standby current is only 140  $\mu$ A. The standby mode lowers power consumption without increasing access time.

Two-line control and JEDEC-approved, 28-pin packaging are standard features of all Intel higher density EPROMs. This ensures easy microprocessor interfacing and minimum design efforts when upgrading, adding or choosing between non-volatile memory alternatives.

The highest degree of protection against latch-up is achieved through Intel's unique EPI processing. Prevention of latch-up is provided for stresses up to 100 mA on address and data pins from V<sub>CC</sub> -0.5V to V<sub>CC</sub> +0.5V.

\*HMOS and CHMOS are patented processes of Intel Corporation.

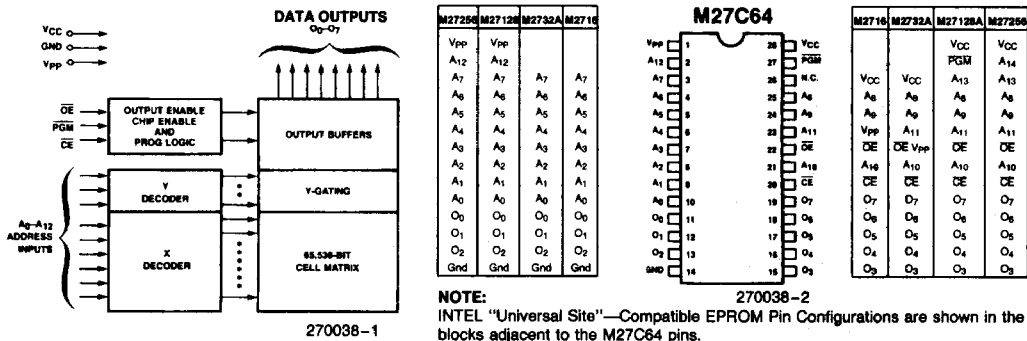
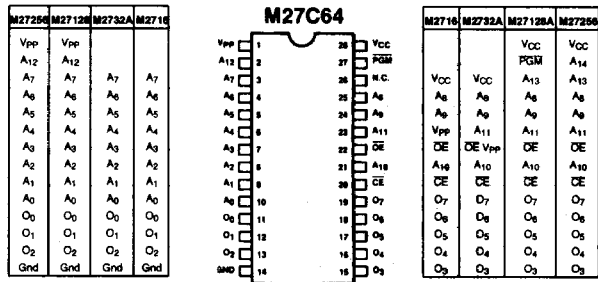


Figure 1. Block Diagram

Pin Names	
A <sub>0</sub> -A <sub>12</sub>	Addresses
CE	Chip Enable
OE	Output Enable
O <sub>0</sub> -O <sub>7</sub>	Outputs
PGM	Program
NC	No Connection



NOTE: INTEL "Universal Site"—Compatible EPROM Pin Configurations are shown in the blocks adjacent to the M27C64 pins.

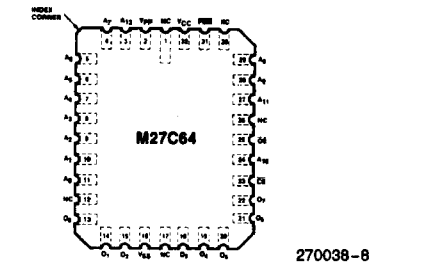


Figure 2. Pin Configurations

### ABSOLUTE MAXIMUM RATINGS\*

- Case Temperature Under Bias . . . -55°C to +125°C
- Storage Temperature . . . . . -65°C to +150°C(1)
- All Input or Output Voltages with  
Respect to Ground . . . . . +7.0V to -2.0V(1)
- Voltage on Pin 24 with  
Respect to Ground . . . . . +13.5V to -2.0V(1)
- V<sub>PP</sub> Supply Voltage with Respect to  
Ground During Programming . . +14V to -2.0V(1)

NOTICE: This is a production data sheet. The specifications are subject to change without notice.

\*WARNING: Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage. These are stress ratings only. Operation beyond the "Operating Conditions" is not recommended and extended exposure beyond the "Operating Conditions" may affect device reliability.

### Operating Conditions

Symbol	Parameter	Min	Max	Units
T <sub>C</sub>	Case Temperature (Instant On)	-55	+125	°C
V <sub>CC</sub>	Digital Supply Voltage	4.50	5.50	V

### READ OPERATION

#### D.C. CHARACTERISTICS (Over Specified Operating Conditions)

Symbol	Parameter	Notes	Min	Typ(2)	Max	Units	Comments
I <sub>LI</sub>	Input Load Current			0.01	1	μA	V <sub>IN</sub> = 5.5V
I <sub>LO</sub>	Output Leakage Current			0.01	1	μA	V <sub>OUT</sub> = 5.5V
I <sub>CC</sub> TTL	Operating Current TTL Inputs	3			25, 30	mA	$\overline{CE} = \overline{OE} = V_{IL}$ V <sub>PP</sub> = V <sub>CC</sub> , I <sub>0-7</sub> = 0 mA
I <sub>CC</sub> CMOS	Operating Current	3			10	mA	$\overline{CE} = \overline{OE} = V_{IL}$ V <sub>PP</sub> = V <sub>CC</sub> , I <sub>0-7</sub> = 0 mA
I <sub>SB</sub> TTL	Standby Current TTL Inputs	3			1	mA	$\overline{CE} = V_{IH}$
I <sub>SB</sub> CMOS	Standby Current CMOS Inputs	4			140	μA	$\overline{CE} = V_{IH}$
I <sub>PP</sub>	V <sub>PP</sub> Read Current	5			100	μA	V <sub>PP</sub> = V <sub>CC</sub>
V <sub>IL</sub>	Input Low Voltage ±10% Supply		-0.5		0.8	V	V <sub>PP</sub> = V <sub>CC</sub>
V <sub>IH</sub>	Input High Voltage ±10% Supply		2.0		V <sub>CC</sub> + 0.5		V <sub>PP</sub> = V <sub>CC</sub>
V <sub>OL</sub>	Output Low Voltage				0.45	V	I <sub>OL</sub> = 2.1 mA
V <sub>OH</sub>	Output High Voltage	2	3.5			V	I <sub>OH</sub> = -2.5 mA
I <sub>OS</sub>	Output Short Circuit Current	6			+100	mA	
V <sub>PP</sub>	V <sub>PP</sub> Read Voltage	7			V <sub>CC</sub>	V	

#### NOTES:

1. Minimum D.C. input voltage is -0.5V. During transition, the inputs may undershoot to -2.0V for periods less than 20 ns.
2. Typical limits are at V<sub>CC</sub> = 5V, T<sub>C</sub> = +25°C.
3. TTL inputs: spec V<sub>IL</sub>, V<sub>IH</sub> levels  
CMOS inputs: GND ±0.2 to V<sub>CC</sub> ±0.2  
25 mA for -35 version only.
4. CE is V<sub>CC</sub> ±0.2V. All other inputs can have any value within spec.
5. Maximum Active power usage is the sum I<sub>PP</sub> + I<sub>CC</sub>.
6. Output shorted for not more than one second. No more than one output shorted at a time.
7. V<sub>PP</sub> may be connected directly to V<sub>CC</sub> except during programming.

**A.C. CHARACTERISTICS(1)** (Over Specified Operating Conditions)

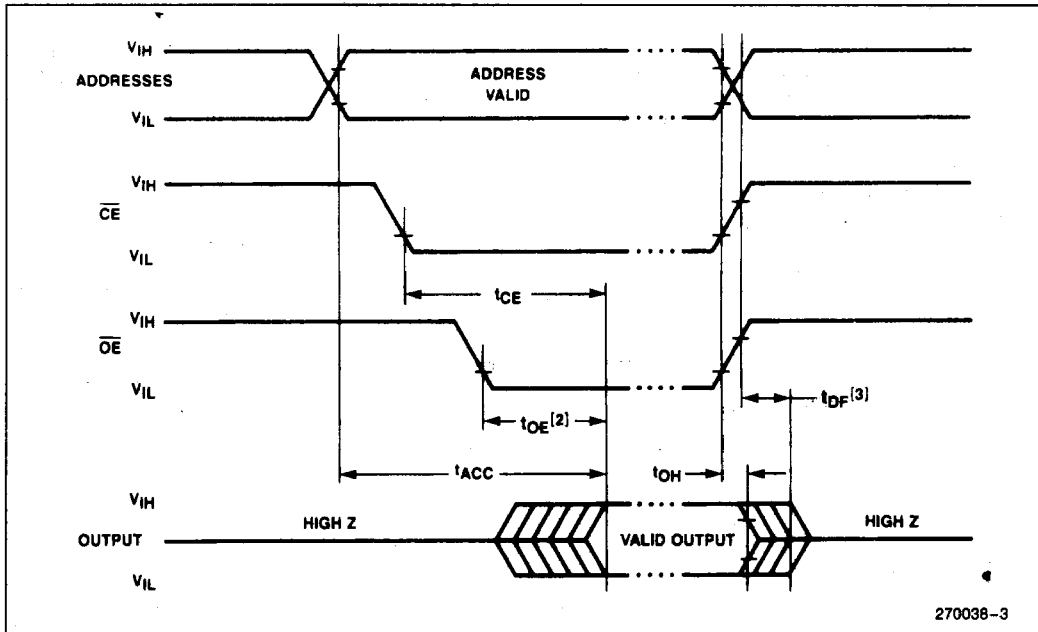
Symbol	Parameter	M27C64-20		M27C64-25		M27C64-35		Units	Comments
		Min	Max	Min	Max	Min	Max		
$t_{ACC}$	Address to Output Delay		200		250		350	ns	$\overline{CE} = \overline{OE} = V_{IL}$
$T_{CE}$	$\overline{CE}$ to Output Delay		200		250		350	ns	$\overline{OE} = V_{IL}$
$t_{OE}$	$\overline{OE}$ to Output Delay		75		100		120	ns	$\overline{CE} = V_{IL}$
$T_{DF}$	$\overline{OE}$ High to Output Float	0	55	0	55	0	105	ns	$\overline{CE} = V_{IL}$
$t_{OH}$	Output Hold from Addresses $\overline{CE}$ or $\overline{OE}$ Whichever Occurred First	0		0		0		ns	$\overline{CE} = \overline{OE} = V_{IL}$

**NOTES:**

1. A.C. Characteristics tested at  $V_{IH} = 2.4V$  and  $V_{IL} = 0.45V$ . Timing measurements made at  $V_{OL} = 0.8V$  and  $V_{OH} = 2.0V$ .

**CAPACITANCE**  $T_C = 25^\circ C, f = 1\text{ MHz}$ 

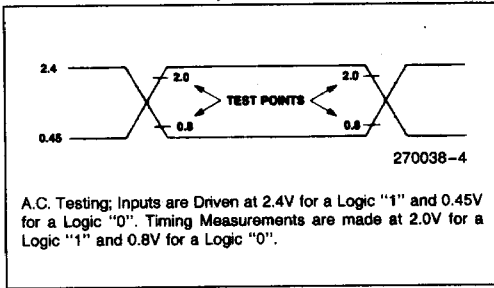
Symbol	Parameter	Typ (1)	Max	Units	Conditions
$C_{IN}$	Input Capacitance	4	6	pF	$V_{IN} = 0V$
$C_{OUT}$	Output Capacitance	8	12	pF	$V_{OUT} = 0V$

**A.C. WAVEFORMS**

**NOTES:**

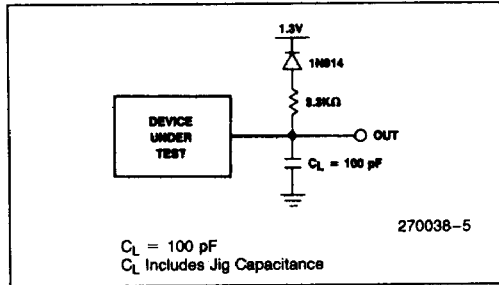
1. Typical values are for  $T_C = 25^\circ C$  and nominal supply voltages.
2.  $\overline{OE}$  may be delayed up to  $t_{ACC} - t_{OE}$  after the falling edge of  $\overline{CE}$  without impact on  $t_{ACC}$ .
3. Output Float is defined as the point where data is no longer driven.

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**A.C. TESTING INPUT, OUTPUT WAVEFORM**



**A.C. TESTING LOAD CIRCUIT**



**Table 1. Read Modes for M27C64**

Mode	Pins CE (20)	OE (22)	PGM (27)	$V_{pp}$ (1)	Outputs (11-13, 15-19)
Read	$V_{IL}$	$V_{IL}$	$V_{IH}$	$V_{CC}$	$D_{OUT}$
Output Disable	$V_{IL}$	$V_{IH}$	$V_{IH}$	$V_{CC}$	High Z
Standby	$V_{IH}$	X	X	$V_{CC}$	High Z

**NOTE:**  
 X can be  $V_{IH}$  or  $V_{IL}$

**READ MODE**

The M27C64 has two control functions, both of which must be logically active in order to obtain data at the outputs. Chip Enable ( $\overline{CE}$ ) is the power control and should be used for device selection. Output Enable ( $\overline{OE}$ ) is the output control and should be used to gate data from the output pins, independent of device selection. Assuming that addresses are stable, the address access time ( $t_{ACC}$ ) is equal to the delay from  $\overline{CE}$  to output ( $t_{CE}$ ). Data is available at the outputs after a delay of  $t_{OE}$  from the falling edge of  $\overline{OE}$ , assuming that  $\overline{CE}$  has been low and addresses have been stable for at least  $t_{ACC}-t_{OE}$ .

**STANDBY MODE**

THE M27C64 has a standby mode which reduces the maximum  $V_{CC}$  current to 140  $\mu\text{A}$ . The M27C64 is placed in the standby mode when pin 20,  $\overline{CE}$  in the TTL-high state. When in the standby mode, the outputs are in a high impedance state, independent of the  $\overline{OE}$  input.

**PROGRAMMING MODES**

*Caution: Exceeding 14.0V on pin 1 ( $V_{PP}$ ) may permanently damage the M27C64.*

**Table 2. Programming Modes for M27C64**

Mode	Pins CE (20)	OE (22)	PGM (27)	$A_9$ (24)	$A_0$ (10)	$V_{PP}$ (1)	$V_{CC}$ (28)	Outputs (11-13, 15-19)
Intelligent Programming	$V_{IL}$	$V_{IH}$	$V_{IL}$	X	X	$V_{PP}$	6.0V <sup>(4)</sup>	$D_{IN}$
Program Verify	$V_{IL}$	$V_{IL}$	$V_{IH}$	X	X	$V_{PP}$	6.0V <sup>(4)</sup>	$D_{OUT}$
Program Inhibit	$V_{IH}$	X	X	X	X	$V_{PP}$	$V_{CC}$	HIGH Z
Intelligent Identifier <sup>(3)</sup> — Manufacturer	$V_{IL}$	$V_{IL}$	$V_{IL}$	$V_H$	$V_{IL}$	$V_{CC}$	$V_{CC}$	89 H
Intelligent Identifier <sup>(3)</sup>	$V_{IL}$	$V_{IL}$	$V_{IH}$	$V_H$	$V_{IH}$	$V_{CC}$	$V_{CC}$	07 H

- NOTES:**
- X can be  $V_{IL}$  or  $V_{IH}$
  - $V_H = 12.0V \pm 0.5V$
  - $A_1-A_8, A_{10-12} = V_{IL}$
  - $V_{CC} = 6.0V \pm 0.25V$

Initially, and after each erasure, all bits of the M27C64 are in the "1" state. Data is introduced by selectively programming "0s" into the desired bit locations. Although only "0s" will be programmed both "1s" and "0s" can be present in the data word. The only way to change a "0" to a "1" is by ultraviolet light erasure.

The M27C64 is in the programming mode when the  $V_{PP}$  input is at 12.5V and  $\overline{CE}$  is at TTL-low. The data to be programmed is applied 8 bits in parallel to the data output pins. The levels required for the address and data inputs are TTL.

### intelligent Programming™ Algorithm

The M27C64 intelligent Programming Algorithm rapidly programs Intel CHMOS II-E EPROMs using an efficient and reliable method particularly suited to the production programming environment. Typical programming times for individual devices are on the order of one minute. Actual programming times may vary due to differences in programming equipment. Programming reliability is also ensured as the incremental program margin of each byte is continually monitored to determine when it has been successfully programmed. A flowchart of the M27C64 intelligent Programming Algorithm is shown in Figure 3.

The intelligent Programming Algorithm utilizes two different pulse types: initial and overprogram. The duration of the initial  $\overline{CE}$  pulse(s) is one millisecond, which will then be followed by a longer overprogram pulse of length  $3X$  msec.  $X$  is an iteration counter and is equal to the number of the initial one millisecond pulses applied to a particular M27C64 location, before a correct verify occurs. Up to 25 one-millisecond pulses per byte are provided for before the overprogram pulse is applied.

The entire sequence of program pulses and byte verifications is performed at  $V_{CC} = 6.0V$  and  $V_{PP} = 12.5V$ . When the intelligent programming cycle has been completed, all bytes should be compared to the original data with  $V_{CC} = 5.0V$ . The M27C64 can also be programmed using the Quick-Pulse Programming™ Algorithm.

### Program Inhibit

Programming of multiple M27C64 EPROMs in parallel with different data is easily accomplished by using the Program Inhibit mode. A high-level  $\overline{CE}$  input inhibits other M27C64 EPROMs from being programmed.

Except for  $\overline{CE}$  all inputs of the parallel M27C64s may be common. A TTL low-level pulse applied to the PGM input with  $V_{PP}$  at 12.5V will program the selected M27C64.

### Verify

A verify (read) should be performed on the programmed bits to determine that they have been correctly programmed. The verify is performed with  $\overline{OE}$  and  $\overline{CE}$  at  $V_{IL}$ . Data should be verified a minimum of  $t_{OEY}$  after the falling edge of  $\overline{OE}$ .

### intelligent Identifier™ Mode

The intelligent Identifier Mode allows the reading out of a binary code from an EPROM that will identify its manufacturer and type. This mode is intended for use by programming equipment for the purpose of automatically matching the device to be programmed with its corresponding programming algorithm. This mode is functional in the  $25^{\circ}C \pm 5^{\circ}C$  ambient temperature range that is required when programming the M27C64.

To activate this mode, the programming equipment must force 11.5V to 12.5V on address line A9 (pin 24) of the M27C64. Two bytes may then be sequenced from the device outputs by toggling address line A0 (pin 10) from  $V_{IL}$  to  $V_{IH}$ . All other address lines must be held at  $V_{IL}$  during intelligent Identifier Mode.

### ERASURE CHARACTERISTICS

The erasure characteristics of the M27C64 are such that erasure begins to occur upon exposure to light with wavelengths shorter than approximately 4000 Angstroms ( $\text{\AA}$ ). It should be noted that sunlight and certain types of fluorescent lamps have wavelengths in the 3000–4000  $\text{\AA}$  range. Data shows that constant exposure to room level fluorescent lighting could erase the typical M27C64 in approximately three years, while it would take approximately one week to cause erasure when exposed to direct sunlight. If the M27C64 is to be exposed to these types of lighting conditions for extended periods of time, opaque labels should be placed over the window to prevent unintentional erasure.

The recommended erasure procedure for the M27C64 is exposure to shortwave ultraviolet light which has a wavelength of 2537 Angstroms ( $\text{\AA}$ ). The integrated dose (i.e., UV intensity x exposure time) for erasure should be a minimum of fifteen (15)

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Wsec/cm<sup>2</sup>. The erasure time with this dosage is approximately 15 to 20 minutes using an ultraviolet lamp with a 12000  $\mu\text{W}/\text{cm}^2$  power rating. The M27C64 should be placed within one inch of the lamp tubes during erasure. The maximum integrated dose an M27C64 can be exposed to without damage is 7258 Wsec/cm<sup>2</sup> (1 week @ 12000  $\mu\text{W}/\text{cm}^2$ ). Exposure of these CHMOS EPROMs to high intensity UV light for longer periods may cause permanent damage.

### CHMOS NOISE CHARACTERISTICS

Special EPI processing techniques have enabled Intel to build CHMOS with features adding to system reliability. These include input/output protection to latch-up. Each of the data and address pins will not latch-up with currents up to 100 mA and voltages from -1V to V<sub>CC</sub> + 1V. Additionally, the V<sub>pp</sub> (programming) pin is designed to resist latch-up to the 14V maximum device limit.

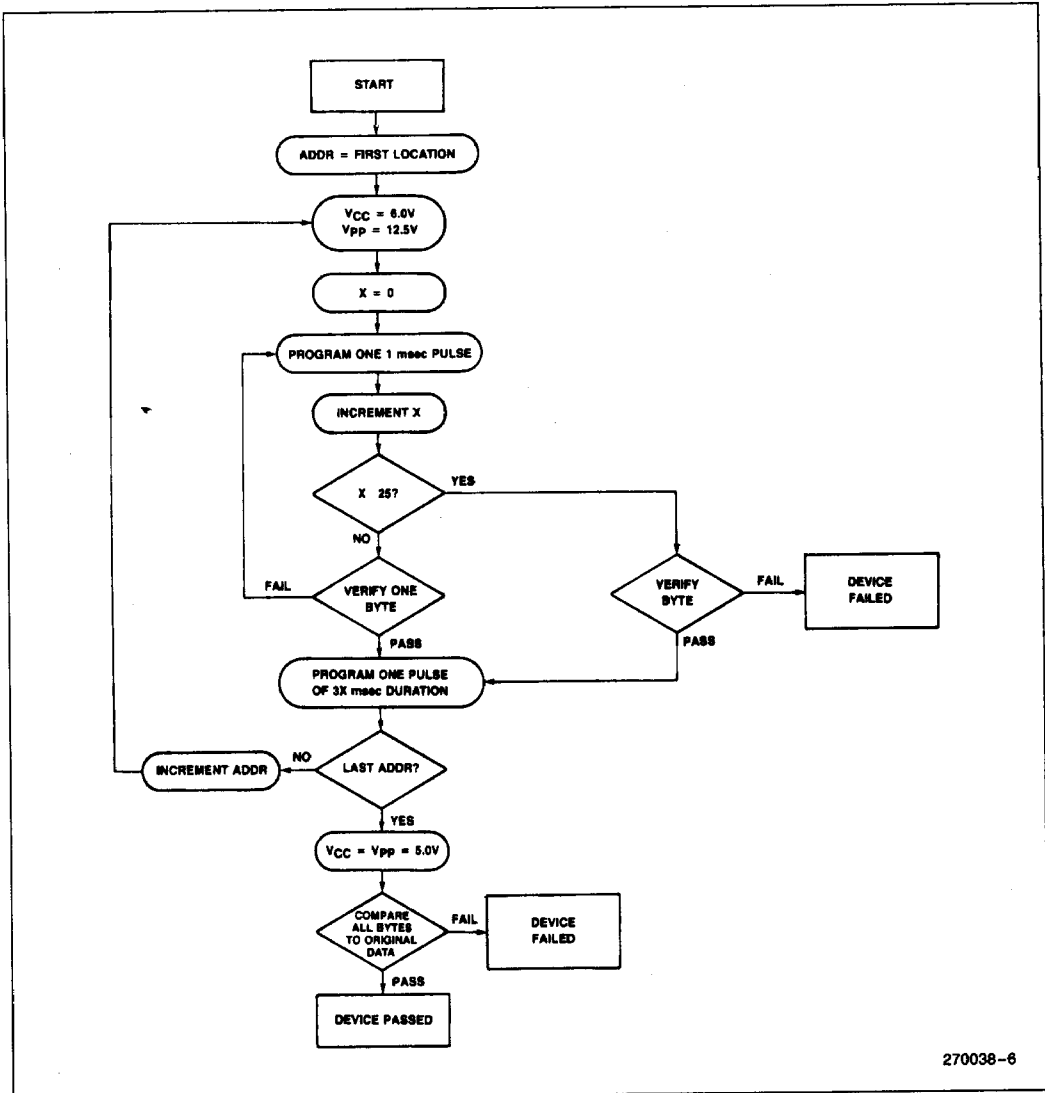


Figure 3. M27C64 intelligent Programming™ Flowchart

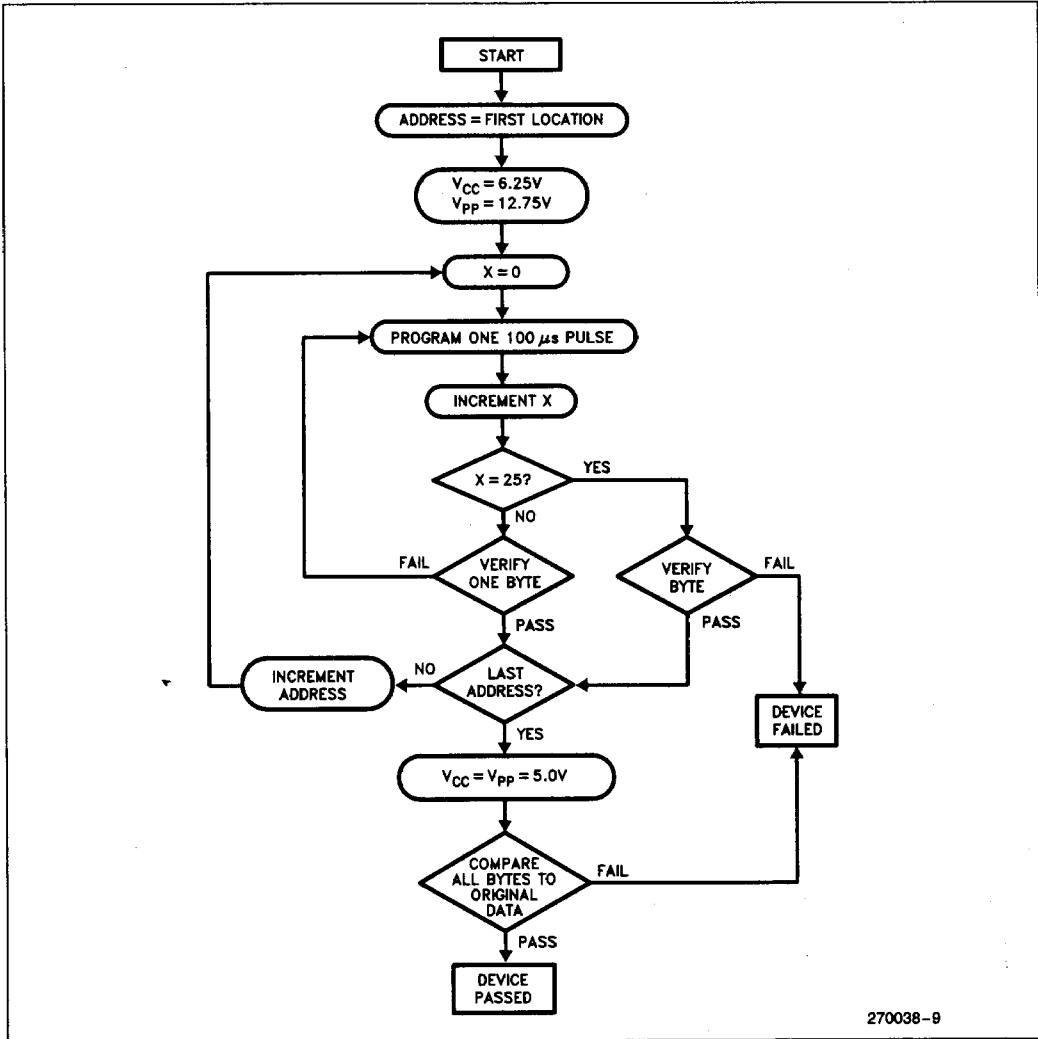


Figure 4. Quick-Pulse Programming™ Algorithm

**Quick-Pulse Programming™ Algorithm**

Intel's M27C64 EPROM is programmed using the Quick-Pulse Programming Algorithm, developed by Intel to substantially reduce the throughput time in the production programming environment.

The Quick-Pulse Programming Algorithm uses initial pulses of 100 μs followed by a byte verification to determine when the address byte has been successfully programmed. Up to 25 100 μs pulses

per byte are provided before a failure is recognized. A flow chart of the Quick-Pulse Programming Algorithm is shown in Figure 4.

For the Quick-Pulse Programming Algorithm, the entire sequence of programming pulses and byte verifications is performed at  $V_{CC} = 6.25V$  and  $V_{PP}$  at 12.75V (nominal). When programming of the EPROM has been completed, all bytes should be compared to the original data with  $V_{CC} = 5.0V$  ( $V_{PP} \leq V_{CC}$ ).



**D.C. PROGRAMMING CHARACTERISTICS**  $T_C = 25^\circ\text{C} \pm 5^\circ\text{C}$ 

Symbol	Parameter	Limits			Test Conditions (Note 1)
		Min	Max	Unit	
$I_{LI}$	Input Current (All Inputs)		1.0	$\mu\text{A}$	$V_{IN} = V_{IL}$ or $V_{IH}$
$V_{IL}$	Input Low Level (All Inputs)	-0.1	0.8	V	
$V_{IH}$	Input High Level	2.0	$V_{CC} + 0.5$	V	
$V_{OL}$	Output Low Voltage During Verify		0.45	V	$I_{OL} = 2.1 \text{ mA}$
$V_{OH}$	Output High Voltage During Verify	2.4		V	$I_{OH} = -400 \mu\text{A}$
$I_{CC2}^{(3)}$	$V_{CC}$ Supply Current		30	mA	
$I_{PP2}^{(3)}$	$V_{PP}$ Supply Current (Program)		30	mA	$\overline{CE} = V_{IL}$
$V_{ID}$	$A_9$ intelligent Identifier Voltage	11.5	12.5	V	
$V_{PP}$	intelligent Programming Algorithm	12.0	13.0	V	$\overline{CE} = \overline{PGM} = V_{IL}$
	Quick-Pulse Programming Algorithm	12.5	13.0	V	
$V_{CC}$	intelligent Programming Algorithm	5.75	6.25	V	
	Quick-Pulse Programming Algorithm	6.0	6.5	V	

**A.C. PROGRAMMING CHARACTERISTICS**
 $T_C = 25^\circ\text{C} \pm 5^\circ\text{C}$  (See Table 2 for  $V_{CC}$  and  $V_{PP}$  voltages.)

Symbol	Parameter	Limits				Conditions (Note 1)
		Min	Typ	Max	Unit	
$t_{AS}$	Address Setup Time	2			$\mu\text{s}$	
$t_{OES}$	$\overline{OE}$ Setup Time	2			$\mu\text{s}$	
$t_{DS}$	Data Setup Time	2			$\mu\text{s}$	
$t_{AH}$	Address Hold Time	0			$\mu\text{s}$	
$t_{DH}$	Data Hold Time	2			$\mu\text{s}$	
$t_{DFP}$	$\overline{OE}$ High to Output Float Delay	0		130	ns	(Note 2)
$t_{VPS}$	$V_{PP}$ Setup Time	2			$\mu\text{s}$	
$t_{VCS}$	$V_{CC}$ Setup Time	2			$\mu\text{s}$	
$t_{CES}$	$\overline{CE}$ Setup Time	2			$\mu\text{s}$	
$t_{PW}$	PGM Initial Program Pulse Width	0.95	1.0	1.05	ms	intelligent Programming Algorithm
		95	100	105	$\mu\text{s}$	Quick-Pulse Programming Algorithm
$t_{OPW}$	PGM Overprogram Pulse Width	2.85		78.75	ms	intelligent Programming Algorithm
$t_{OE}$	Data Valid from $\overline{OE}$			150	ns	

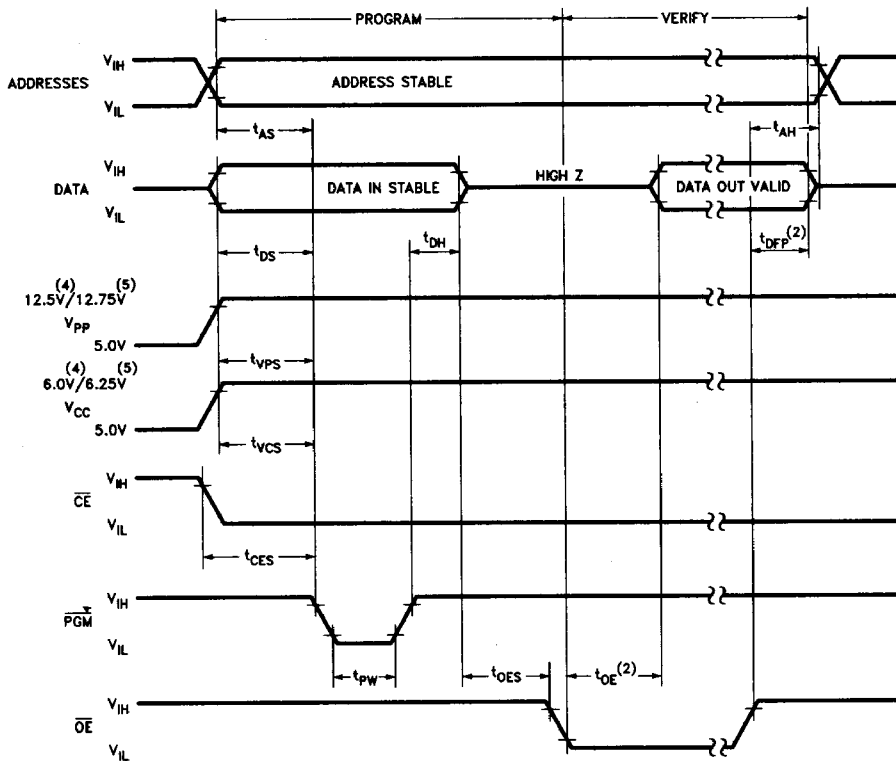
**A.C. CONDITIONS OF TEST**

Input Rise and Fall Times (10% to 90%) . . . . . 20 ns  
 Input Pulse Levels . . . . . 0.45V to 2.4V  
 Input Timing Reference Level . . . . . 0.8V and 2.0V  
 Output Timing Reference Level . . . . . 0.8V and 2.0V

**NOTES:**

- $V_{CC}$  must be applied simultaneously or before  $V_{PP}$  and removed simultaneously or after  $V_{PP}$ .
- This parameter is only sampled and is not 100% tested. Output Float is defined as the point where data is no longer driven—see timing diagram.
- The maximum current value is with outputs  $O_0$ – $O_7$  unloaded.

**PROGRAMMING WAVEFORMS** ( $V_{IL}$ ,  $V_{IH}$ )<sup>(1)</sup>



270038-10

**NOTES:**

1. The Input Timing Reference Level is 0.8V for  $V_{IL}$  and 2V for a  $V_{IH}$ .
2.  $t_{OE}$  and  $t_{DFP}$  are characteristics of the device but must be accommodated by the programmer.
3. When programming the M27C128, a 0.1  $\mu$ F capacitor is required across  $V_{PP}$  and ground to suppress spurious voltage transients which can damage the device.
4. intelligent Programming Algorithm Voltage Levels.
5. Quick-Pulse Programming Algorithm Voltage Levels.