DATA SHEET

For a complete data sheet, please also download:

- The IC06 74HC/HCT/HCU/HCMOS Logic Family Specifications
- The IC06 74HC/HCT/HCU/HCMOS Logic Package Information
- The IC06 74HC/HCT/HCU/HCMOS Logic Package Outlines

74HC/HCT173

Quad D-type flip-flop; positive-edge trigger; 3-state

Product specification
File under Integrated Circuits, IC06

December 1990

Philips Semiconductors

PHILIPS

Quad D-type flip-flop; positive-edge trigger; 3-state 74HC/HCT173

FEATURES

- Gated input enable for hold (do nothing) mode
- Gated output enable control
- Edge-triggered D-type register
- Asynchronous master reset
- Output capability: bus driver
- I_{CC} category: MSI

GENERAL DESCRIPTION

The 74HC/HCT173 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT173 are 4-bit parallel load registers with clock enable control, 3-state buffered outputs (Q_0 to Q_3) and master reset (MR).

When the two data enable inputs ($\overline{E}_1$ and $\overline{E}_2$) are LOW, the data on the D_n inputs is loaded into the register synchronously with the LOW-to-HIGH clock (CP) transition. When one or both $\overline{E}_n$ inputs are HIGH one set-up time prior to the LOW-to-HIGH clock transition, the register will retain the previous data. Data inputs and clock enable inputs are fully edge-triggered and must be stable only one set-up time prior to the LOW-to-HIGH clock transition.

The master reset input (MR) is an active HIGH asynchronous input. When MR is HIGH, all four flip-flops are reset (cleared) independently of any other input condition.

The 3-state output buffers are controlled by a 2-input NOR gate. When both output enable inputs ($\overline{OE}_1$ and $\overline{OE}_2$) are LOW, the data in the register is presented to the Q_n outputs. When one or both $\overline{OE}_n$ inputs are HIGH, the outputs are forced to a high impedance OFF-state. The 3-state output buffers are completely independent of the register operation; the $\overline{OE}_n$ transition does not affect the clock and reset operations.

QUICK REFERENCE DATA

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f$ = 6 ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t_{PHL}/ t_{PLH}	propagation delay CP to Q_n MR to Q_n	C_L = 15 pF; V_{CC} = 5 V	 17 13	 17 17	 ns ns
f_{max}	maximum clock frequency		88	88	MHz
C_I	input capacitance		3.5	3.5	pF
C_{PD}	power dissipation capacitance per flip-flop	notes 1 and 2	20	20	pF

Notes

1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz
   f_o = output frequency in MHz
   $\sum (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs
   C_L = output load capacitance in pF
   V_{CC} = supply voltage in V
2. For HC the condition is V_I = GND to V_{CC}
   For HCT the condition is V_I = GND to V_{CC} –1.5 V

ORDERING INFORMATION

See *"74HC/HCT/HCU/HCMOS Logic Package Information"*.

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1, 2	$\overline{OE}_1$, $\overline{OE}_2$	output enable input (active LOW)
3, 4, 5, 6	Q_0 to Q_3	3-state flip-flop outputs
7	CP	clock input (LOW-to-HIGH, edge-triggered)
8	GND	ground (0 V)
9, 10	$\overline{E}_1$, $\overline{E}_2$	data enable inputs (active LOW)
14, 13, 12, 11	D_0 to D_3	data inputs
15	MR	asynchronous master reset (active HIGH)
16	V_{CC}	positive supply voltage

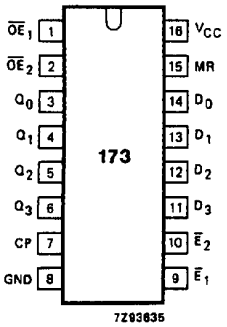


Fig.1 Pin configuration.

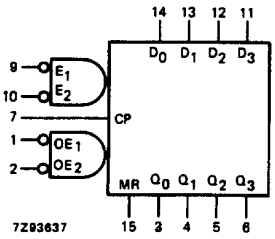


Fig.2 Logic symbol.

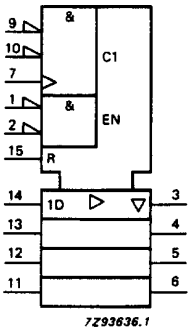


Fig.3 IEC logic symbol.

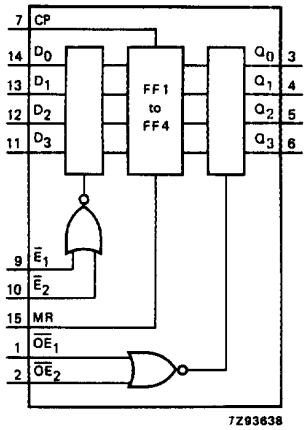


Fig.4 Functional diagram.

FUNCTION TABLE

REGISTER OPERATING MODES	INPUTS					OUTPUTS
	MR	CP	$\overline{E}_1$	$\overline{E}_2$	D_n	Q_n (register)
reset (clear)	H	X	X	X	X	L
parallel load	L L	↑ ↑	l l	l l	l h	L H
hold (no change)	L L	X X	h X	X h	X X	q_n q_n

3-STATE BUFFER OPERATING MODES	INPUTS			OUTPUTS			
	Q_n (register)	$\overline{OE}_1$	$\overline{OE}_2$	Q_0	Q_1	Q_2	Q_3
read	L H	L L	L L	L H	L H	L H	L H
disabled	X X	H X	X H	Z Z	Z Z	Z Z	Z Z

Notes

1. H = HIGH voltage level
   h = HIGH voltage level one set-up time prior to the LOW-to-HIGH CP transition
   L = LOW voltage level
   l = LOW voltage level one set-up time prior to the LOW-to-HIGH CP transition
   q = lower case letters indicate the state of the referenced input (or output) one set-up time prior to the LOW-to-HIGH CP transition
   X = don't care
   Z = high impedance OFF-state
   ↑ = LOW-to-HIGH CP transition

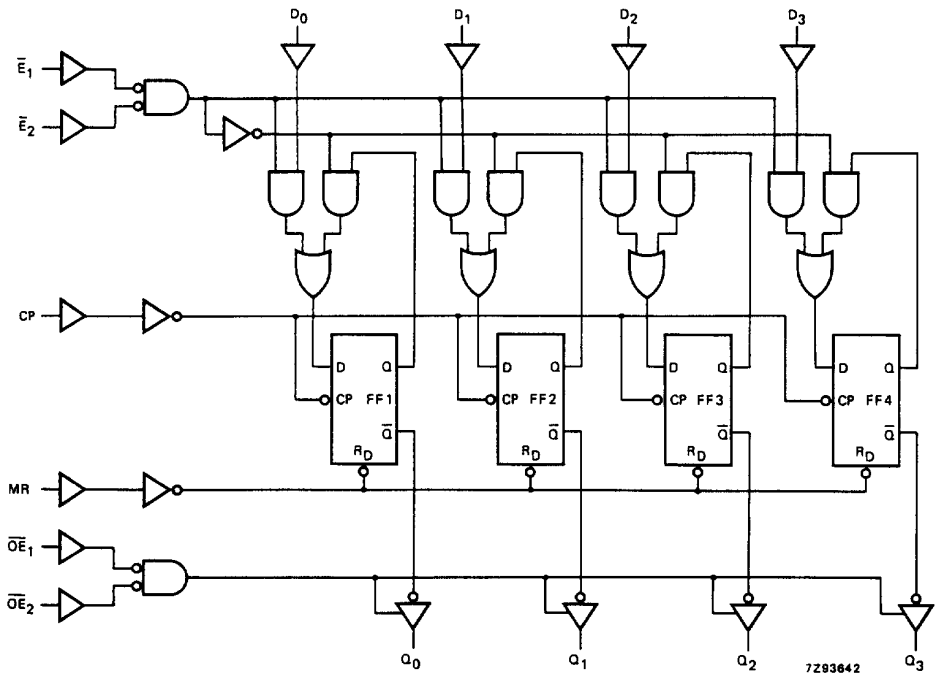


Fig.5 Logic diagram.

DC CHARACTERISTICS FOR 74HC

For the DC characteristics see *"74HC/HCT/HCU/HCMOS Logic Family Specifications"*.

Output capability: bus driver
I_{CC} category: MSI

AC CHARACTERISTICS FOR 74HC

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HC								V_{CC} (V)	WAVEFORMS
		+25			–40 to +85		–40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/ t_{PLH}	propagation delay CP to Q_n		55 20 16	175 35 30		220 44 37		265 53 45	ns	2.0 4.5 6.0	Fig.6
t_{PHL}	propagation delay MR to Q_n		44 16 13	150 30 26		190 38 33		225 45 38	ns	2.0 4.5 6.0	Fig.7
t_{PZH}/ t_{PZL}	3-state output enable time $\overline{OE}_n$ to Q_n		52 19 15	150 30 26		190 38 33		225 45 38	ns	2.0 4.5 6.0	Fig.8
t_{PHZ}/ t_{PLZ}	3-state output disable time $\overline{OE}_n$ to Q_n		52 19 15	150 30 26		190 38 33		225 45 38	ns	2.0 4.5 6.0	Fig.8
t_{THL}/ t_{TLH}	output transition time		14 5 4	60 12 10		75 15 13		90 18 15	ns	2.0 4.5 6.0	Fig.6
t_W	clock pulse width HIGH or LOW	80 16 14	14 5 4		100 20 17		120 24 20		ns	2.0 4.5 6.0	Fig.6
t_W	master reset pulse width; HIGH	80 16 14	14 5 4		100 20 17		120 24 20		ns	2.0 4.5 6.0	Fig.7
t_{rem}	removal time MR to CP	60 12 10	–8 –3 –2		75 15 13		90 18 15		ns	2.0 4.5 6.0	Fig.7
t_{su}	set-up time $\overline{E}_n$ to CP	100 20 17	33 12 10		125 25 21		150 30 26		ns	2.0 4.5 6.0	Fig.9
t_{su}	set-up time D_n to CP	60 12 10	17 6 5		75 15 13		90 18 15		ns	2.0 4.5 6.0	Fig.9

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HC								V_{CC} (V)	WAVEFORMS
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_h	hold time $\overline{E}_n$ to CP	0 0 0	−17 −6 −5		0 0 0		0 0 0		ns	2.0 4.5 6.0	Fig.9
t_h	hold time D_n to CP	1 1 1	−11 −4 −3		1 1 1		1 1 1		ns	2.0 4.5 6.0	Fig.9
f_{max}	maximum clock pulse frequency	6.0 30 35	26 80 95		4.8 24 28		4.0 20 24		MHz	2.0 4.5 6.0	Fig.6

DC CHARACTERISTICS FOR 74HCT

For the DC characteristics see *"74HC/HCT/HCU/HCMOS Logic Family Specifications"*.

Output capability: bus driver
I_{CC} category: MSI

Note to HCT types

The value of additional quiescent supply current (ΔI_{CC}) for a unit load of 1 is given in the family specifications. To determine ΔI_{CC} per input, multiply this value by the unit load coefficient shown in the table below.

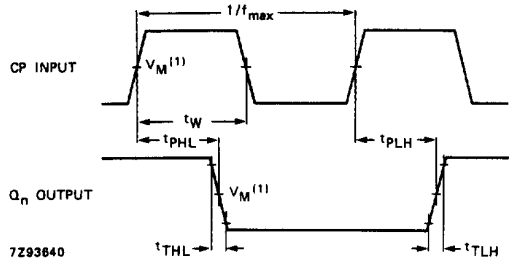
INPUT	UNIT LOAD COEFFICIENT
$\overline{OE}_1$, $\overline{OE}_2$	0.50
MR	0.60
$\overline{E}_1$, $\overline{E}_2$	0.40
D_n	0.25
CP	1.00

AC CHARACTERISTICS FOR 74HCT

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

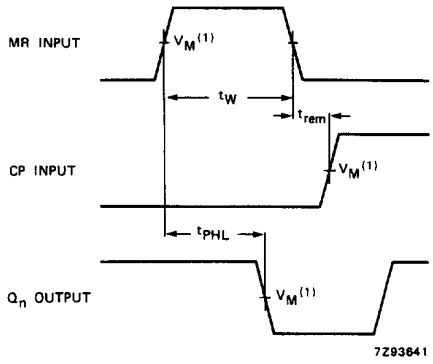
SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HCT								V_{CC} (V)	WAVEFORMS
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/ t_{PLH}	propagation delay CP to Q_n		20	40		50		60	ns	4.5	Fig.6
t_{PHL}	propagation delay MR to Q_n		20	37		46		56	ns	4.5	Fig.7
t_{PZH}/ t_{PZL}	3-state output enable time $\overline{OE}_n$ to Q_n		20	35		44		53	ns	4.5	Fig.8
t_{PHZ}/ t_{PLZ}	3-state output disable time $\overline{OE}_n$ to Q_n		19	30		38		45	ns	4.5	Fig.8
t_{THL}/ t_{TLH}	output transition time		5	12		15		19	ns	4.5	Fig.6
t_W	clock pulse width HIGH or LOW	16	7		20		24		ns	4.5	Fig.6
t_W	master reset pulse width; HIGH	15	6		19		22		ns	4.5	Fig.7
t_{rem}	removal time MR to CP	12	−2		15		18		ns	4.5	Fig.7
t_{su}	set-up time $\overline{E}_n$ to CP	22	13		28		33		ns	4.5	Fig.9
t_{su}	set-up time D_n to CP	12	7		15		18		ns	4.5	Fig.9
t_h	hold time $\overline{E}_n$ to CP	0	−6		0		0		ns	4.5	Fig.9
t_h	hold time D_n to CP	0	−3		0		0		ns	4.5	Fig.9
f_{max}	maximum clock pulse frequency	30	80		24		20		MHz	4.5	Fig.6

AC WAVEFORMS



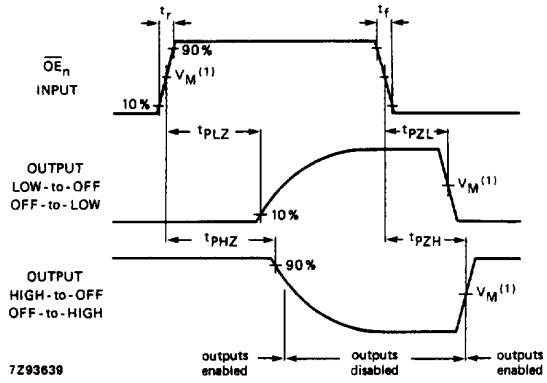
(1) HC : V_M = 50%; V_I = GND to V_{CC}.
HCT: V_M = 1.3 V; V_I = GND to 3 V.

Fig.6 Waveforms showing the clock (CP) to output (Q_n) propagation delays, the clock pulse width, the output transition times and the maximum clock pulse frequency.



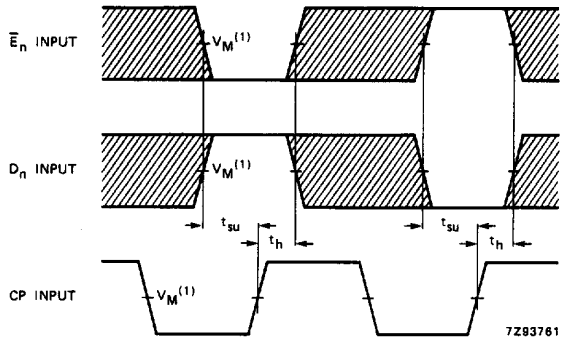
(1) HC : V_M = 50%; V_I = GND to V_{CC}.
HCT: V_M = 1.3 V; V_I = GND to 3 V.

Fig.7 Waveforms showing the master reset (MR) pulse width, the master reset to output (Q_n) propagation delays and the master reset to clock (CP) removal time.



(1) HC : V_M = 50%; V_I = GND to V_{CC}.
HCT: V_M = 1.3 V; V_I = GND to 3 V.

Fig.8 Waveforms showing the 3-state enable and disable times.



The shaded areas indicate when the input is permitted to change for predictable output performance.

(1) HC : V_M = 50%; V_I = GND to V_{CC}.
HCT: V_M = 1.3 V; V_I = GND to 3 V.

Fig.9 Waveforms showing the data set-up and hold times from input ($\overline{E}n$, D_n) to clock (CP).

PACKAGE OUTLINES

See *"74HC/HCT/HCU/HCMOS Logic Package Outlines"*.

74HC/HCT173; Quad D-type flip-flop; positive-edge trigger; 3-state

Information as of 2003-04-22

- Products
- MultiMarket Semiconductors
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- Catalog by Function
- Catalog by System
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General description

The 74HC/HCT173 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT173 are 4-bit parallel load registers with clock enable control, 3-state buffered outputs (Q_0 to Q_3) and master reset (MR).

When the two data enable inputs (E_1 and E_2) are LOW, the data on the Dn inputs is loaded into the register synchronously with the LOW-to-HIGH clock (CP) transition. When one or both E_n inputs are HIGH one set-up time prior to the LOW-to-HIGH clock transition, the register will retain the previous data. Data inputs and clock enable inputs are fully edge-triggered and must be stable only one set-up time prior to the LOW-to-HIGH clock transition.

The master reset input (MR) is an active HIGH asynchronous input. When MR is HIGH, all four flip-flops are reset (cleared) independently of any other input condition.

The 3-state output buffers are controlled by a 2-input NOR gate. When both output enable inputs (OE_1 and OE_2) are LOW, the data in the register is presented to the Q_n outputs. When one or both OE_n inputs are HIGH, the outputs are forced to a high impedance OFF-state. The 3-state output buffers are completely independent of the register operation; the OE_n transition does not affect the clock and reset operations.

Features

- Gated input enable for hold (do nothing) mode
- Gated output enable control
- Edge-triggered D-type register
- Asynchronous master reset
- Output capability: bus driver
- I_{CC} category: MSI

Datasheet

Type number	Title	Publication release date	Datasheet status	Page count	File size (kB)	Datasheet
74HC/HCT173	Quad D-type flip-flop; positive-edge trigger; 3-state	12/1/1990	Product specification	10	65	Download

Additional datasheet info

To complete the device datasheet with package and family information, also download the following PDF files. The "Logic Package Information" document is required to determine in which package(s) this device is available.

	Document	Description
1	HCT_FAMILY_SPECIFICATIONS	HC/T Family Specifications, The IC06 74HC/HCT/HCMOS Logic Family Specifications
2	HCT_PACKAGE_INFO	HC/T Package Info, The IC06 74HC/HCT/HCMOS Logic Package Information
3	HCT_PACKAGE_OUTLINES	HC/T Package Outlines, The IC06 74HC/HCT/HCMOS Logic Package Outlines

Parametrics

Type number	Package	Description	Propagation Delay(ns)	Voltage	No. of Pins	Power Dissipation Considerations	Logic Switching Levels	Output Drive Capability
74HC173D	SOT109 (SO16)	Quad D-Type Flip-Flop; Postive-Edge Trigger; 3-State	15	5 Volts +	16	Low Power or Battery Applications	CMOS	Low
74HC173DB	SOT338-1 (SSOP16)	Quad D-Type Flip-Flop; Postive-Edge Trigger; 3-State	15	5 Volts +	16	Low Power or Battery Applications	CMOS	Low
74HC173N	SOT38-1 (DIP16)	Quad D-Type Flip-Flop; Postive-Edge Trigger; 3-State	15	5 Volts +	16	Low Power or Battery Applications	CMOS	Low

74HC173PW	SOT403-1 (TSSOP16)	Quad D-Type Flip-Flop; Postive-Edge Trigger; 3-State	15	5 Volts +	16	Low Power or Battery Applications	CMOS	Low
74HCT173D	SOT109 (SO16)	Quad D-Type Flip-Flop; Postive-Edge Trigger; TTL Enabled (3-State)	15	5 Volts +	16	Low Power or Battery Applications	TTL	Low
74HCT173DB	SOT338-1 (SSOP16)	Quad D-Type Flip-Flop; Postive-Edge Trigger; TTL Enabled (3-State)	15	5 Volts +	16	Low Power or Battery Applications	TTL	Low
74HCT173N	SOT38-1 (DIP16)	Quad D-Type Flip-Flop; Postive-Edge Trigger; TTL Enabled (3-State)	15	5 Volts +	16	Low Power or Battery Applications	TTL	Low

Products, packages, availability and ordering

Type number	North American type number	Ordering code (12NC)	Marking/Packing Discretes packing info	Package	Device status	Buy online
74HC173D	74HC173D	9337 145 60652	Standard Marking * Bulk Pack, CECC	SOT109 (SO16)	Full production	order this -
	74HC173D-T	9337 145 60653	Standard Marking * Reel Pack, SMD, 13", CECC	SOT109 (SO16)	Full production	order this -
74HC173DB	74HC173DB	9351 892 50112	Standard Marking * Bulk Pack	SOT338-1 (SSOP16)	Full production	order this -
	74HC173DB-T	9351 892 50118	Standard Marking * Reel Pack, SMD, 13"	SOT338-1 (SSOP16)	Full production	order this -
74HC173N	74HC173N	9336 694 20652	Standard Marking * Bulk Pack, CECC	SOT38-1 (DIP16)	Full production	order this -

74HC173PW	74HC173PW	9351 895 50112	Standard Marking * Bulk Pack	SOT403-1 (TSSOP16)	Full production	order this
	74HC173PW-T	9351 895 50118	Standard Marking * Reel Pack, SMD, 13"	SOT403-1 (TSSOP16)	Full production	order this
74HCT173D	74HCT173D	9337 150 40652	Standard Marking * Bulk Pack, CECC	SOT109 (SO16)	Full production	order this
	74HCT173D-T	9337 150 40653	Standard Marking * Reel Pack, SMD, 13", CECC	SOT109 (SO16)	Full production	order this
74HCT173DB	74HCT173DB	9351 897 10112	Standard Marking * Bulk Pack	SOT338-1 (SSOP16)	Full production	order this
	74HCT173DB-T	9351 897 10118	Standard Marking * Reel Pack, SMD, 13"	SOT338-1 (SSOP16)	Full production	order this
74HCT173N	74HCT173N	9336 700 50652	Standard Marking * Bulk Pack, CECC	SOT38-1 (DIP16)	Full production	order this

Products in the above table are all in production. Some variants are discontinued; click here for information on these variants.

Similar products

74HC/HCT173 links to the similar products page containing an overview of products that are similar in function or related to the type number(s) as listed on this page. The similar products page includes products from the same catalog tree(s), relevant selection guides and products from the same functional category.

Support & tools

HC/T Family Specifications, The IC06 74HC/HCT/HCMOS Logic Family Specifications(date 01-Mar-98)
HC/T User Guide(date 01-Nov-97)

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  French Translate

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