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82750LV
Technical Specifications

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82750LV Technical Specifications

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82750LV VRAM, SCSI AND CAPTURE GATE ARRAY (VSCGA)

Introduction

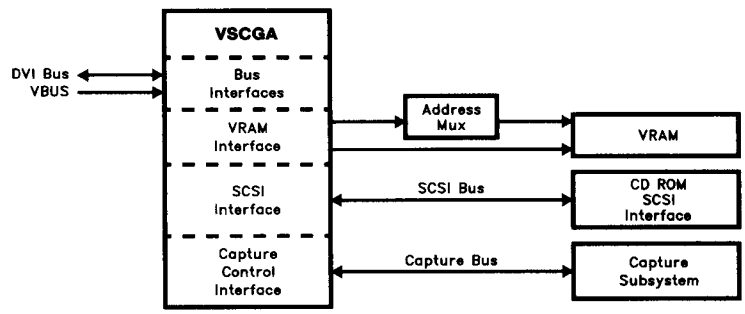
The VRAM, SCSI and Capture Gate Array (VSCGA) serves five functions: (1) It provides all of the signals necessary to operate the VRAM; (2) It interfaces the DVI Bus to the SCSI Bus, allowing control of a CD-ROM and other SCSI Device; (3) It interfaces the DVI Bus to the Video Capture Bus allowing command and status information to be exchanged between the two busses and digitized video to be directly loaded into VRAM through the parallel port; (4) It prioritizes CD-ROM and video capture DMA requests and implements the DVI protocols to execute those requests; (5) It converts the time-multiplexed addresses on the DVI Data Bus to a separate Address Bus for use by the other DVI Bus components.

The following figure shows a simplified block diagram of the VSCGA gate array interconnections in a typical DVI system. The DVI Bus and the VBUS contain address, data and/or control signals required by the array to perform its functions.

The VRAM Interface provides all the control signals for randomly accessing the memory including the Address Mux signals used to generate row and column addresses. Additionally, the operation of the serial output memory port to the Intel 82750 DVI Display Processor (DB) and the transfer of data between the parallel and serial memory ports are the responsibility of the gate array.

The VSCGA chip implements a SCSI Interface with the capability of operating multiple devices. Preparatory operations are handled under software control but the main task of transferring data is automated by a state machine contained within the array.

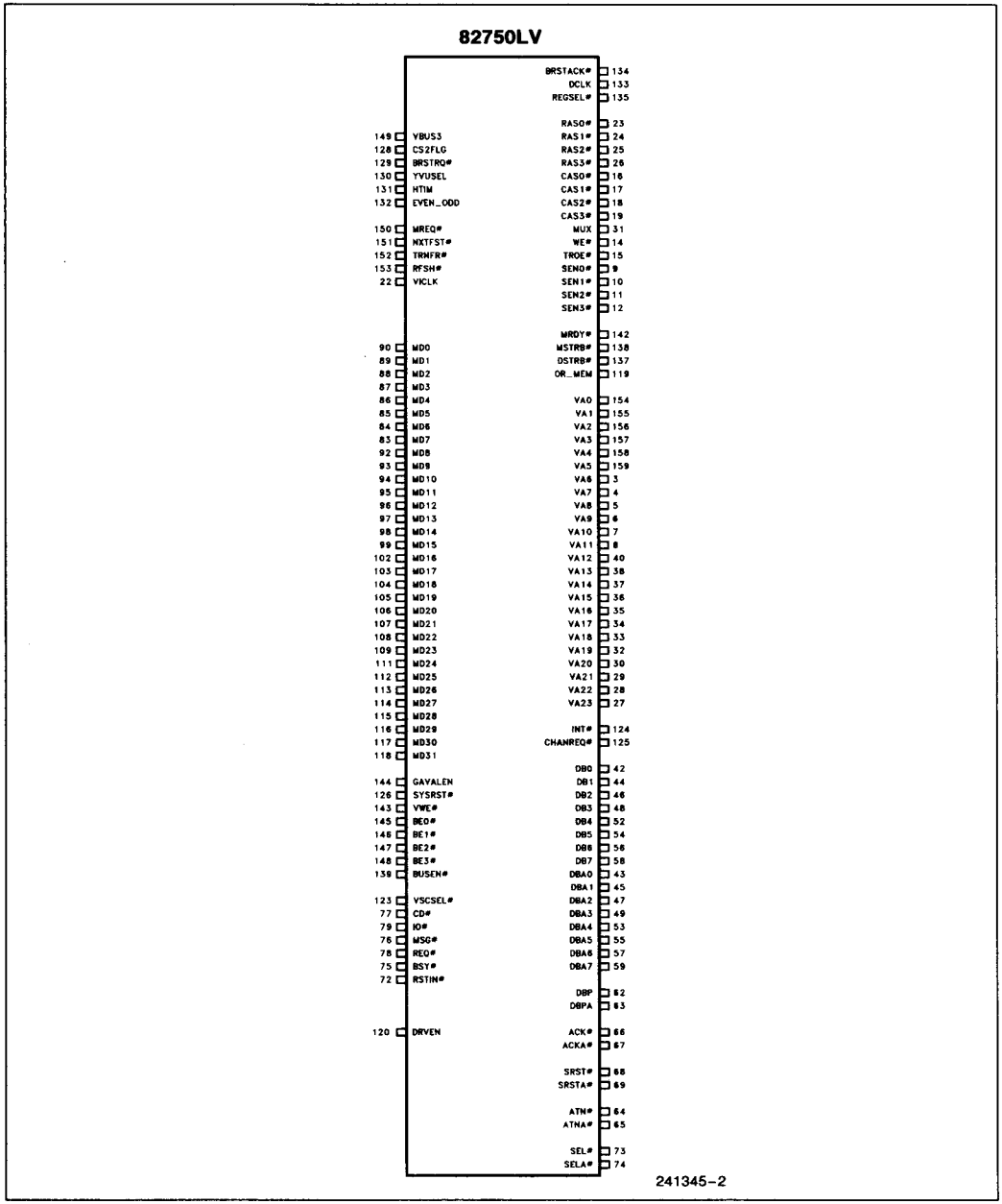
The Video Capture Bus uses the parallel data port of the VRAM to introduce video data into the DVI system. This is a departure from earlier systems which used the serial port for this function and was done to isolate the capture video from the DB display video, which also requires the serial VRAM data.



NOTE:
Manufactured and tested for Intel by Texas Instruments in accordance with Texas Instruments internal standards.

1.0 PIN DESCRIPTION

1.1 Pinout



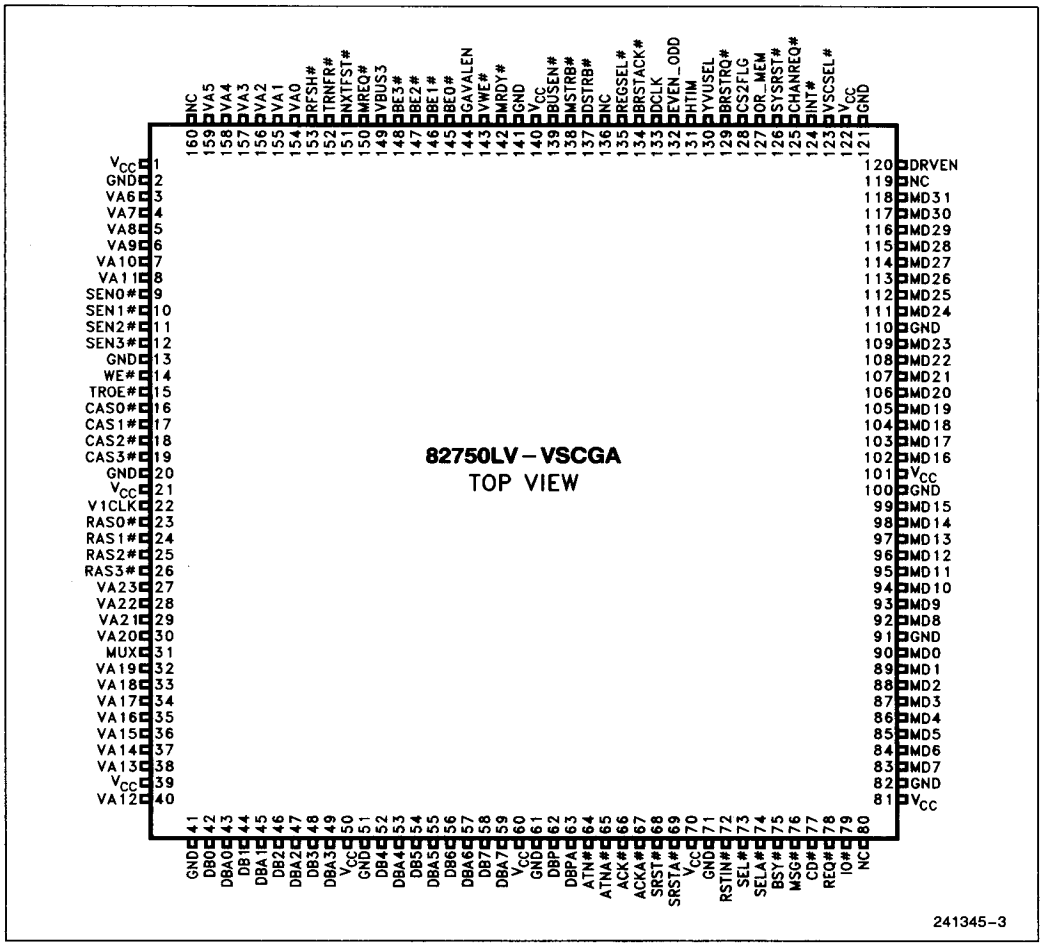


Figure 1-1. 82750LV Pinout

Table 1-1. Pin Cross Reference by Pin Name

Pin Name	Location
ACK#	66
ACKA#	67
ATN#	64
ATNA#	65
BE0#	145
BE1#	146
BE2#	147
BE3#	148
BRSTACK#	134
BRSTRQ#	129
BSY#	75
BUSEN#	139
CAS0#	16
CAS1#	17
CAS2#	18
CAS3#	19
CD#	77
CHANREQ#	125
CS2FLG	128
DB0	42
DB1	44
DB2	46
DB3	48
DB4	52
DB5	54
DB6	56
DB7	58
DBA0	43
DBA1	45
DBA2	47
DBA3	49
DBA4	53
DBA5	55
DBA6	57
DBA7	59
DBP	62
DBPA	63
DCLK	133
DRVEN	120
DSTRB#	137

Pin Name	Location
EVEN_ODD	132
GAVALEN	144
GND	2
GND	13
GND	20
GND	41
GND	51
GND	61
GND	71
GND	82
GND	91
GND	100
GND	110
GND	121
GND	141
HTIM	131
INT#	124
IO#	79
MD0	90
MD1	89
MD2	88
MD3	87
MD4	86
MD5	85
MD6	84
MD7	83
MD8	92
MD9	93
MD10	94
MD11	95
MD12	96
MD13	97
MD14	98
MD15	99
MD16	102
MD17	103
MD18	104
MD19	105
MD20	106
MD21	107

Pin Name	Location
MD22	108
MD23	109
MD24	111
MD25	112
MD26	113
MD27	114
MD28	115
MD29	116
MD30	117
MD31	118
MRDY#	142
MREQ#	150
MSG#	76
MSTRB#	138
MUX	31
NC	80
NC	119
NC	136
NC	160
NXTFST#	151
OR_MEM	127
RAS0#	23
RAS1#	24
RAS2#	25
RAS3#	26
REGSEL#	135
REQ#	78
RFSH#	153
RSTIN#	72
SEL#	73
SELA#	74
SEN0#	9
SEN1#	10
SEN2#	11
SEN3#	12
SRST#	68
SRSTA#	69
SYSRST#	126
TRNFR#	152
TROE#	15

Pin Name	Location
V1CLK	22
VA0	154
VA1	155
VA2	156
VA3	157
VA4	158
VA5	159
VA6	3
VA7	4
VA8	5
VA9	6
VA10	7
VA11	8
VA12	40
VA13	38
VA14	37
VA15	36
VA16	35
VA17	34
VA18	33
VA19	32
VA20	30
VA21	29
VA22	28
VA23	27
VBUS3	149
V_{CC}	1
V_{CC}	21
V_{CC}	39
V_{CC}	50
V_{CC}	60
V_{CC}	70
V_{CC}	81
V_{CC}	101
V_{CC}	122
V_{CC}	140
VSCSEL#	123
VWE#	143
WE#	14
YVUSEL	130S

Table 1-2. Pin Cross Reference by Pin Number

Pin Name	Location	Pin Name	Location	Pin Name	Location	Pin Name	Location
1	V_{CC}	41	GND	81	V_{CC}	121	GND
2	GND	42	DB0	82	GND	122	V_{CC}
3	VA6	43	DBA0	83	MD7	123	VSCSEL#
4	VA7	44	DB1	84	MD6	124	INT#
5	VA8	45	DBA1	85	MD5	125	CHANREQ#
6	VA9	46	DB2	86	MD4	126	SYSRST#
7	VA10	47	DBA2	87	MD3	127	OR_MEM
8	VA11	48	DB3	88	MD2	128	CS2FLG
9	SEN0#	49	DBA3	89	MD1	129	BRSTRQ#
10	SEN1#	50	V_{CC}	90	MD0	130	YVUSEL
11	SEN2#	51	GND	91	GND	131	HTIM
12	SEN3#	52	DB4	92	MD8	132	EVEN_ODD
13	GND	53	DBA4	93	MD9	133	DCLK
14	WE#	54	DB5	94	MD10	134	BRSTACK#
15	TROE#	55	DBA5	95	MD11	135	REGSEL#
16	CAS0#	56	DB6	96	MD12	136	NC
17	CAS1#	57	DBA6	97	MD13	137	DSTRB#
18	CAS2#	58	DB7	98	MD14	138	MSTRB#
19	CAS3#	59	DBA7	99	MD15	139	BUSEN#
20	GND	60	V_{CC}	100	GND	140	V_{CC}
21	V_{CC}	61	GND	101	V_{CC}	141	GND
22	V1CLK	62	DBP	102	MD16	142	MRDY#
23	RAS0#	63	DBPA	103	MD17	143	VWE#
24	RAS1#	64	ATN#	104	MD18	144	GAVALEN
25	RAS2#	65	ATNA#	105	MD19	145	BE0#
26	RAS3#	66	ACK#	106	MD20	146	BE1#
27	VA23	67	ACKA#	107	MD21	147	BE2#
28	VA22	68	SRST#	108	MD22	148	BE3#
29	VA21	69	SRSTA#	109	MD23	149	VBUS3
30	VA20	70	V_{CC}	110	GND	150	MREQ#
31	MUX	71	GND	111	MD24	151	NXTFST#
32	VA19	72	RSTIN#	112	MD25	152	TRNFR#
33	VA18	73	SEL#	113	MD26	153	RFSH#
34	VA17	74	SELA#	114	MD27	154	VA0
35	VA16	75	BSY#	115	MD28	155	VA1
36	VA15	76	MSG#	116	MD29	156	VA2
37	VA14	77	CD#	117	MD30	157	VA3
38	VA13	78	REQ#	118	MD31	158	VA4
39	V_{CC}	79	IO#	119	NC	159	VA5SS
40	VA12	80	NC	120	DRVEN	160	NC

1.2 Pin Descriptions

1.2.1 DVI BUS PIN DESCRIPTIONS

Symbol	Type	Name and Function
BE[3:0]#	BI	**BYTE ENABLES 3..0:** These signals are used to decode the CAS signals on the VRAM interface. These lines are latched at the leading edge of each CAS cycle.
CHANRQ#	O	**DMA CHANNEL REQUEST SIGNAL:** This signal is output to the HIGA to indicate a request to perform a memory operation. After VSCSEL# and BUSEN# are asserted CHANRQ# will be negated.
BUSEN#	I	**BUS ENABLE SIGNAL:** This signal is output by the 82750PB in response to a CHANRQ# indicating that access to the DVI Bus has been granted.
MSTRB#	O	**MEMORY STROBE SIGNAL:** A memory strobe pulse is generated for each non-82750PB cycle and is provided as a data valid strobe for VRAM and register access.
MRDY#	O	**MEMORY READY SIGNAL:** This signal is an output to the 82750PB indicating the end of a memory cycle.
DSTRB#	O	**DEVICE STROBE SIGNAL:** A pulse is generated on this signal whenever an access is made to one of the eight DVI devices. This signal is provided as a data valid strobe for register accesses.
DRVEN	I	**DRIVE ENABLE SIGNAL:** This signal is provided for testing purposes only. Bringing this signal low will switch all output and bidirectional pins their high impedance state.
GAVALEN	I	**GATE ARRAY VRAM ADDRESS LATCH ENABLE:** This signal is driven by the HIGA. The rising edge of the first V1CLK following the negation of GAVALEN latches address information from the MD[31:0] Bus onto the VA[23:0] Bus.
INT#	O	**INTERRUPT SIGNAL:** This signal is an output from the VSCGA that indicates to the Host that a service is being requested.
MD[31:0]	BI	**MEMORY DATA BUS:** This bus is the data path between the Host and the VSCGA, the VSCGA and VRAM or other DVI devices.
SYSRST#	I	**MASTER RESET SIGNAL:** Asserting this signal will reset all of the internal logic of the VSCGA and should only be used for power-on initialization.
V1CLK	I	**MASTER CLOCK SIGNAL:** This signal is driven by the KAGA and is used to drive the internal state machine and control logic in the VSCGA.
VA[23:0]	O/BI	**VRAM ADDRESS 23..0:** These signals are driven by the VSCGA for all non-82750PB cycles. They are driven active when BUSEN# is asserted by the 82750PB. VA2-4 and VA17-23 are bidirectional signals that are looped back and used as inputs to the VSCGA or are driven by the 82750PB and used by the CD-ROM subsystem logic. All other signals on this bus are outputs.
VSCSEL#	I	**VRAM SCSI CAPTURE SELECTION SIGNAL:** This signal is an input from the HIGA that indicates that the VSCGA is the next request to be serviced.
VWE#	BI	**VRAM WRITE ENABLE SIGNAL:** This signal is driven by the requesting DVI device during DVI device and VRAM transfers to indicate the direction of the transfer. A high indicates a read and a low indicates a write.
OR_MEM	O	**OR_MEM:** This signal is an output that is used for diagnostic purposes only and should be left unconnected for normal operation.

1.2.2 SCSI INTERFACE PIN DESCRIPTIONS

Symbol	Type	Name and Function
CD#	I	**CONTROL/DATA SIGNAL:** This signal is an input to the VSCGA that indicates whether control or data information is present on the SCSI bus. A high indicates control information is present and a low indicates data is present.
IO#	I	**INPUT/OUTPUT SIGNAL:** This signal is an input to the VSCGA that controls the direction of data movement. A high indicates data input to the VSCGA and a low indicates data output from the VSCGA.
MSG#	I	**MESSAGE SIGNAL:** This signal is an input to the VSCGA that is used during the message phase of a SCSI transfer.
REQ#	I	**REQUEST SIGNAL:** This signal is an input to the VSCGA that indicates a request for a REQ/ACK data transfer handshake.
BSY#	I	**BUSY SIGNAL:** This is an OR-tied input signal to the VSCGA that indicates whether the SCSI bus is being used.
RSTIN#	I	**RESET IN SIGNAL:** This signal is SCSI RST input to the VSCGA.
SRST# SRSTA#	O O	**SCSI RESET SIGNAL:** These two signals are externally tied together to meet the 48 mA current drive requirement of the SCSI standard. Together these two signals form the RST output from the VSCGA.
ACK# ACKA#	O O	**ACKNOWLEDGE SIGNAL:** These two signals are externally tied together to meet the 48 mA current drive requirement of the SCSI standard. Together these two signals form the acknowledge output from the VSCGA.
ATN# ATNA#	O O	**ATTENTION SIGNAL:** These two signals are externally tied together to meet the 48 mA current drive requirement of the SCSI standard. Together these two signals form the attention output from the VSCGA.
SEL# SELA#	BI O	**SELECT SIGNAL:** These two signals are externally tied together to meet the 48 mA current drive requirement of the SCSI standard. Together these two signals form the target select output from the VSCGA. SEL# can also be used by a target as the reselect input.
DB[7:0,P] DBA[7:0,P]	BI O	**DATA BUS SIGNALS:** Each of the corresponding bits of these two busses are externally tied together to meet the 48 mA current drive requirement of the SCSI standard. Together these two busses form the eight-bit data plus parity bus. Data parity is odd. When outputting the VSCGA drives both busses. When inputting only DB[7:0,P] is used.

1.2.3 VRAM INTERFACE PIN DESCRIPTIONS

Symbol	Type	Name and Function
RAS[3:0]#	O	**VRAM ROW ADDRESS SELECT SIGNALS:** These signals are used to select the VRAM row address. The RAS lines are not completely decoded.
CAS[3:0]#	O	**VRAM COLUMN ADDRESS SELECT SIGNALS:** These signals are used to select the VRAM column address. The CAS lines are decoded by the Byte Enable lines.
WE#	O	**WRITE ENABLE SIGNAL:** This write enable pin is used to allow for Write-per-bit operations and Write Enable. The DVI bus signal VWE# is latched at the beginning of a memory cycle and determines the state of WE#. If VWE# is latched low (active) then WE# will also be asserted low.
TROE#	O	**OUTPUT ENABLE SIGNAL:** This signal is used to allow for transfer operations and output enable. The DVI Bus signal VWE# is latched at the beginning of a memory cycle and determines the state of TROE#. If VWE# is latched high (inactive) then TROE# will be asserted low.
MUX	O	**MUX SIGNAL:** This signal transitions high to low on the falling edge of the system clock after RAS to signal a switch to the column address.
MREQ#	I	**MEMORY REQUEST SIGNAL:** This signal is an input from the 82750PB that indicates the beginning of a memory cycle.
NXTFST#	I	**NEXT-FAST ACCESS SIGNAL:** This signal is an input from the 82750PB that indicates that a fast page memory cycle may be done.
TRNFR#	I	**TRANSFER SIGNAL:** This signal is an input to the VSCGA indicating a transfer cycle.
RFSH#	I	**REFRESH SIGNAL:** This signal is an input to the VSCGA that indicates a memory refresh cycle.
SEN[3:0]#	O	**SERIAL ENABLE SIGNALS:** These signals are used to select the serial port on the 82750DB that is being addressed during a transfer.

1.2.4 CAPTURE INTERFACE PIN DESCRIPTIONS

Symbol	Type	Name and Function
VBUS3	I	**VBUS3 SIGNAL:** This signal indicates to the VSCGA that a transfer is taking place on the video bus.
BRSTACK#	O	**BURST ACKNOWLEDGE SIGNAL:** This signal is output from the VSCGA in response to a BRSTRQ# indicating to the Capture subsystem that it may drive the current data word in its FIFO onto the memory data lines.
BRSTRQ#	I	**BURST REQUEST SIGNAL:** This signal is an input from the Capture subsystem that indicates that there is captured video data in a FIFO ready to be transferred.
DCLK	O	**DATA CLOCK SIGNAL:** This signal is driven by the VSCGA to indicate that a video data word has been stored to VRAM. DCLK is a free-running clock.
HTIM	I	**HORIZONTAL TIME SIGNAL:** This signal carries an active high pulse from the Capture subsystem for each horizontal line.
EVEN__ODD	I	**EVEN/ODD SIGNAL:** This signal is an input from the Capture subsystem that indicates to the VSCGA which field is currently being captured. Low indicates an even field and high indicates an odd field.

1.2.4 CAPTURE INTERFACE PIN DESCRIPTIONS (Continued)

Symbol	Type	Name and Function
YVUSEL	I	**YUV SELECT SIGNAL:** This signal is an input from the Capture subsystem that indicates the type of data to be transferred in a video data burst cycle. A Y burst is indicated when this signal is low and a UV burst is indicated when it is high.
REGSEL#	O	**REGISTER SELECT SIGNAL:** This signal is an output from the VSCGA to the Capture subsystem that indicates that a register access is being performed.
CS2FLG	I	**CAPTURE FLAG SIGNAL:** This signal is active high and is driven by the Capture subsystem to indicate when register read data is ready or when register write data has been accepted.

2.0 INTERNAL ARCHITECTURE

2.1 VRAM and Capture

2.1.1 OVERVIEW

Video data typically enters the VRAM through its parallel port, originating from the Capture Module, the SCSI interface or from the Host Interface Gate Array. Once in memory it can be processed by the Intel 82750PB Pixel Processor (PB). The data can then be displayed by shifting it out of the VRAM serial port to the Intel 82750 Display Processor (DB). Each of these operations is supported by the VRAM and Capture portion of the VSCGA gate array whose internal architecture is shown in Figure 2-1. Before each of its component blocks is examined, the functionality of the VSCGA chip will be described.

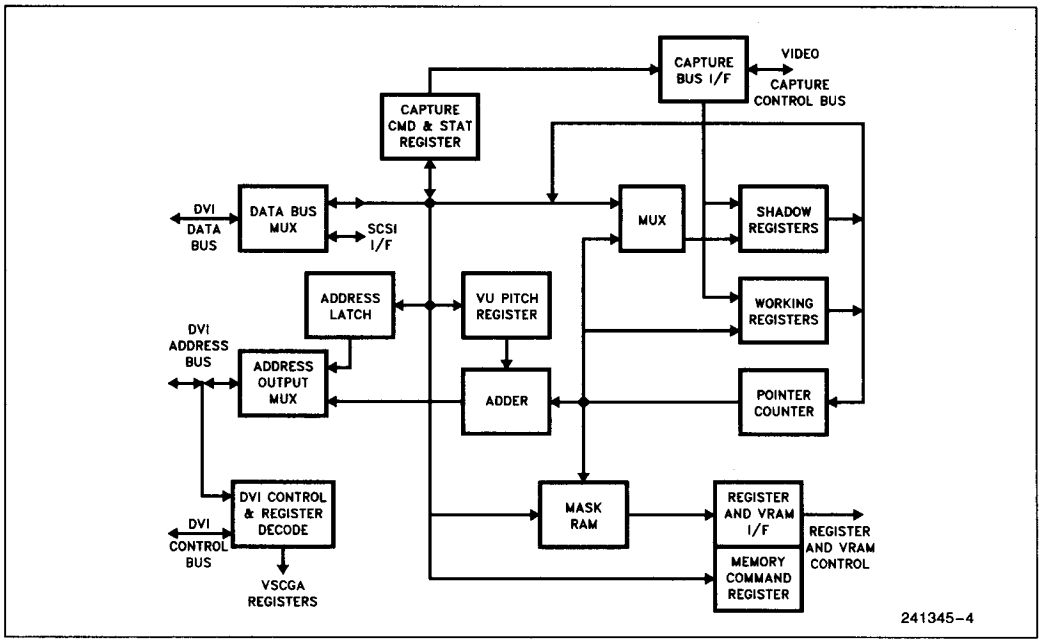


Figure 2-1. VRAM and Capture Gate Array Architecture

One function of the VSCGA chip is to drive the VRAM Address lines. It does this for all DVI Bus cycles where the Intel Pixel Processor is not the bus master. When addresses from other DVI devices are placed on the time-multiplexed DVI Data Bus, VSCGA latches the information and uses it to drive the VRAM Address Bus. The address data can also originate internally from video capture write cycles and SCSI data acquisition. Driving VRAM addresses is hardware-efficient since other chips driving the DVI Bus do not have to implement the entire VA(23:0) Bus as well as the MD(31:0) Bus.

The VSCGA can support the accessing of up to 4 MB of memory in 1 MB increments using 256K x 4 VRAM chips, or up to 16 MB of memory in 4 MB increments using 1 MB x 4 VRAM chips. Each Megabyte of the lower density chips consists of 8 integrated circuits making up the 32-bit wide data path. Chip selection is controlled by CAS on each chip which is in turn controlled by the byte enable lines, BE(3:0), on the DVI Bus. Each 4 Megabytes of the higher density memory is similarly configured. The VSCGA chip always assumes that the maximum amount of memory is installed and generates VRAM cycles accordingly. If this is not the case a software check may be in order to determine how much memory is available.

The VSCGA monitors the DVI Bus for VRAM and DVI Bus Register accesses, and when detected, generates the timing and control to execute the cycles. The following operations are supported:

Single VRAM Read-Write cycle. Either the Intel Pixel Processor or any other DVI Device can read or write to a single 32-bit VRAM location. This also includes the ability to address 16- and 8-bit locations using BE(3:0).

Dual VRAM Read-Write cycle. Either PB or any other DVI Device can read or write to two consecutive 32-bit VRAM locations (where the first word has an even word address) using page mode access. This is more efficient than a single cycle access because less time is spent acquiring the DVI Bus from PB, asserting RAS and waiting between accesses.

VRAM Transfer cycle. Transfer cycles are used to load the VRAM serial shift register with data for the Intel Display Processor. DB makes requests for various types of data transfers of PB, which then initiates those cycles.

VRAM Refresh cycle. Refresh cycles are initiated by DB and executed by PB. Every output horizontal line time, DB issues a refresh request to PB over the VBUS. For each request, up to 15 refresh cycles are initiated by the Pixel Processor. During refresh cycles all banks of VRAM are addressed.

Single DVI Register Read-Write cycle. Either the Intel Pixel Processor or any other DVI Device can read or write to a single 32-bit DVI Register location. This also includes the ability to address 16- and 8-bit locations using BE(3:0).

Capture cycle. Bursts of captured video are stored in VRAM under DMA control. The length of these bursts is not usually limited by the gate array. Address pointers stored in the gate array are automatically updated as the data is processed. A write mask can be employed which prevents the writing of particular areas of the memory. Additionally, write-per-bit operations are supported which prevent the writing of particular bit positions and assist the Intel Display Processor in the mixing of graphics and video data.

Burst Read cycle. Bursts of VRAM data are loaded into the Mask RAM under DMA control. Either 2, 4 or 8 page-mode cycles are executed before the DVI Bus is relinquished.

Video capture operations are supported in conjunction with a video Capture Module containing a complete digitizing interface to analog YVU or RGB data in interlaced NTSC or PAL format. The video Capture Module is relatively independent of the VSCGA, and, once programmed using the Capture Module Command and Status Register, will continuously generate digitized fields of video data and output them to the gate array without further commands.

Captured video data is transferred to VRAM in bursts through a series of Capture Module requests to VSCGA for use of the DVI Data Bus. Each request is passed on to the Host Interface Gate Array for prioritization, and when bus access is granted, a sequence of only one type of data is written to memory. For YVU data with subsampled chroma, this is either Y data or a combination of VU data, selectable by the Capture Module each burst. For RGB and 24-bit YVU data, each component is sent for a minimum of an entire field. These transfers are a high DVI priority and are interruptible only by a DB VRAM data transfer request.

During video capture, the gate array monitors video timing signals from the Capture Module to control where data is stored in memory. VSCGA is able to keep data from successive fields and YVU components from within a field in separate areas of memory as programmed by the Intel Pixel Processor or other DVI Bus Device. This operation is handled by two sets of Shadow Registers, one for even and one for odd fields, one set of Working Registers, a Pointer Counter, a VU Pitch Register and an Adder. Each set of Shadow Registers and the set of Working Registers contains one memory pointer for Y data,

one for VU data and one for Input Mask data. Immediately before even field processing begins, the previously programmed Even Shadow Registers are used to load data into their respective Working Registers. The information transferred consists of starting locations in VRAM in which to deposit Y and VU data and from which to read mask information. During the field, as various data and timing signals are received from the Capture Module, the Pointer Counter selectively uses the Working Registers to generate updated addresses, which are used for DMA accesses to VRAM and then stored back in the respective registers. Before the completion of the even field, it is necessary to program the set of Odd Shadow Registers, which will automatically be used at the beginning of the next field. It is also possible to program the gate array to keep V and U data separate in memory. VSCGA accomplishes this by adding a fixed offset from the VU Pitch Register to the Pointer address only while processing U data.

Captured data can be transferred to memory in six different formats. They are Y8, YVU9, YVU10, YVU12, YVU24 and RGB24. Y8 mode contains only 8-bit luminance data. In YVU9 mode V and U data are subsampled 4:1 in both horizontal and vertical directions. In YVU10 mode, V and U data are subsampled 4:1 in the horizontal and 2:1 in the vertical direction. In YVU12 mode, V and U data are subsampled 4:1 in the horizontal and sampled each line vertically. The 24-bit modes are used for higher quality still images. Capture is accomplished over six fields. During the first two, R or Y data is stored. During the second two, G or V data is captured and during the third two, B or U data is transferred to memory. In these modes, the Odd and Even Shadow Registers alternate each field and can be loaded in such a way as to keep the three components separated in VRAM. While the first three display formats are "VRAM-compatible" with the Intel Display Processor, the last three cannot be directly displayed without first reformatting them in VRAM.

Interlaced fields of data can easily be interleaved into complete frames as they are written into VRAM by making the proper choice of register parameters. For example, if a 640 x 480 (280H x 1 E0H) resolution image with VU subsampled by 4 in each direction is captured (YVU9 mode), setting the Y horizontal resolution for 2048 (800H) pixels and offsetting the odd and even fields by 1024 (400H) pixels will integrate the two luminance scans. Setting the combined chrominance horizontal resolution for 1024 (400H), offsetting the U by 256 (100H) and offsetting the odd and even fields by 512 (200H) will integrate the two components of the two chrominance scans. A memory map of this structure is illustrated in Figure 2-2.

The foregoing discussion illustrates the capability of the VSCGA gate array. In actual system operation, the capture of interlaced video alternates between Y8 and YVU10 modes on successive fields with chrominance data captured only every other field. This results in VU data being temporally as well as spatially subsampled with only a minor effect on picture quality.

2.1.2 REGISTER CONFIGURATION

There are ten memory-mapped DVI Registers in the VRAM and Capture portion of the VSCGA array. Table 2-1 shows a listing of their names, addresses, lengths and accessibility from the DVI Bus. All are located in the range from FC0000H to FC0021H, conforming to a DVI Device ID of 6. Each can be accessed with either byte, word or long word operations.

Table 2-1. VRAM and Capture Register Configuration

Register	DVI Address	DVI R/W	Register Length	Register Description
Y_EVEN	FC0000H	R/W	32 Bits	Even Field Y Shadow Register
VU_EVEN	FC0004H	R/W	32 Bits	Even Field VU Shadow Register
MASK_EVEN	FC0008H	R/W	32 Bits	Even Field Mask Shadow Register
Y_ODD	FC000CH	R/W	32 Bits	Odd Field Y Shadow Register
VU_ODD	FC0010H	R/W	32 Bits	Odd Field VU Shadow Register
MASK_ODD	FC0014H	R/W	32 Bits	Odd Field Mask Shadow Register
VU_PITCH	FC0018H	R/W	8 Bits	V-U Interleave Register
CAP_CST	FC001AH	R/W	16 Bits	Capture Command and Status
MEM_CMD	FC001CH	W	32 Bits	Memory Command
CM_CST	FC0020H	R/W	16 Bits	Capture Module CMD and Status

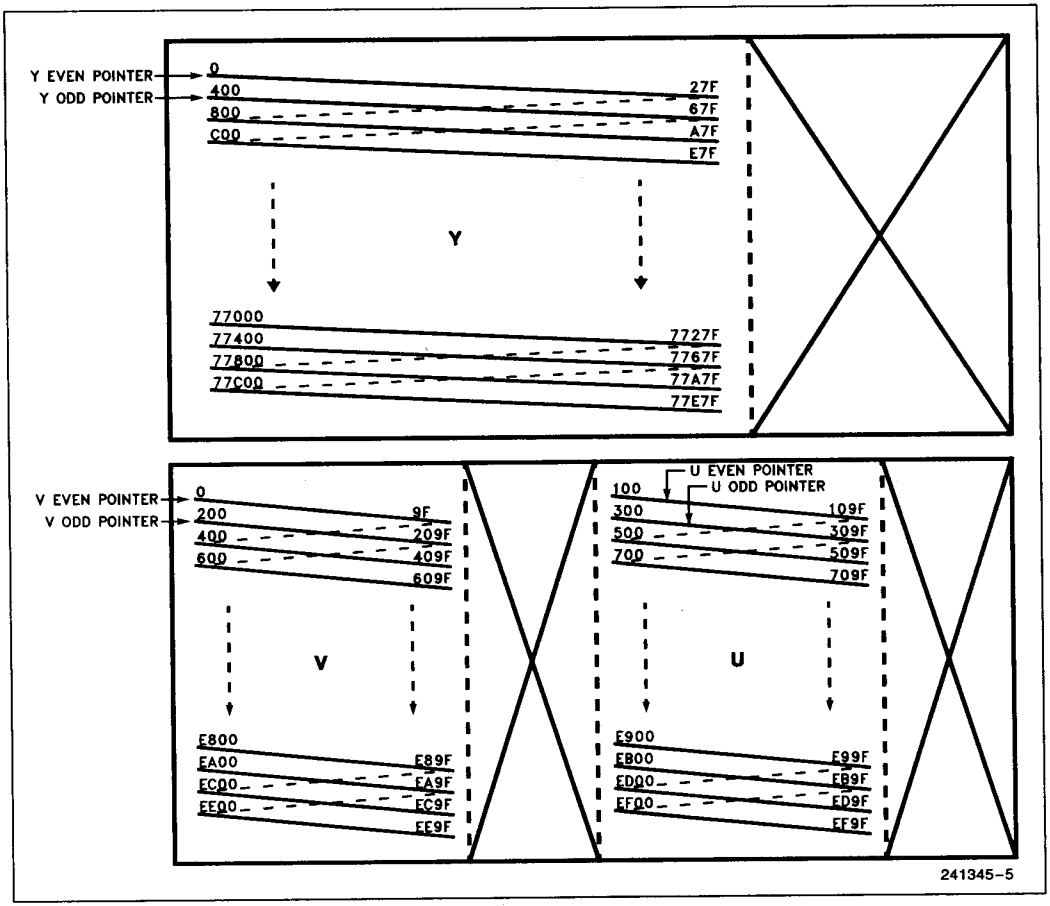


Figure 2-2. YVU Memory Map

2.1.3 MEMORY COMMAND REGISTER

This write-only register is used to program the timing parameters used in memory and register accesses to accommodate different speed VRAMs and various system clock rates. It also determines whether the 1 or 4 Megabyte VRAM addressing scheme is implemented. Finally, it stores the write-per-bit mask used to selectively write captured video data.

2.1.4 REGISTER AND VRAM INTERFACE

This logic block accepts the timing parameters and write-per-bit mask information from the Memory Command Register and write mask information from the Mask RAM and generates the signals necessary to access VRAM and DVI registers.

2.1.5 MASK RAM

As the Pointer Counter develops addresses to write captured video data to memory, these addresses are simultaneously used as pointers into a Mask RAM which may be used to selectively inhibit these write cycles. Each bit of this 24-byte RAM controls the write access to a single V and U pixel and to the corresponding 4 x 4 or a 4 x 2 array of Y pixels, for the YVU9 and YVU10 modes respectively. If this mode is enabled, data will not be written to masked locations even though DVI Bus cycles will be consumed in making the data available at the VRAM inputs. The number of bits of RAM that are used is dependent on the horizontal resolution of the captured image. For example, an image with Y resolution of 256 x 240 requires only 256 ÷ 4 or eight

bytes, while one with a horizontal resolution of 768 needs the full 24-byte storage. When this RAM is in use, it is automatically loaded at the beginning of the first video line using the appropriate Odd or Even Shadow Mask Register. Its data is reused until it is updated at the beginning of every two or four lines, depending on the vertical chroma resolution.

2.1.6 SHADOW REGISTERS AND MUX

These six read-write registers are used to store two sets of initial pointers to VRAM for captured Y and VU video and mask data: one set for even and one set for odd fields. They also store information indicating the number of bytes of memory to allocate for each horizontal line of data. This number is used to indicate to the Pointer Counter how much to increment the Working Register at the end of each line and is always a power of two regardless of the actual resolution. These registers also contain additional information which determines other operational details of their use.

The Mux allows data from the DVI Data Bus to be loaded into the Shadow Registers and, in one mode of operation, permits the Shadow Registers to be continuously updated from the Pointer Counter during a field. This allows the DVI Bus to monitor the state of various address counts in real time since neither the Working Counters nor the Pointer Counter are accessible to that Bus.

2.1.7 WORKING REGISTERS

Each of these three registers are loaded, one at a time, at the beginning of each field of captured video, from its respective Even or Odd Shadow Register. Each 32-bit quantity is passed through the Pointer Counter, which is transparent for this operation. (Refer to Figure 2-1.) Depending on the programming mode, the pixel portion of the count may be set to 0 as it is loaded. The Y data is transferred first, followed by VU and finally by the Input Mask data. If the input mask mode is selected, the Mask RAM is immediately loaded using the Input Mask Working Register as an address source, which is updated each DMA read cycle by the Pointer Counter. Only after the Mask RAM is loaded can burst requests from the Capture Module be processed. As each request is received the data type is specified so that the appropriate Working Register (Y or VU) is loaded into the Pointer Counter, used as a VRAM write address and updated after each DMA write cycle. At the end of each burst, the Working Register contains the location of the next pixel to be written. This value is ready to be reloaded into the Pointer Counter the next time the same type of burst data is requested during that line. At the end of each horizontal line, the three Working Register outputs are sequentially passed through the Pointer Counter and their line counts are selectively incremented before being restored in those same registers. The decision to increment each register depends on the status of an activity monitor associated with each Working Register. The Y and VU activity monitors detect the capture of the respective data type during each horizontal line. The Mask monitor detects the fetching of the mask data from VRAM during that time. Only when the monitor outputs are asserted are the Working Register line counts incremented. Depending on the programming mode, the pixel count may either be set to 0 or loaded with the corresponding bits from the respective Shadow Register.

2.1.8 POINTER COUNTER

This is a flexible logic block that accepts and processes 32-bit inputs from the six Shadow Registers and the three Working Registers. It then processes those inputs and makes them available to those same registers and to the DVI Address Bus through the VU Pitch Register Adder and the Address Output Mux. The processing can be minimal, such as at the beginning of a field when the Shadow Registers are used to load the Working Registers; or it can be more substantial, such as during a horizontal line when pixel counts are incremented (by four for each 4-byte read) or at the end of each horizontal line when the line count is incremented. The bit position in the 24-bit Counter where pixel count ends and line count begins is dependent on the horizontal resolution, the video component, the amount of subsampling of that component and whether interleaving of the interlaced data is being performed. The bit position information is programmed into each Shadow Register and passes through the various processing loops along with the address.

2.1.9 VU INTERLEAVE REGISTER AND ADDER

This register contains one byte of storage which, when enabled, allows the V and U data from subsampled chroma fields to be accumulated in distinct areas of VRAM. The VU data comes from the Capture Module alternating between four bytes of V and four bytes of U data. The VU Interleave Register contents are multiplied by eight and then combined only with addresses for U data in the Adder (V addresses pass through unmodified). The result is used to determine the VRAM location for the captured data. Note that the eight bits of pitch are not sufficient to totally separate the U and V components in memory, but are enough to allow them to be placed side-by-side as shown in Figure 2-2.

2.1.10 DATA BUS MUX

This block is a bidirectional interface to the DVI Data Bus from both the SCSI and the VRAM and Capture

portions of the VSCGA gate array. In this portion of the array it is used to read and write register data and to pass the time-multiplexed address data to the Address Latch.

2.1.11 ADDRESS LATCH

This block latches the time-multiplexed address data from the DVI Data Bus, MD(31:0) and supplies it to the DVI Address Bus, VA(23:0). This allows other DVI Bus components to implement only the MD(31:0) signals for output addressing and data transfers and the few VA bits they need to decode their own register addresses.

2.1.12 ADDRESS OUTPUT MUX

This block selects between the Address Latch and the Pointer Counter (or Adder) outputs as a source for the DVI Address Bus.

2.1.13 CAPTURE COMMAND AND STATUS REGISTER

This register controls several of the parameters for capturing data and allows the DVI Bus to monitor some of the control signals from the Capture Module.

2.1.14 CAPTURE MODULE COMMAND AND STATUS REGISTER

This Register is located in the Capture Module. VSCGA provides the control to interface this register to the DVI Bus by decoding a bus strobe.

2.2 SCSI Interface

2.2.1 OVERVIEW

This portion of VSCGA contains a DMA interface from the SCSI Bus to the DVI Bus. This capability is important because it provides a high-speed path for the input of CD-ROM data, a major source of compressed DVI images. The DVI Bus interface allows the operations preliminary to the data transfer to be set up by software, using a set of registers inside the gate array, but the DMA transfer itself can be automatically carried out by a State Machine within the array. Up to sixteen Megabytes of VRAM memory can be addressed by the DMA controller, although the topmost Megabyte is reserved for DVI Bus Devices. The VSCGA implements a complete single-initiator, multiple-target, single-ended SCSI Bus with parity, capable of controlling up to 8 devices. Being a single initiator system implies that neither an Arbitration nor a Reselection Phase is implemented on the SCSI Bus and results in a simplified protocol. In the rest of this specification the CD-ROM interface and operation will be used as an example of the Target Device. Please keep in mind that the interface is general and can handle both read and write DMA operations. For a complete description of the SCSI standard, refer to the ANSI document X3.131.

The VSCGA DMA Controller has the ability to gather discrete data blocks from the CD-ROM Subsystem and form them into a continuous data stream or to split a continuous data stream into discrete blocks. A typical CD-ROM data transfer works as follows: Once the preliminary Target Device protocol has been completed (Target selected) and the location of the first Chain Block in VRAM has been stored in the array, the DMA Controller is enabled and fetches and internally stores this block of data. Each of the memory-contiguous 12-byte Chain Blocks consists of an initial byte address to load the incoming data, a byte count and control information. This information is used by the Controller to direct data output from the CD-ROM to one or more areas in VRAM. As the 8-bit data is accumulated into 32-bit words and written into VRAM, the DMA Byte and Address Register counts are updated. This continues until byte count reaches 0, at which time a new Chain Block is automatically fetched. The process completes when a terminator flag is found to be set in the fetched Chain Block. Once the CD-ROM completes its data transfer, (which may span more than one Chain Block operation), the Target status is read followed by a message from the Target indicating that the read is complete. Several registers in VSCGA are used to send commands and messages out, accept status and input messages and monitor the SCSI Bus and State Machine operation. An internal Pattern Generator is also included for self-test.

A detailed block diagram of the SCSI portion of the VSCGA gate array is shown in Figure 2-4.

2.2.2 CHAIN BLOCKS

In order to perform a CD-ROM DMA transfer, a set of Chain Blocks exactly matching the retrieved data organization must be stored contiguously in VRAM. The format of each Chain Block is shown in Figure 2-3. In the lowest address is the byte count, which is a 24-bit number in two's complement format. The most significant byte of the word should be set to FF for future compatibility. The next higher address contains the the 24-bit Byte Address of the starting location for stored data. The most significant byte of this word should be 0. The lowest byte of the next word contains control information, including whether this Chain Block is the last one in the transfer.

31	23	15	7	0
FF	Byte Count			
0	Byte Address			
0	0	0	Control	

Figure 2-3. Chain Block Format

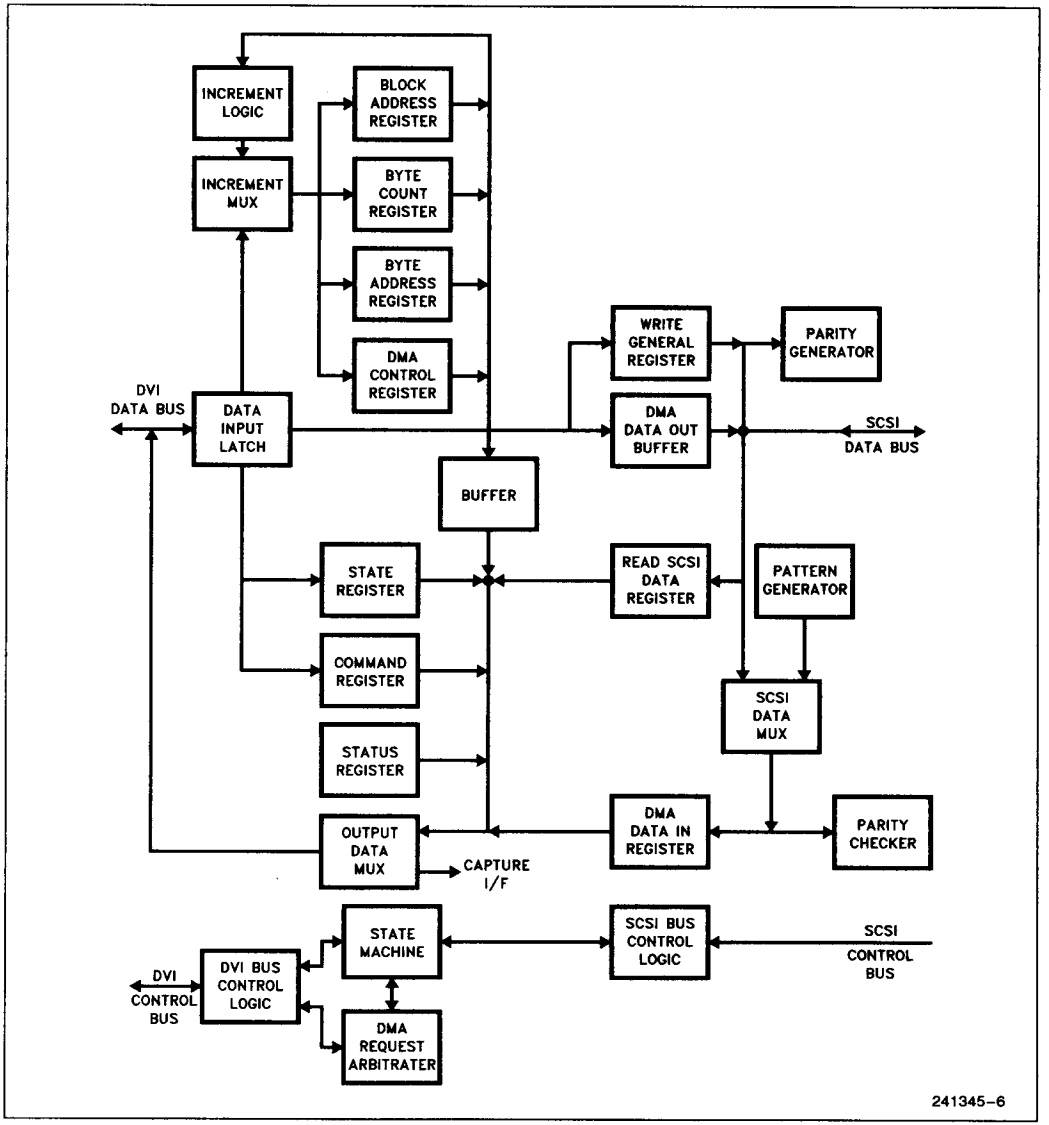


Figure 2-4. SCSI Gate Array Architecture

2.2.3 REGISTER CONFIGURATION

There are nine memory-mapped DVI Registers in the SCSI portion of the VSCGA array. Table 2-2 shows a listing of their names, addresses, lengths and accessibility from the DVI Bus. All are located in the range from F80000H to F80021H, conforming to a DVI Device ID of 4. Each can be accessed with either byte, word or long word operations.

2.2.4 CHAIN BLOCK ADDRESS REGISTER

At the start of a CD-ROM transfer, this register stores the address of the initial Chain Block. When the DMA process begins, Chain Block data is automatically read from VRAM in three long words fetches. After each one, the register is incremented by four to point to the next long word to be fetched.

2.2.5 BYTE COUNT REGISTER

This register is automatically loaded at the beginning of a DMA transfer from the current Chain Block with the 24-bit two's complement byte count corresponding to the number of CD-ROM bytes that are to be stored in a given area of memory. As the transfer progresses, each four bytes is accumulated in the DMA Data In Register and it is then transferred to VRAM. The Byte Count register is then incremented by four and tested for zero. If zero, the next Chain Block is fetched unless the last block has been reached. If not zero, the transfer continues.

2.2.6 BYTE ADDRESS REGISTER

This register is automatically loaded from the current Chain Block at the beginning of a DMA transfer with the initial 24-bit byte VRAM address to begin loading the CD-ROM data. After each transfer to VRAM, it is incremented by four to point to the byte address of the next long word.

2.2.7 DMA CONTROL REGISTER

The lower byte of this 16-bit register is automatically loaded from the current Chain Block at the beginning of a DMA transfer with control information. The upper byte contains additional control information loaded directly from the DVI Bus.

2.2.8 COMMAND REGISTER

This 16-bit register is used to control the activity on the SCSI Bus.

2.2.9 STATUS REGISTER

This read-only register monitors the status of the SCSI Bus.

2.2.10 READ SCSI DATA REGISTER

This one byte register is a buffer which allows status and message information on the SCSI Data Bus to be read.

2.2.11 WRITE GENERAL REGISTER

This one byte register stores command and message data as well as the Target ID to be placed on the SCSI Bus.

2.2.12 STATE REGISTER

This register allows for the monitoring of the internal State Machine and DMA Controller.

Table 2-2. SCSI Register Configuration

Register	DVI Address	DVI R/W	Register Length
Chain Block Address Register	F80000H	R/W	32 Bits
Byte Count Register	F80004H	R/W	32 Bits
Byte Address Register	F80008H	R/W	32 Bits
DMA Control Register	F8000CH	R/W	16 Bits
Command Register	F80010H	R/W	16 Bits
Status Register	F80014H	R/W	16 Bits
Read SCSI Data Register	F80018H	R/W	8 Bits
Write General Register	F8001CH	W	6 Bits
State Register	F80020H	R/W	16 Bits

2.2.13 INCREMENT LOGIC AND MUX

These logic blocks allow the Block Address Register, the Byte Count Register and the Byte Address Register to be loaded from the DVI Bus and incremented by four during a DMA process.

2.2.14 DATA INPUT LATCH

This non-addressable register latches the data from the MD(31:0) DVI Data Bus so that it is available for a longer period of time.

2.2.15 DMA OUTPUT BUFFER

This four-byte register is used for DMA writes to the SCSI Bus. Although the register cannot be loaded directly, DMA reads are automatically stored here until the State Machine outputs the bytes, one at a time, to the SCSI Bus.

2.2.16 DMA DATA IN REGISTER

This register accumulates one-byte data words from the SCSI Bus until they can be written to the VRAM as a four-byte quantity.

2.2.17 PARITY GENERATOR

This logic block generates odd parity for the data output to the SCSI Bus.

2.2.18 PATTERN GENERATOR

This logic block generates cyclic data for the self-test of the DMA data read operation.

2.2.19 SCSI DATA MUX

This logic block selects between the SCSI Bus and the Pattern Generator as the source of SCSI data for the system.

2.2.20 PARITY CHECKER

This logic block checks the parity of data emerging from the SCSI Data Mux.

2.2.21 DVI AND SCSI BUS CONTROL LOGIC

These logic blocks contain all the drivers, receivers and associated logic for each of the control signals on their respective bus.

2.2.22 STATE MACHINE

This eight-state logic block controls the DMA transfers between the SCSI Bus and the DVI Bus.

2.2.23 DMA REQUEST ARBITRATER

This logic block arbitrates the four DMA requests from the Input Mask fetch, Chain Block fetch, Capture Logic and the SCSI State Machine.

3.0 HARDWARE INTERFACE

A diagram of the VSCGA gate array interconnections is shown in Figure 3-1. These signals will be described in the following sections in conjunction with various operations performed by the VRAM, Capture and SCSI subsystem.

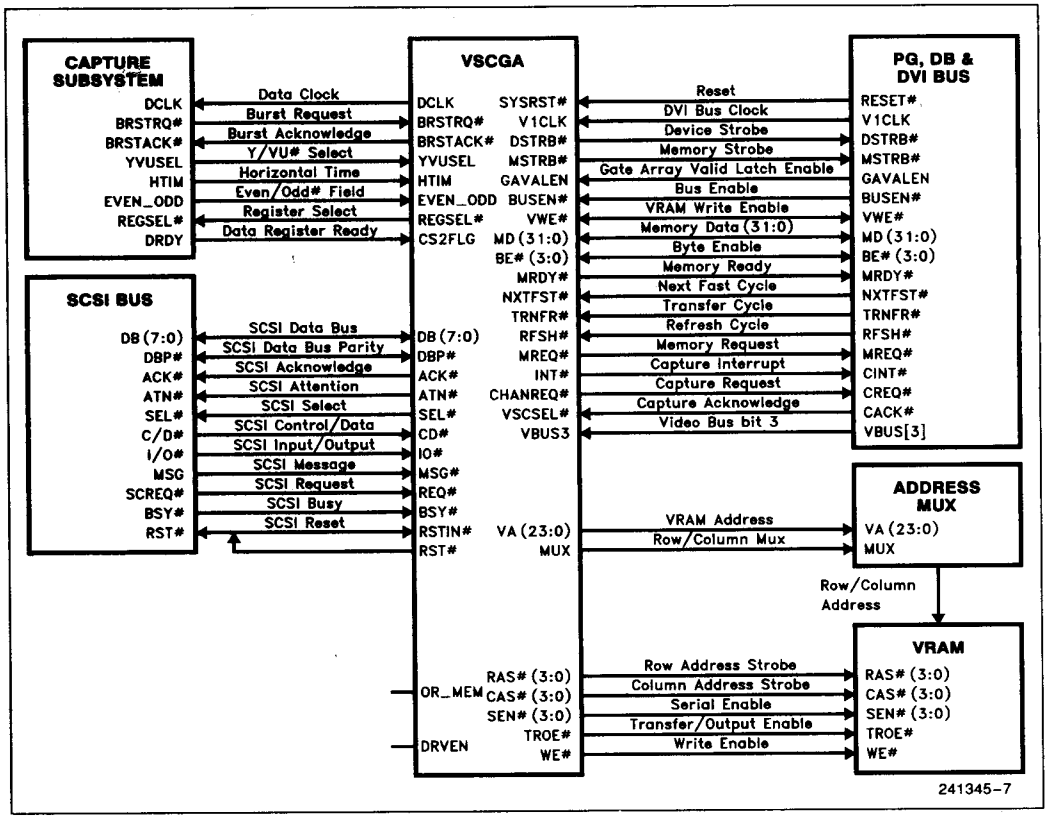


Figure 3-1. VSCGA System Interconnections

3.1 DVI Address Latching

Whenever (1) a DVI Bus cycle takes place (indicated by MREQ# asserted low) simultaneous with (2) BUSEN# asserted low (indicating that PB is not the Bus Master) and (3) the Pointer Counter is not the source of the address, then the VSCGA gate array latches the time-multiplexed address from the MD(31:0) lines on the falling edge of GAVALEN. The VA(23:0) address drivers are already enabled by the assertion of BUSEN# and the address becomes valid after the positive edge of V1CLK following GAVALEN going to 0. The address becomes invalid on the positive edge of the V1CLK after GAVALEN again rises to a 1, and the VA(31:0) lines tristate immediately after BUSEN# goes to a 1. This is demonstrated in Figure 3-2.

While the least significant 24 MD bits contain the VRAM address, the most significant bit determines the length of non-PB-initiated accesses. If MD31 is a 0 or 1 at the falling edge of GAVALEN, it indicates that the access is a single or a dual page-mode cycle, respectively. In the case of a dual page-mode cycle, the VA2 line must be a zero (an even 32-bit word address) for the first cycle and a one for the second. By contrast, PB asserts the NEXTFAST# signal during its accesses to execute a dual page-mode cycle.

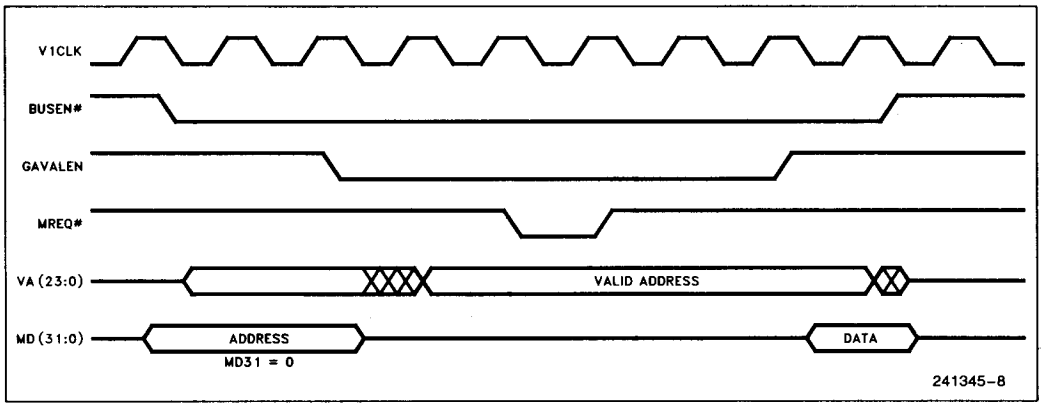


Figure 3-2. Latching of MD Address Information

3.2 VRAM and Capture

For additional information about the capture process, refer to the ActionMedia II Capture Bus Specification.

3.2.1 VRAM AND REGISTER ACCESS

In addition to latching the VA(23:0) Address Bus, the VSCGA chip supports DVI VRAM and Register accesses in several ways: (1) It monitors the DVI Address Bus and determines whether the address corresponds to the VRAM or register space. All addresses below F00000H point to VRAM and consequently the gate array outputs a memory strobe (MSTRB#) at the appropriate time during those cycles. For multiple cycle accesses this signal indicates when the address may be changed. Similarly, for higher addresses up to the maximum FFFFFFH, the chip outputs a data strobe (DSTRB#) indicating a register access. This signal allows other bus interfaces to develop chip enables without having to decode the address lines. (2) It monitors the DVI Control Bus, determines the bus master (the Intel 82750 Pixel Processor or other DVI Device) and for VRAM cycles determines the type of cycle. Single read-write, Dual page-mode read-write (NXTFST and BUSFAST), transfer, refresh and continuous page-mode read-write cycles for capture are all supported. (3) It allows the programmer to independently select timing parameters for a variety VRAM read and write and register control signals, including CAS#, RAS#, MSTRB# and DSTRB#. This feature accommodates a wide variety of clock and VRAM speeds.

The VRAM addressing is organized such that the four RAS# outputs reflect the most significant bits of memory, only one of which can be active at a time (except during refresh), while the four CAS# outputs represent the byte enables (BE3# . . . BE0#) and are not mutually exclusive. The CAS# outputs each enable 8 output bits and will all be active simultaneously when a 32-bit word is being addressed.

Single Cycle VRAM Access

A single VRAM read cycle followed by a single VRAM write cycle is shown in Figure 3-3. For simplicity, the diagram does not show the bus mastership acquisition required for non-PB-initiated cycles. The read cycle begins with the assertion of MREQ# by PB (regardless of bus ownership.) Once the cycle is begun, time is allowed for the row address to propagate through the external Address Mux at which time RAS# is asserted. Shortly thereafter, the Mux output is switched from high to low, causing the column address to appear at the output of the external Address Mux. After a short delay CAS# and TROE# are asserted, completing the address and enabling the VRAM output. One V1CLK cycle later MRDY# is asserted indicating that data can be latched at the next rising edge of V1CLK.

The second cycle in Figure 3-3 is a write cycle. The timing is very similar to the read cycle except that TROE# remains unasserted and the WE# output is enabled. In this cycle the assertion of MRDY# indicates that the data will be latched in VRAM at the rising edge of that signal. Note that while the write cycle request is asserted at the earliest possible opportunity, the cycle is delayed by one V1CLK pulse. Whenever two or more contiguous requests are received, VSCGA automatically delays the generation of the second cycle to meet the minimum VRAM timing requirement for RAS# to be unasserted between cycles (RAS Precharge).

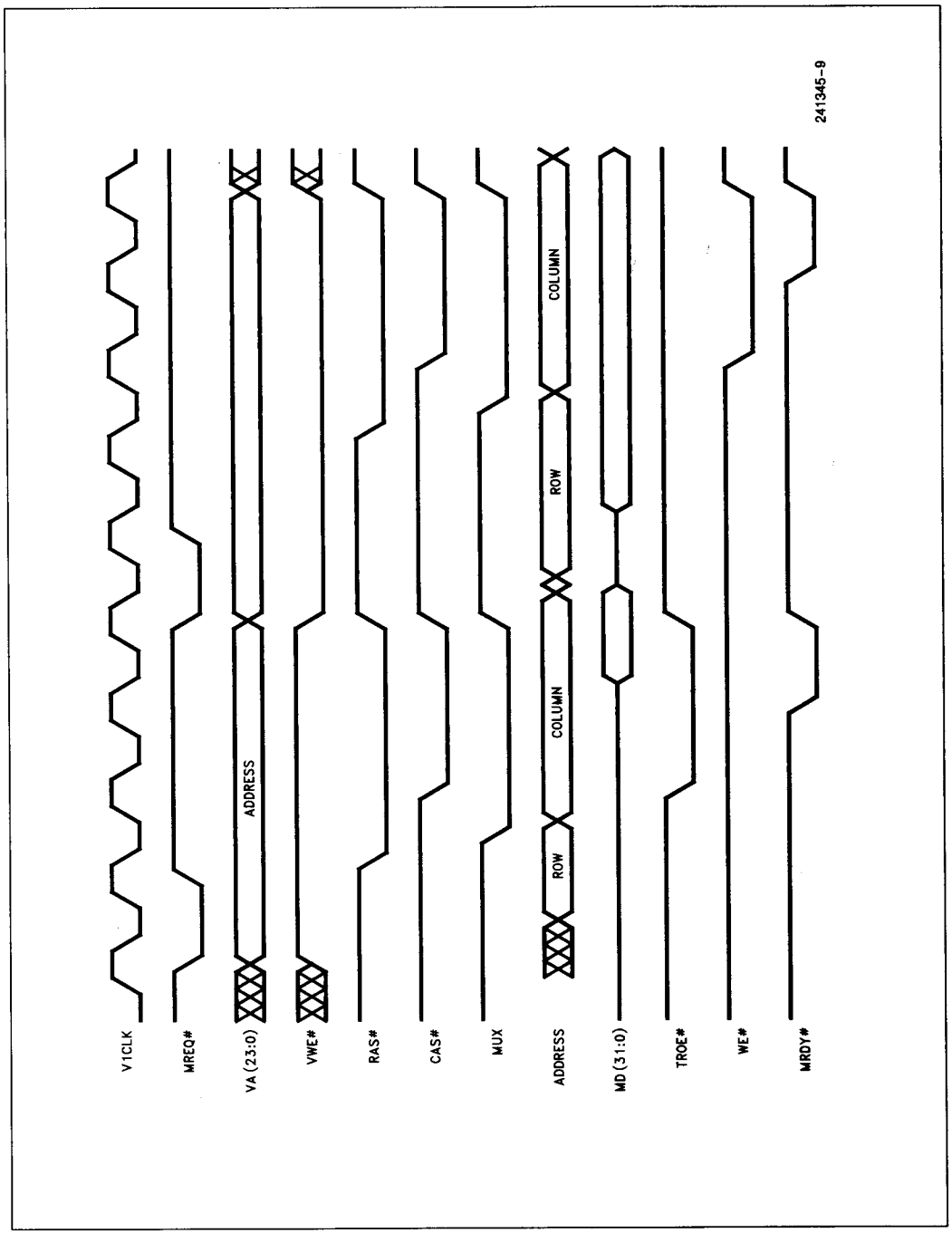


Figure 3-3. Single VRAM Read and Write Cycles

Dual-Cycle Page-Mode VRAM Access

There are two very similar dual page-mode VRAM cycles supported by VSCGA. The first is the NXTFST cycle which is one initiated by the PB. The second is a BUSFAST cycle which is initiated by any other DVI Device. A NEXTFAST read cycle is shown in Figure 3-4. The gate array looks for the simultaneous assertion of MREQ# and NXTFST# as the V1CLK goes high to generate this cycle. The waveforms are similar to that of the single read cycle with the following exceptions: (1) There are two CAS# strobes for the RAS# strobe. (2) The first access must be an even word address (VA2 = 0) and the second the next higher odd address (VA2 = 1). (3) There is no delay due to RAS# being unasserted.

Note that there is an MRDY# strobe after each access to indicate that data is available and the cycle may be ended.

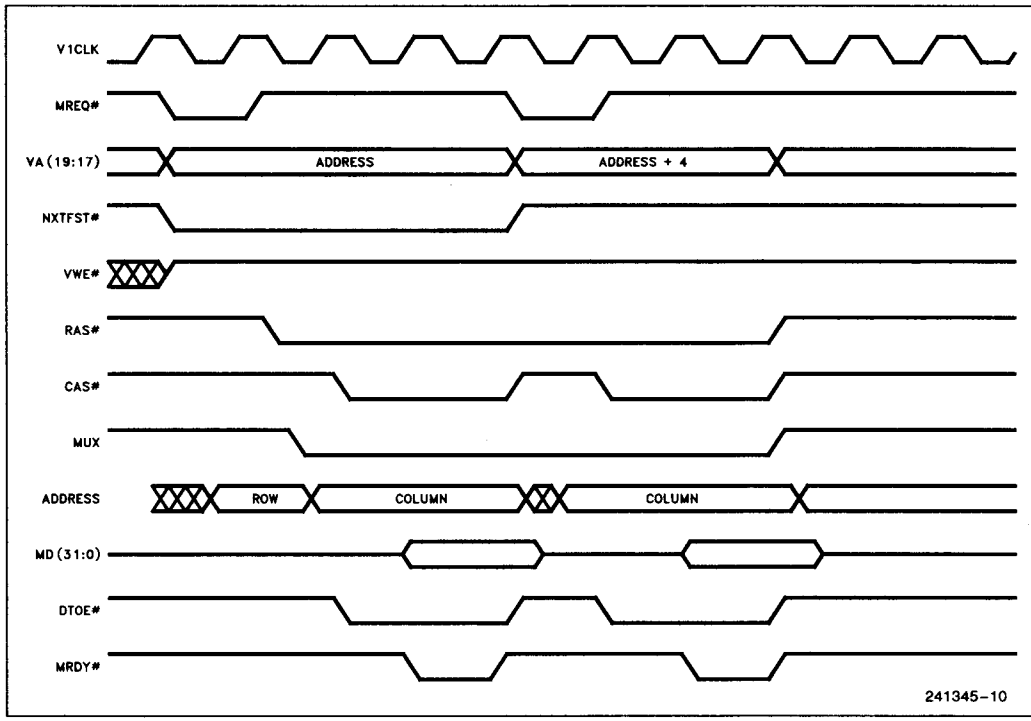


Figure 3-4. NXTFST Dual Page-Mode Read Cycle

A BUSFAST read cycle is shown in Figure 3-5. Since this cycle is initiated by a DVI Bus Device, the bus mastership is first acquired through a request process (not shown) which results in the BUSEN# signal being asserted and enabling the output drivers during the read cycle. The GAVALEN low transition causes the least significant 24-bit address on the MD(31:0) Bus to be latched and MD31 = 1 causes the BUSFAST cycle to be generated by the gate array. The cycle proceeds identically to the NXTFST cycle with the exception that (1) the MSTRB# signal is used by the bus master to indicate that the read data can be latched and the address incremented and (2) the MRDY# signal is asserted only once at the end of the dual cycle to indicate to the PB that the cycle is complete.

Transfer Cycle

Transfer cycles are used to load the VRAM serial shift register with data for DB. DB requests the transfer of different types of data but has no knowledge of memory addresses or pointers. These pointers are maintained by PB, which schedules a transfer cycle upon receipt of any of several transfer codes over the VBUS. Since there is no mechanism for DB to get feedback as to when the transfer is performed, it waits a programmable period of time and assumes it is complete. In order to minimize this period, the PB makes transfers the highest priority operation it can perform on the memory system.

A transfer cycle appears similar to a single read cycle except that TROE# is asserted before the falling edge of RAS# as shown in Figure 3-6. Some programmable time after the end of the memory cycle, DB begins to deliver serial clocks to the VRAMs and the data comes out of the serial port one 32-bit word at a time. The serial port being addressed is enabled by one of the SE#(3:0) outputs, which are decoded by the gate array in the same manner as the RAS# signals.

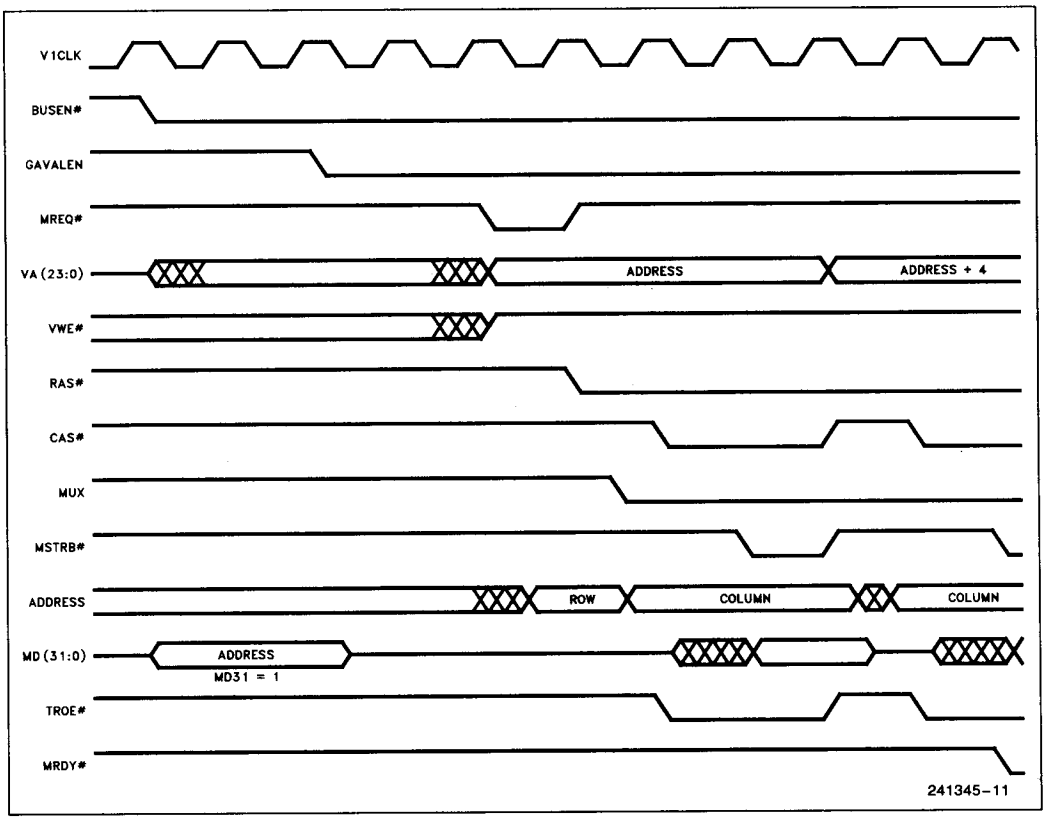


Figure 3-5. BUSFAST Dual Page-Mode Read Cycle

Refresh Cycle

Refresh cycles are initiated by DB and executed by PB. DB issues a refresh request over the VBUS to PB which generates a programmable number (up to 15) of refresh cycles for each DB request. These cycles are distinguished by RFRSH# being asserted simultaneously with MREQ# as shown in Figure 3-7. VSCGA generates a Refresh cycle by asserting CAS# before RAS#. All banks of VRAM go active regardless of the state of the address bus.

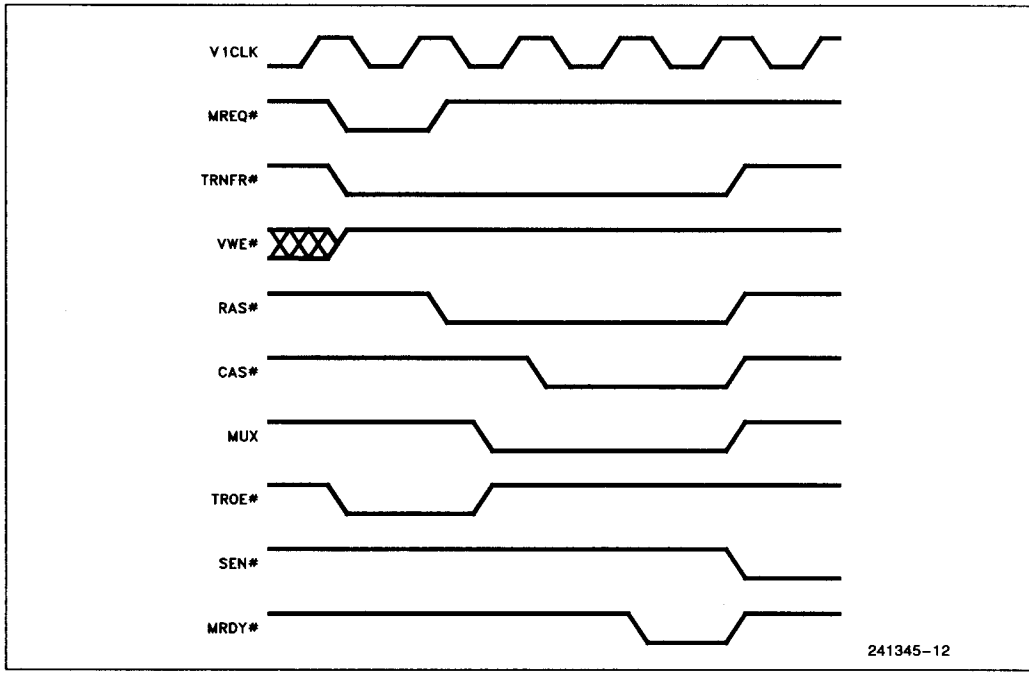


Figure 3-6. Transfer Cycle

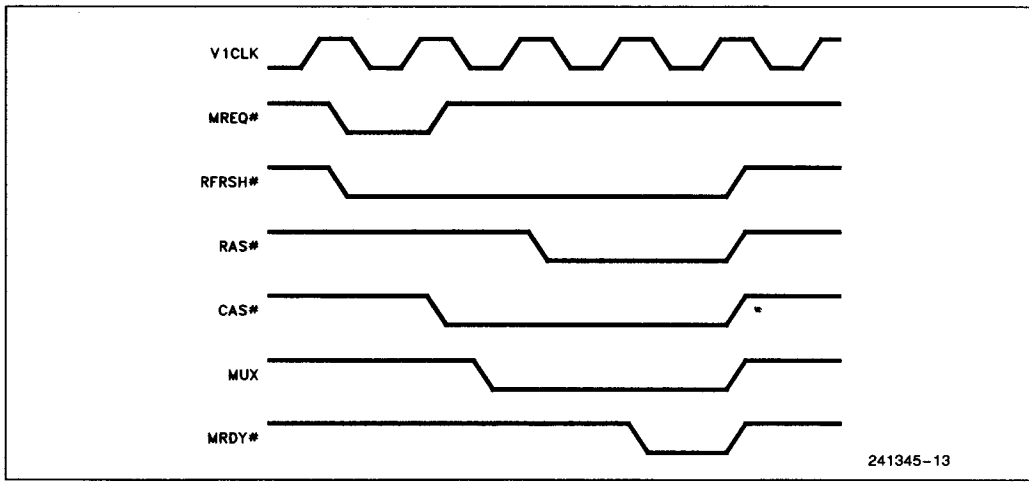


Figure 3-7. Refresh Cycle

Register Cycles

Each of the DVI Bus Devices contains one or more addressable registers used for control and monitoring of the Device's functions. These registers are all in the range from F00000H to FFFFFFH. Whenever any device in that range is accessed, the VSCGA generates a register cycle as shown in Figure 3-8 for a read cycle. The acquisition of bus mastership for non-PB-accesses is omitted from the figure. Once the gate array decodes the four most significant address bits, it asserts the DSTRB# pulse used by the other DVI Bus Device address decoders. The length of the strobe is programmable.

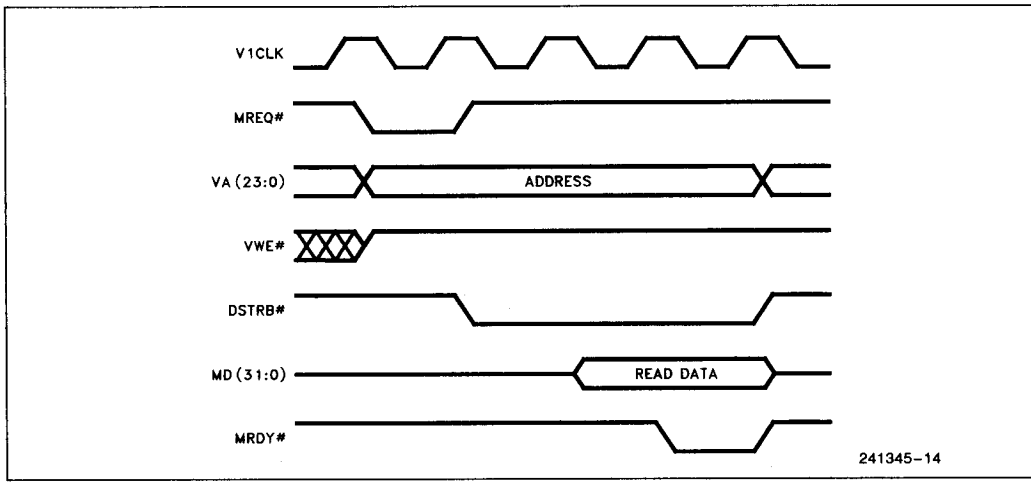


Figure 3-8. Register Read Cycle

3.2.2 CAPTURE BURST

When a Capture Module is ready to transfer Y or VU data into a section of VRAM, it sets the YVUSEL signal to the appropriate level (0 for Y, 1 for VU) and asserts the BRSTREQ# line to request the use of the DVI Bus as shown in Figure 3-8. The VSCGA passes the request on by asserting the CHANREQ# output and receives a grant of its request when BUSEN# and VSCSEL# are simultaneously asserted by the Host Interface Gate Array. VSCGA, in turn, asserts BRSTACK#, which is monitored by the Capture Module, indicating that the MD(31:0) Bus may be driven with the captured data. DCLK, which is a free-running clock at half the V1CLK frequency when captured data is not being transferred, is phased to the incoming data and used as a handshaking signal to indicate when new data may be placed on the Bus. When data is being transferred DCLK goes to a 1 for one V1CLK cycle and then goes to a 0 for a programmed length of time. The page mode access continues until the Capture Module completes its transfer, as shown in Figure 3-8, or until the DB requests a transfer cycle by setting VBUS3 to a 0. This is shown in Figure 3-9. In this latter case note that the BRSTREQ# stays asserted even though the BRSTACK# is terminated. After the transfer cycle completes the request will still be asserted and the process of acquiring the DVI bus will begin again.

During the transfer of captured data the BE#(3:0) lines are ignored. All CAS strobes are generated unless inhibited by the Input Mask (if selected).

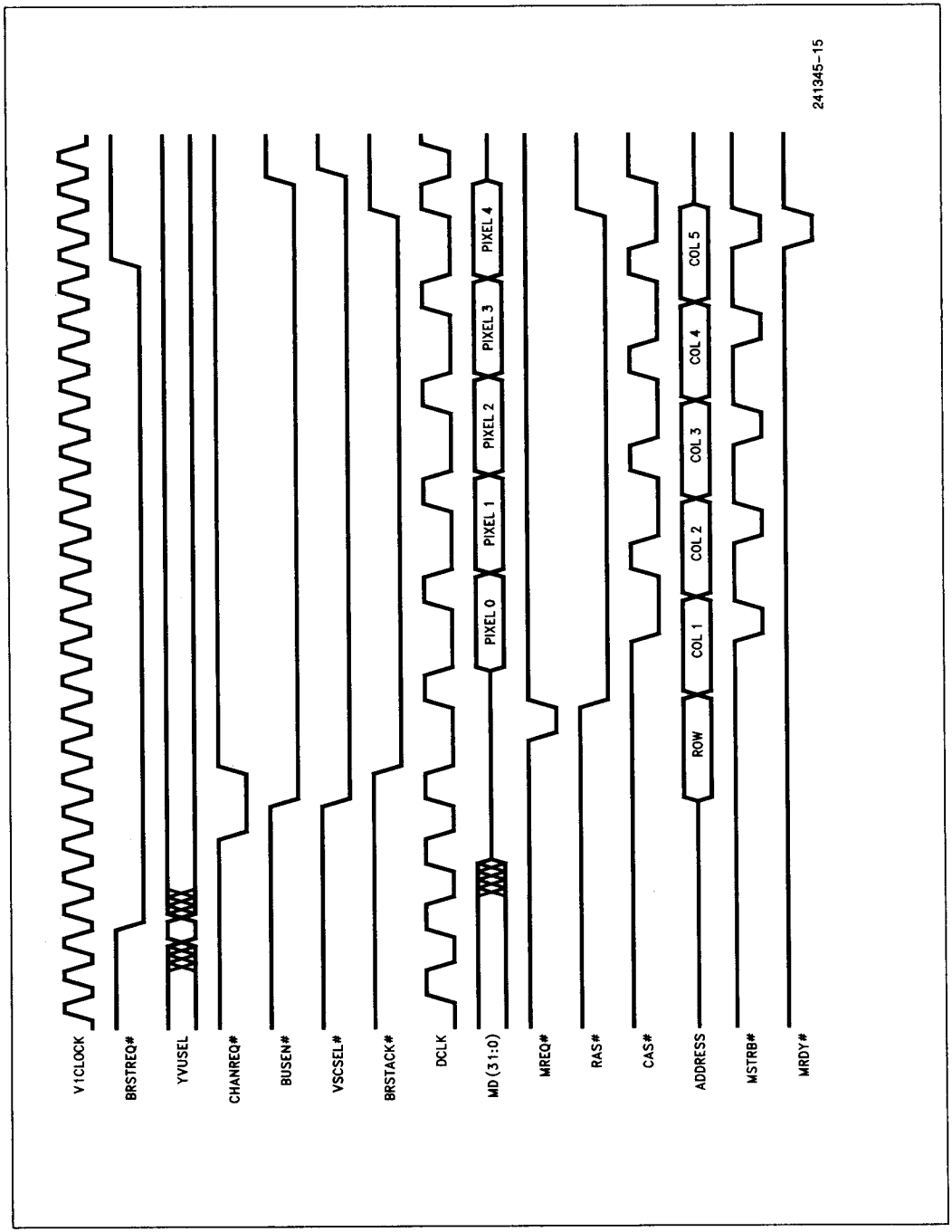


Figure 3-8. Capture Burst (Request Terminated)

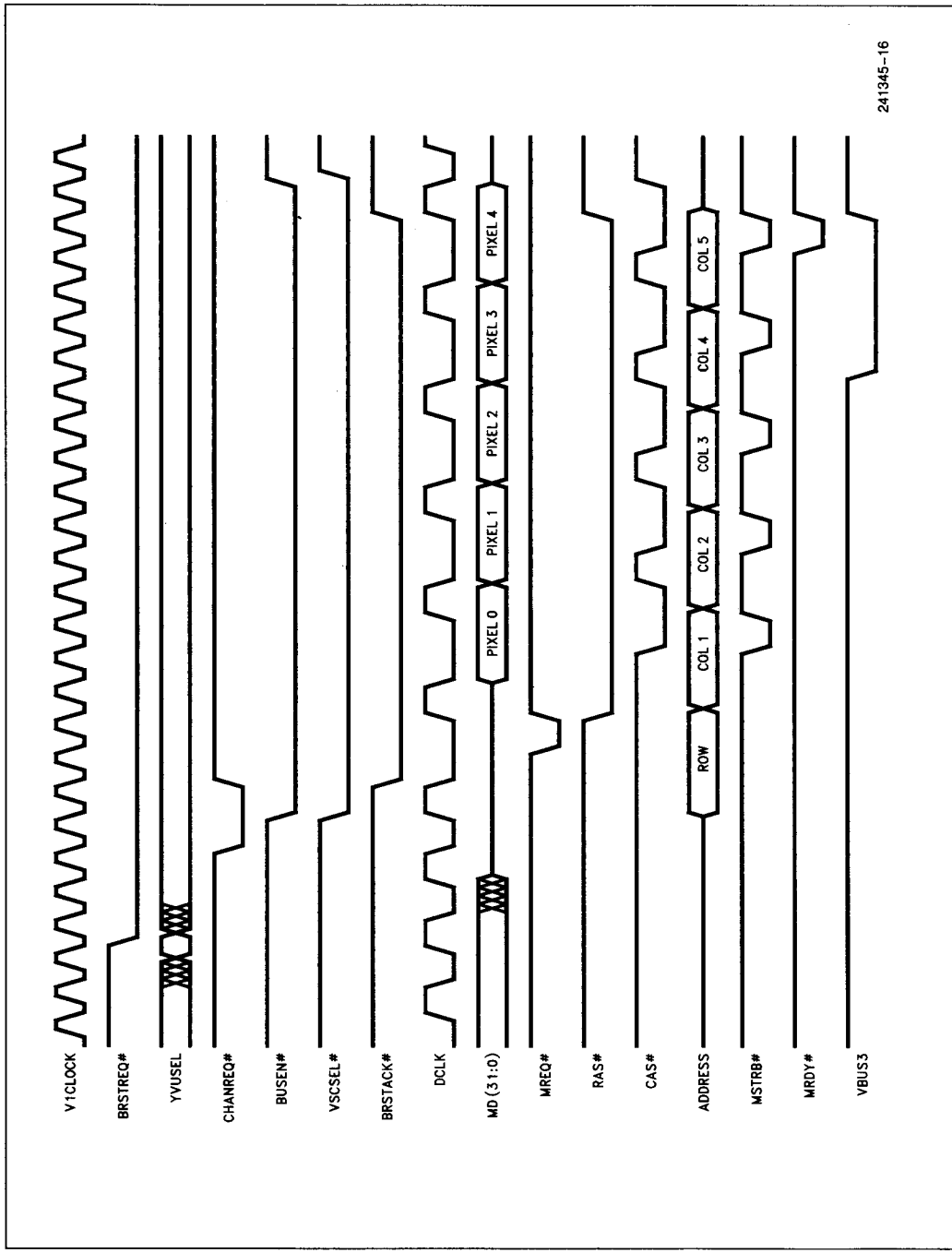


Figure 3-9. Capture Burst (Transfer Terminated)

3.2.3 MASKING

During the capture of data there are two ways of masking the data written to VRAM. The first, input masking, entails selectively preventing rectangular areas of pixels (as small as 4 x 2 for Y data) from being written to memory by inhibiting CAS strobes. The decision to enable the strobe is based upon a reduced resolution, single-bit memory map. When input masking is selected, this map is periodically automatically loaded at the beginning of a captured horizontal video line into the Mask RAM. The second type of masking is write-per-bit masking, which uses an eight-bit value stored in the Memory Control Register to selectively inhibit bits in every byte that is written to VRAM. When this mode is enabled, VSCGA places the mask data (replicated four times) on the DVI Data Bus and asserts the WE# line before RAS# is asserted for the capture burst. The VRAM chips will continue to mask data writes only during that burst. The procedure must be repeated each time RAS is asserted to continue the masking.

3.2.4 CAPTURE MODULE TIMING SIGNALS

In addition to the signals already discussed, there are several lines linking the Capture Module with VSCGA which support the capture operation: (1) HTIM is a pulse driven by the Capture Module for each horizontal line. It is timed to occur just before the active data. (2) EVEN/ODD is a signal driven by the Capture Module to indicate which field is currently being captured. A 0 indicates an even field while a 1 indicates an odd field. The EVEN/ODD transition is expected to occur between HTIM pulses. (3) REGSEL# is an output signal to the Capture Module whose assertion indicates that a register access operation is being performed. It is the logical "AND" of DSTRB and (address = FC0020H). Data written to the Capture Module should be latched from the MD(31:0) Bus on the trailing edge of REGSEL#. Data read from the Module should be enabled on the leading edge of REGSEL# for as long as REGSEL# is active. (4) CS2FLG is an input handshaking signal indicating that the Capture Module has register data available to be read or that register write data has been accepted.

3.3 SCSI Interface

3.3.1 SCSI PROTOCOL

In the process of VSCGA as the Initiator commanding a CD-ROM Target to perform its various functions, the SCSI Bus goes through several states. A simple state diagram encompassing the sequences for Data In operations encountered in a Single-Initiator system is shown in Figure 3-10. In the figure, I(nitiator), and T(arget) followed by a colon and a signal name indicate the assertion or negation of a signal and its source. Signal sequences within dotted boxes may be repeated in their entirety. Arrows within states indicate the direction of data flow. The following paragraphs describe how the phases are traversed during normal CD-ROM operation:

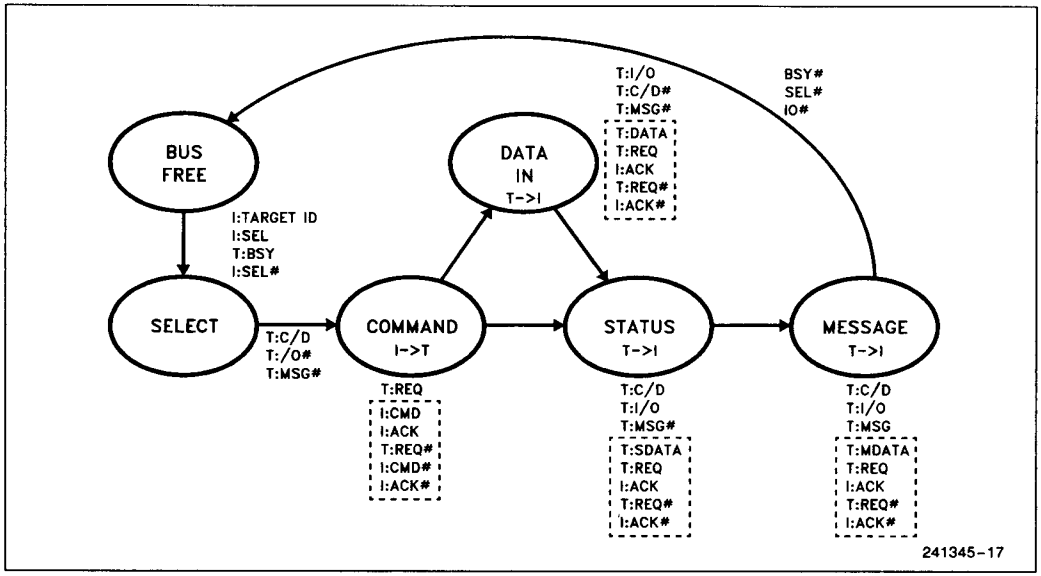


Figure 3-10. SCSI Bus Phase Diagram

BUS FREE PHASE. In the diagram the system starts off in the BUS FREE state with none of the control signals asserted.

SELECTION PHASE. Because this is a Single-Initiator system, there is no Arbitration Phase, and the Initiator can go directly into the Selection Phase. The ID of the Target Device (one of eight possible single bit selections) is placed onto the SCSI Bus. Next, SEL is asserted to indicate that the Target ID is valid. The selected Target then asserts BSY after which time the Initiator releases SEL and the selection process is complete.

COMMAND PHASE. Without further direction, the Target now asserts C/D and negates MSG and I/O to put the SCSI Bus into the Command Phase. It then asserts the REQ line to receive command data. This is placed on the Data Bus by the Initiator, followed by the assertion of ACK. The Target receives ACK, reads the command data and releases REQ. In response the Initiator releases ACK and may place new command data on the Bus. The target may continue to request command bytes by asserting REQ again. The number of command bytes to be transferred is contained in the first command byte.

DATA IN PHASE. Depending on the nature of the command, the SCSI Bus may enter either the DATA IN or the STATUS PHASE. If the DATA IN PHASE is selected, the Target asserts I/O and negates C/D and MSG. It then places retrieved data on the Data Bus and asserts REQ. The Initiator reads the Data Bus and then asserts ACK. When the Target detects ACK it negates REQ and waits for the Initiator to negate ACK. The Target may then continue to provide data by asserting REQ again. The Initiator "knows" how many bytes of data to expect by virtue of the original command.

STATUS PHASE. This phase is entered either after the DATA IN PHASE or directly from the COMMAND PHASE depending on the command. In either case the Target asserts C/D and I/O and negates MSG. The Target then places Status Data on the Data Bus and asserts REQ. The process continues as in the DATA IN PHASE.

MESSAGE PHASE. This phase follows the STATUS PHASE and typically indicates that the command is complete. The Target asserts C/D, I/O and MSG. It places the Message Data on the Data Bus and asserts REQ. The process continues as in the DATA

IN PHASE. Afterwards the Initiator and Target release all lines and the SCSI Bus returns to the BUS FREE PHASE.

3.3.2 SCSI BUS DRIVERS

There are thirteen signal lines that must be driven by the VSCGA on the SCSI Bus. Each requires a drive capability of 48 mA. In order to achieve that current capability output drivers in the chip are paired. The pin names of the two drivers are the same except that one has an "A" suffix.

4.0 PROGRAMMING INFORMATION

4.1 VRAM and Capture

This section describes the details of the ten VRAM and Capture registers addressable from the DVI Bus.

4.1.1 Y SHADOW REGISTERS (Y_EVEN, Y_ODD)

There are two 32-bit Y Shadow Registers, one which is used during even fields and the other during odd fields. Figure 4-1 identifies each bit of these registers as well as its accessibility. These registers are used during all modes of capture and are pointers into VRAM for the location to start storing the captured Y, R, G or B data.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
YA15	YA14	YA13	YA12	YA11	YA10	YA9	YA8	YA7	YA6	YA5	YA4	YA3	YA2	YA1	YA0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
LSB	TRAN	0	0	OFF3	OFF2	OFF1	OFF0	YA23	YA22	YA21	YA20	YA19	YA18	YA17	YA16
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Figure 4-1. Video Capture Y Shadow Registers

YA23..YA0 - Y Address Pointer (Bits 23:0)

These 24 bits represent the starting location for storing captured Y pixels stored in VRAM. Once this value is loaded into the Working Register it becomes the current Y address pointer into VRAM for that field and is incremented by one for each pixel and by the horizontal line length (next higher power of two) for each received HTIM pulse preceded by active Y data.

OFF3..OFF0 - Y OFFSET (Bits 27:24)

These four bits determine where in the YA(23:0) pointer that the pixel counter ends and the least significant bit of the horizontal line counter begins. Table 4-1 indicates where the LSB of the line counter is located for all values of OFF(3:0). Note that for values of OFF greater than 9 there is no change in functionality.

Table 4-1. LSB of Line Counter vs Offset

Offset	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
LSB	YA3	YA4	YA5	YA6	YA7	YA8	YA9	YA10	YA11	YA12	YA12	YA12	YA12	YA12	YA12	YA12

LSB Mode (Bit 30)

The LSB bit allows the pixel counter to either be initialized to a value or cleared to zero when it is loaded into the Pointer Counter. If this bit is set to 0, bits of lesser significance than the LSB of the line counter are set to a zero at the beginning of each line regardless of the pixel count in the Working or Shadow Register. When this bit is set to a 1, the register pixel count will be loaded into Pointer Counter at that time. This mode is useful for offsetting images or preserving that offset when the Capture Module is producing cropped data.

TRAN Mode (Bit 31)

The TRAN bit, when set to a 1, allows the Y Shadow Register to be updated at the beginning of each line. This feature is mainly for diagnostic purposes but could be used to allow the programmer to monitor the capture progress within a field. Since neither the Working Registers nor the Pointer Counter are addressable the only way to accomplish this is to read a continuously updated Shadow Register. The only difficulty is that the read may coincide with a register update and the resulting data may be erroneous. This can be overcome with multiple software reads or with a simple external hardware fix which prevents updating during a read.

4.1.2 VU Shadow Registers (VU_EVEN, VU_ODD)

There are two 32-bit VU Shadow Registers, one which is used during even fields and the other during odd fields. Figure 4-2 identifies each bit of these registers as well as its accessibility. These registers are used during YVU9, YVU10 and YVU12 capture modes and are pointers into VRAM for the location to start storing the captured V and U data. These registers are defined exactly the same as the Y Shadow Registers.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
VUA15	VUA14	VUA13	VUA12	VUA11	VUA10	VUA9	VUA8	VUA7	VUA6	VUA5	VUA4	VUA3	VUA2	VUA1	VUA0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
LSB	TRAN	1	0	OFF3	OFF2	OFF1	OFF0	VUA23	VUA22	VUA21	VUA20	VUA19	VUA18	VUA17	VUA16
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Figure 4-2. Video Capture VU Shadow Registers

4.1.3 Mask Shadow Registers (VU_EVEN, VU_ODD)

There are two 32-bit Mask Shadow Registers, one which is used during even fields and the other during odd fields. Figure 4-3 identifies each bit of these registers as well as its accessibility. These registers are used during YVU9, YVU10 and YVU12 capture modes and are pointers into VRAM for the location of the Input Mask bit Map. These registers are defined exactly the same as the Y and VU Shadow Registers except for bits 28 and 29 which control the phase of the line counter controlling the mask fetch.

MOD1, MOD0 (Bits 29:28)

Each 1, 2 or 4 lines, depending on the VU subsampling mode, mask data is fetched from VRAM and loaded into the Mask RAM. These bits control the starting count for the ÷4 counter which controls that process. This feature gives the programmer the ability to vertically phase the Input Mask with the captured image without modifying the VRAM mask data. The relationship between the MOD(1:0) field and the starting line is shown below:

Starting Line	MOD1	MOD0
0	0	0
1	1	1
2	1	0
3	0	1

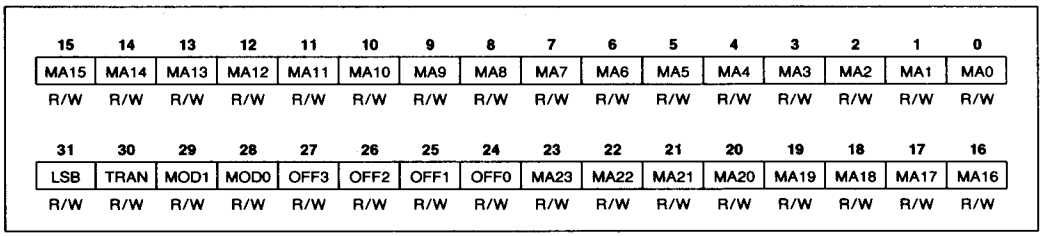


Figure 4-3. Video Capture Input Mask Shadow Registers

4.1.4 V-U INTERLEAVE REGISTER (VU_PITCH)

This 16-bit register is used in YVU9, YVU10 and YVU12 modes of capture to separate the intertwined V and U data into adjacent areas of VRAM. Figure 4-4 identifies each bit of this register as well as its accessibility.

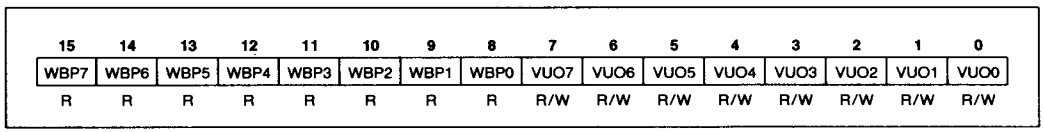


Figure 4-4. VU Interleave Register

VUO7..VUO0 - VU Offset (Bits 7:0)

When the Capture Module sends bursts of captured chroma data to VRAM, the repeated eight-byte format consists of four bytes of V followed by four bytes of U data. VSCGA keeps track of the incoming data format and allows the contents of the VU Offset field to be added only to the U data addresses. Before the addition, the register contents are multiplied by eight. Since the field is one byte wide, a maximum offset of 2048 bytes is achievable. This is not sufficient to totally separate the two components but is enough to allow them to be placed side-by-side as shown in Figure 2-2.

WPB7..WPB0 - Write-per-Bit (Bits 15:8)

This read-only field is used for diagnostic purposes and contains the Write-per-Bit field information from the Memory Command Register.

4.1.5 CAPTURE COMMAND AND STATUS REGISTER (CAP_CST)

This 16-bit register is used to set up the parameters for the video capture operation. Figure 4-5 identifies each bit of this register as well as its accessibility.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
INT	RDY	V-G	UPM	VUD	HTIM	ORX	ORM	ORVU	ORY	OR	OME	4x2#	IMD	EOIE	E/O#
R/W	R	R	R/W	R/W	R	R	R	R/W	R	R/W	R/W	R/W	R/W	R/W	R

Figure 4-5. Video Capture Command and Status Register

INT - Capture Interrupt (Bit 15)

When this bit is a 1, the gate array is asserting a Capture Interrupt because of an EVEN/ODD field bit transition (either direction). For this to occur, the Even/Odd Interrupt Enable (EOIE) must be enabled. Writing a 1 to this location will reset the bit to a 0 but will not clear the interrupt. Reading the SCSI Status Register (F8000CH) will reset the bit and clear the interrupt.

RDY - Capture Module Ready (Bit 14)

This read-only bit reflects the status of CS2FLAG pin which, in turn, reflects the status of the Capture Module Command and Status Register. When this bit is a 1, it indicates either that write data has been accepted or that read data is valid.

V-G - Video Gate (Bit 13)

When this bit is a 1, the gate array is in the process of processing a burst of data from the Capture Module. This read-only bit is for diagnostic purposes.

UPM - Update Pointer Mode (Bit 12)

When this bit is set to a 1, the Shadow Registers will be updated from the Working Registers on every occurrence of the HTIM pulse. This is equivalent to setting the TRAN bit to a 1 on all the Shadow Registers. This bit becomes effective on the following transition of the EVEN/ODD signal. When this bit is set to a 0, the Shadow Registers will be updated from VRAM once per field (even or odd each time).

VUD - VU Data Deinterleave (Bit 11)

When this bit is set to a 1 the U and V data bursts will be deinterleaved as they are written into VRAM. This bit becomes effective on the following transition of the EVEN/ODD signal.

HTIM - Horizontal Timing (Bit 10)

This read-only bit indicates the status of the HTIM signal on the Video Capture Bus.

ORX - Overrun X (Bit 9)

This read-only bit is set when an HTIM pulse is asserted before the bursts from previous video line have been written to VRAM and the capture process has been interrupted to perform a TRANSFER cycle. Setting the OR bit to a 1 will clear this condition.

ORM - Overrun Mask (Bit 8)

This read-only bit is set when an overrun occurs during a transfer of mask data. This probably indicates a serious problem since it is the first data to be transferred after an HTIM pulse. Setting the OR bit to a 1 will clear this condition.

ORY - Overrun Y (Bit 7)

This read-only bit is set when an overrun occurs during a transfer of Y data. Setting the OR bit to a 1 will clear this condition.

ORVU - Overrun VU (Bit 6)

This read-only bit is set when an overrun occurs during a transfer of VU data. Setting the OR bit to a 1 will clear this condition.

OR - Overrun (Bit 5)

This bit is set when an HTIM pulse is asserted before the bursts from previous video line have been written to VRAM. At least one of the preceding four bits must be set as well. Setting this bit to a 1 will clear this condition and the preceding four bits as well.

OME - Output Mask Enable (Bit 4)

Setting this bit to a one enables the Write-per-Bit capture feature of the gate array. This bit becomes effective on the following transition of the EVEN/ODD signal.

4x2# - 4 x 4 vs. 4 x 2 Subsampled Chroma (Bit 3)

When this bit is set to a 1, each bit in the Input Mask represents a 4 x 4 rectangular area of pixels. When this bit is set to a 0 each bit in the Input Mask represents a 4 x 2 rectangular area of pixels. For this bit to have meaning, the following IMD bit must be set to a 0. This bit becomes effective on the following transition of the EVEN/ODD signal.

IMD - Input Mask Disable (Bit 2)

When this bit is set to a 0 the Input Mask Mode is enabled. This means that prefetched mask data from VRAM loaded into the Mask Ram will determine which bytes, if any, of a capture burst will be written into VRAM. This bit becomes effective on the following transition of the EVEN/ODD signal.

EOIE - Even/Odd Interrupt Enable (Bit 1)

When this bit is set to a 1, VSCGA will create a Capture Interrupt for every transition of the EVEN/ODD input signal. This bit is effective immediately.

E/O# - Even/Odd# (Bit 0)

This read-only bit indicates the state of the EVEN/ODD signal input pin on the gate array. It is a 1 during even fields and a 0 during odd fields.

4.1.6 MEMORY COMMAND REGISTER (MEM_CMD)

This write-only 32-bit register determines the timing parameters to allow for a wide variety of combinations of system clock and memory speeds. It also stores mask information for Write-per-Bit operations. Figure 4-6 identifies each bit of this register as well as its accessibility.

WPB7..WPB0 - Write-per-Bit (Bits 23:16)

This field of data contains the mask value that is loaded into VRAM during a Write-per-Bit capture cycle when the Output Mask Mode is enabled. A value of 1 in any bit position allows that bit to be written; a 0 prevents it. Typically, the value is set to FE to allow the PB to distinguish between video and graphics data in its "Alpha Channel" mode of operation.

4MEG# - 1 Mb vs. 4 Mb VRAMS (Bit 12)

When this bit is set to a 0 the controller decodes addresses for 4 Megabit VRAMs and addresses a total of 15 Megabytes of memory. The address ranges for which the four RAS# lines are decoded is shown in Table 4-2. The top Megabyte of the address space is reserved for DVI Bus Devices and is not decoded for VRAM.

Table 4-2. 4 Megabit VRAM RAS# Decodes

Address Range	RAS0#	RAS1#	RAS2#	RAS3#
0–3FFFFFH	Yes	No	No	No
400000–7FFFFFH	No	Yes	No	No
800000–BFFFFFH	No	No	Yes	No
C00000–EFFFFFH	No	No	No	Yes

When this bit is set to a 1 the controller decodes addresses for 1 Megabit VRAMs and addresses a total of 4 Megabytes of memory. The address ranges for which the four RAS# lines are decoded is shown in Table 4-3. The RAS# lines are not fully decoded in this mode and are asserted for higher address spaces as well but the CAS# lines are inhibited for addresses above 400000H in this mode so that no memory operations will take place there.

Table 4-3. 1 Megabit VRAM RAS# Decodes

Address Range	RAS0#	RAS1#	RAS2#	RAS3#
0–0FFFFFH	Yes	No	No	No
100000–1FFFFFN	No	Yes	No	No
200000–2FFFFFH	No	No	Yes	No
300000–3FFFFFH	No	No	No	Yes

DWL1, DWL0 - DSTRB# Write Length (Bits 11:10)

This field determines the number of cycles that DSTRB# is asserted during a Register Write Cycle. This is chosen as a function of the minimum write pulse widths required by the DVI Bus Devices. In this mode DSTRB# is asserted for (DRL + 1) × 2 V1CLK periods.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	4MEG#	DWL1	DWL0	DRL1	DRL0	COD	DOD	XP	ROD	WL1	WL0	RL1	RL0
W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0	0	0	0	0	0	0	0	WPB7	WPB6	WPB5	WPB4	WPB3	WPB2	WPB1	WPB0
W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W

Figure 4-6. Memory Command Register

DRL1, DRL0 - DSTRB# Read Length (Bits 9:8)

This field determines the number of cycles that DSTRB# is asserted during a Register Read Cycle. It is chosen as a function of the maximum read access time exhibited by any of the DVI Bus Devices. In this mode DSTRB# is asserted for (DRL + I) × 2 + 1 V1CLK periods.

COD - CAS# Onset Delay (Bit 7)

When this bit is set to a 1, it adds a delay cycle to the leading edge of all CAS# cycles. This allows for extra Column Address or Write Data setup time. This bit has no effect on Refresh Cycles.

DOD - DSTRB# Onset Delay (Bit 6)

When this bit is set to a 1, it adds a delay cycle to the leading edge of all DSTRB# cycles. This allows for extra address or control signal setup time.

XP - Extra Precharge (Bit 5)

This bit adds an extra precharge wait cycle after RAS# is unasserted. When this bit is set to a 0, there are two V1CLK cycles from the time that RAS# is unasserted until the time it is reasserted. When this bit is set to a 1, that number is extended to three.

ROD - RAS# Onset Delay (Bit 4)

When this bit is set to a 1, it adds a delay cycle to the leading edge of RAS# cycles only when the normal delay cycle between single VRAM read-write cycles is not inserted. This allows for extra Row Address setup time from the assertion of MREQ#. This bit has no effect on Refresh Cycles.

WL1 ,WL0 - Memory Write Operation Length (Bits 3:2)

This field determines the number of V1CLK cycles that RAS# and CAS# are simultaneously active during a VRAM Write Cycle. Its value is chosen as a function of the minimum RAS#, CAS# or WE# pulse width required by VRAM. The relationship between the WL(1:0) field and the number of V1CLK cycles is shown below:

# V1CLK Cycles	WL1	WL0
1	0	0
2	0	1
3	1	0
4	1	1

RL1, RL0 - Memory Write Operation Length (Bits 1:0)

This field determines the number of V1CLK cycles that RAS# and CAS# are simultaneously active during a VRAM Read Cycle. Its value is chosen as a function of the maximum RAS# or CAS# access time. The relationship between the RL(1:0) field and the number of V1CLK cycles is shown below:

# V1CLK Cycles	RL1	RL0
1	0	0
2	0	1
3	1	0
4	1	1

4.1.7 CAPTURE MODULE COMMAND AND STATUS REGISTER (CM_CST)

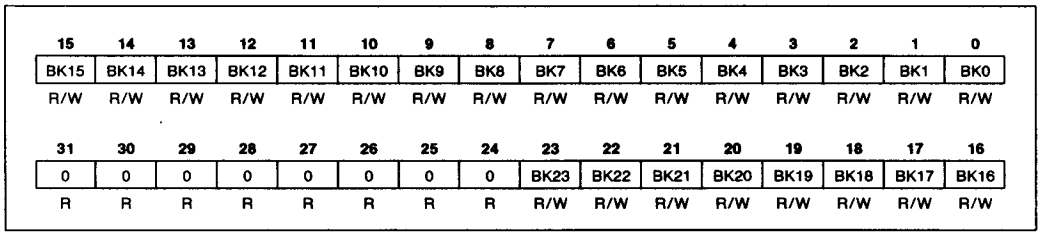
This 16-bit read-write register is decoded by the Capture Module logic. For information as to how to interpret this field, refer to the Capture Module Microcontroller Software Specification.

4.2 SCSI Interface

This section describes the details of the nine SCSI registers addressable from the DVI Bus.

4.2.1 CHAIN BLOCK ADDRESS REGISTER

This 32-bit register contains a 24-bit pointer to the next Chain Block in VRAM. It is initially loaded using a DVI Bus Register access. Thereafter, whenever a Chain Block is fetched from memory, this register is incremented by four after each read cycle so that its pointer is always prepared for the next access. Figure 4-7 identifies each bit of this register as well as its accessibility.



15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BK15	BK14	BK13	BK12	BK11	BK10	BK9	BK8	BK7	BK6	BK5	BK4	BK3	BK2	BK1	BK0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

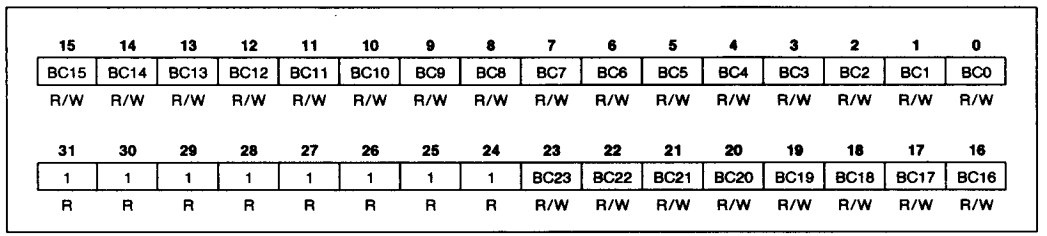
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0	0	0	0	0	0	0	0	BK23	BK22	BK21	BK20	BK19	BK18	BK17	BK16
R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Figure 4-7. Chain Block Address Register

4.2.2 BYTE COUNT REGISTER

This 32-bit register contains a 24-bit two's complement number indicating how many bytes are left to be transferred in the current block. The register is initially loaded during a Chain Block fetch. Each time data is read from or written to memory as part of a SCSI DMA cycle, the Byte Count Register is incremented by four to keep it current. The register can also be read or modified using a DVI Bus Register access.

The least significant bit of this register must always be written as a 0 so that the block length is a multiple of two. Figure 4-8 identifies each bit of this register as well as its accessibility.



15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BC15	BC14	BC13	BC12	BC11	BC10	BC9	BC8	BC7	BC6	BC5	BC4	BC3	BC2	BC1	BC0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
1	1	1	1	1	1	1	1	BC23	BC22	BC21	BC20	BC19	BC18	BC17	BC16
R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Figure 4-8. Byte Count Register

4.2.3 BYTE ADDRESS REGISTER

This 32-bit register contains a 24-bit address indicating how many bytes are left to be transferred in the current block. The register is initially loaded during a Chain Block fetch. Each time data is read from or written to memory as part of a SCSI DMA cycle, the Byte Count Register is incremented by four to keep it current. The register can also be read or modified using a DVI Bus Register access. The least significant bit of this register must always be written as a 0 so that the block length is a multiple of two. Figure 4-9 identifies each bit of this register as well as its accessibility.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BA15	BA14	BA13	BA12	BA11	BA10	BA9	BA8	BA7	BA6	BA5	BA4	BA3	BA2	BA1	BA0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0	0	0	0	0	0	0	0	BA23	BA22	BA21	BA20	BA19	BA18	BA17	BA16
R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Figure 4-9. Byte Address Register

4.2.4 DMA Control Register

This 16-bit register provides control information for the CD-ROM DMA Controller. The least significant byte is copied from the corresponding VRAM location during the fetch of the Chain Block. The two most significant bits are written using DVI Bus Register writes. Figure 4-10 identifies each bit of this register as well as its accessibility.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CDE	FNB	0	0	0	0	0	0	SD4	SD3	SD2	SD1	SD0	LB	IOE	NULL
R/W	R/W	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

CDE - CD-ROM DMA Controller Enable (Bit 15)

This bit is the enable for the CD-ROM DMA which allows requests to be generated on the DVI Bus. The bit is reset automatically after the last data block is complete (one in which the LB bit is set).

FNB - Fetch Next Block (Bit 14)

This bit is used to start the CD-ROM DMA Chain Block sequence. Initially, a VRAM address is loaded into the Chain Block Address Register. Then, when this bit is set to a 1, the Chain Block starting at that location will be stored in VSCGA's registers, and updated as the sequence progresses. This bit is set to a 0 when the first word of the Chain Block is fetched.

SD4..SD0 - Software Definable Bits (Bits 7:3)

These bits can be read from this register and may contain information specific to the current Chain Block in use (e.g. Chain Block ID).

LB - Last Block (Bit 2)

When this bit is set to a 1, the CD-ROM DMA Channel will terminate at the end of the current block. CD-ROM DMA data transfers will not continue until re-enabled by software.

IOE - Interrupt on End of Block (Bit 1)

When this bit is set to a 1 a CD-ROM DMA Interrupt will be generated when the last word of the current block is transferred.

NULL - Null Transfer (Bit 1)

When this bit is set to a 1, it disables the data transfer for the current block. Other than not writing any data to VRAM, the DMA Channel will behave normally. Specifically, it will continue to request DVI Bus cycles. This feature can be used to strip off Pad Characters from the CD-ROM data stream.

4.2.5 COMMAND REGISTER

This 16-bit register contains the signals used to control the SCSI Bus, and the manner in which the gate array responds to SCSI Bus errors. Figure 4-11 identifies each bit of this register as well as its accessibility.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ELOB	ENPI	0	RGA	ENBC	EMSI	ENPR	ACK	RST	ATN	EWGR	SEL	EPMI	PMB2	PNB1	PMB0
R/W	R/W	R	R/W	R/W	R/W	R/W	R/W	W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Figure 4-11. Command Register

ELOB - Enable Loss Of Busy Interrupt (Bit 15)

When this bit is set to a 1, VSCGA will generate an interrupt if the connected Target prematurely enters the Bus Free Phase.

ENPI - Enable Parity Interrupts (Bit 14)

When this bit is set to a 1 and the ENPR bit is set, an interrupt will be generated upon the detection of a parity error during a Data In transfer over the SCSI Bus.

RGA - Reset Gate Array (Bit 12)

When this unlatched bit is set to a 1, all the internal gate array CD-ROM logic is reset.

ENBC - Enable Bus Drive Command (Bit 11)

When this bit is set to a 1, VSCGA will be enabled to drive the SCSI Bus. When this bit is set to a 0, the SCSI Bus outputs will go to a high impedance state.

EMSI - Enable Message and Status Interrupts (Bit 10)

When this bit is set to a 1 and ENPR is asserted, an interrupt will be generated upon the detection of a parity error during a Message In or Status transfer over the SCSI Bus.

ENPR - Enable Parity Checking (Bit 9)

When this bit is set to a 1 the Parity Checker is enabled to examine data transferred from the Target over the SCSI Bus.

Ack - Acknowledge (Bit 8)

When this bit is set to a 1 and ENBC is asserted, the ACK signal on the SCSI Bus will be asserted. This bit is a handshaking signal used in conjunction with REQ to transfer data bytes between the Initiator and Target.

RST - Reset (Bit 7)

When this bit is set to a 1 the RST signal on the SCSI Bus will be asserted. This signal must be asserted for a minimum of 25 μs.

ATN - Attention (Bit 6)

When this bit is set to a 1, the ATN signal on the SCSI Bus will be asserted. The ATN signal is used to force the Target into the Message Out Phase.

EWGR - Enable Write General Register (Bit 5)

When this bit is set to a 1, the contents of the Write General Register are enabled onto the SCSI Data Bus. This bit is used to select a Target.

SEL - Select (Bit 4)

When this bit is set to a 1 and ENBC is asserted, the SEL signal on the SCSI Bus will be asserted.

EPMI - Enable Phase Match Interrupt (Bit 3)

When this bit is set to a 1, an interrupt is generated whenever the PMB(2:0) bits don't match the respective SCSI Bus signals when REQ is asserted. Upon interrupt, the State Machine will return to its reset state.

PMB2..PMB0 - Phase Match Bits (Bits 2:0)

These three bits are used to compare to the three SCSI bus signals driven by the Target that determine the phase of the SCSI Bus. Bit 0 corresponds to I/O, bit 1 to MSG and bit 2 to C/D. The comparison of these bits to the SCSI signals is performed each time the Target asserts the REQ line, and, if a mismatch occurs with the EPMI bit set to a 1, causes an interrupt.

4.2.6 STATUS REGISTER

This 16-bit read-only register is used to monitor the signals on the SCSI Bus and interrupt sources. Figure 4-12 identifies each bit of this register as well as its accessibility.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CHRQ	CINT	ENSM	IOE	PMI	LOBI	PERR	IDAT	RST	IRQ	REQ	SEL	BSY	C/D	MSG	I/O
R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Figure 4-12. Status Register

CHRQ - DMA Channel Request (Bit 15)

When this bit is set to a 1, it indicates that the CHANREQ# signal is asserted. This is provided for diagnostic purposes.

CINT - Capture Interrupt (Bit 14)

When this bit is set to a 1, it indicates that the Video Capture logic is the source of the interrupt. This bit and the interrupt will be set to a 0 when the upper byte of this register is read.

ENSM - Enable State Machine (Bit 13)

When this bit is set to a 1, it indicates that the State Machine is enabled to execute DMA cycles. This bit is written in the State Register.

IOE - Interrupt on End of Block (Bit 12)

When this bit is set to a 1, it indicates that interrupt was caused by the completion of a Chain Block DMA. This bit and the interrupt will be set to a 0 when the upper byte of this register is read.

PMI - Phase Match Interrupt (Bit 11)

When this bit is set to a 1, it indicates that the Interrupt was caused by the connected Target asserting REQ while being in a different phase than is stored in the Phase Match bits in the Command Register. The PMI bit and the interrupt will be set to a 0 when the upper byte of this register is read.

LOBI - Loss of Busy Interrupt (Bit 10)

When this bit is set to a 1, it indicates that the interrupt was caused by the Target prematurely enters the Bus Free Phase. The LOBI bit and the interrupt will be set to a 0 when the upper byte of this register is read.

PERR - Parity Error Interrupt (Bit 9)

When this bit is set to a 1, it indicates that the interrupt was caused by a parity error. The PERR bit and the interrupt will be set to a 0 when the upper byte of this register is read.

IDAT - Internal Data (Bit 8)

This bit reflects the state of the IDAT bit written in the State Register. When it is set to a 1, it indicates that the internal data generator is enabled.

RST - Reset (Bit 7)

This bit reflects the state of the RST signal on the SCSI Bus. When it is set to a 1, it indicates that the RST signal is asserted.

IRQ - Internal Request (Bit 6)

This bit reflects the state of the IRQ bit written in the State Register. When it is set to a 1, it indicates that the Internal request is enabled.

REQ - Request (Bit 5)

This bit reflects the state of the REQ signal on the SCSI Bus. When it is set to a 1, it indicates that the REQ signal is asserted.

SEL - Select (Bit 4)

This bit reflects the state of the SEL signal on the SCSI Bus. When it is set to a 1, it indicates that the SEL signal is asserted.

BSY - Busy (Bit 3)

This bit reflects the state of the BSY signal on the SCSI Bus. When it is set to a 1, it indicates that the BSY signal is asserted.

C/D - Command/Data (Bit 2)

This bit reflects the state of the C/D signal on the SCSI Bus. When it is set to a 1, it indicates that the C/D signal is asserted.

MSG - Message (Bit 1)

This bit reflects the state of the MSG signal on the SCSI Bus. When it is set to a 1, it indicates that the MSG signal is asserted.

I/O - Input/Output (Bit 0)

This bit reflects the state of the I/O signal on the SCSI Bus. When it is set to a 1, it indicates that the I/O signal is asserted.

4.2.7 READ SCSI DATA REGISTER

This 8-bit read-only register is used to read Status and Message bytes from the Target.

4.2.8 WRITE GENERAL REGISTER

This 8-bit write-only register is used to buffer Command and Message bytes sent to the Target. It is also used to store the Target ID prior to selection. For diagnostic purposes, this register may also be used to send data to the Target via programmed I/O.

4.2.9 STATE REGISTER

This 16-bit read-only register is used to monitor the State Machine which sequences data during DMA transfers. Figure 4-13 identifies each bit of this register as well as its accessibility.

PIRQ - Pending Input Mask Request (Bit 15)

When this read-only bit is set to a 1, it indicates that the Input Mask Request has won the arbitration and is the current pending DMA request. This bit is provided primarily for diagnostic purposes.

PCRQ - Pending Capture Request (Bit 14)

When this read-only bit is set to a 1, it indicates that the Video Capture Request has won the arbitration and is the current pending DMA request. This bit is provided primarily for diagnostic purposes.

PSRQ - Pending SCSI Request (Bit 13)

When this read-only bit is set to a 1, it indicates that the SCSI Request has won the arbitration and is the current pending DMA request. This bit is provided primarily for diagnostic purposes.

PIRQ - Pending Block Request (Bit 12)

When this read-only bit is set to a 1, it indicates that the Chain Block Request has won the arbitration and is the current pending DMA request. This bit is provided primarily for diagnostic purposes.

IMRQ - Input Mask Request (Bit 11)

This read-only bit reflects the state of the internal Input Mask DMA Request signal. It is provided primarily for diagnostic purposes.

CRQ - Capture Request (Bit 10)

This read-only bit reflects the state of the internal Video Capture DMA Request signal. It is provided primarily for diagnostic purposes.

SRQ - SCSI Request (Bit 9)

This read-only bit reflects the state of the internal SCSI DMA Request signal. It is provided primarily for diagnostic purposes.

BRQ - Block Request (Bit 8)

This read-only bit reflects the state of the internal Chain Block DMA Request signal. It is provided primarily for diagnostic purposes.

SB7..SB0 - State Bits (Bits 7:0)

These eight bits are for diagnostic purposes and indicate the state of the State Machine.

ENSM - Enable State Machine (Bit 7)

When this bit is set to a 1, the State Machine is enabled to sequence. This bit should only be enabled for DMA transfers. The State Machine controls the handshaking signals transferring data during Data In and Data Out Phases of the SCSI Bus. It also controls the handshaking signals transferring data to and from VRAM during DMA operations on the DVI Bus. When this bit is set to a 0, the State Machine will hold its present value, allowing the programmer to read its state. The value of this bit can be read from the Status Register.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PIRQ	PCRQ	PSRQ	PBRQ	IMRQ	CRQ	SRQ	BRQ	SB7 ENSM	SB6 IDAT	SB5 IRQ	SB4	SB3	SB2	SB1	SB0
R	R	R	R	R	R	R	R	R/W	R/W	R/W	R	R	R	R	R

Figure 4-13. State Register

IDAT - Internal Data (Bit 6)

When this bit is set to a 1, the SCSI Data In Phase is generated internally. An internal pattern generator is enabled and generates the following sequence: 01H, 02H, 04H, 08H, 10H, 20H, 40H, 80H, 0H. This bit is used in conjunction with IRQ to emulate Data In transfers in a diagnostic mode. Its value can be read in the Status Register.

IRQ - Internal Request (Bit 5)

When this bit is set to a 1, the SCSI Bus signal REQ is generated internally. This bit is used in conjunction with IDAT to emulate Data In transfers in a diagnostic mode. The state of this bit can be read in the Status Register.

5.0 ELECTRICAL SPECIFICATIONS

5.1 DC Characteristics

Table 5-1 contains stress ratings only, and functional operation at the maximums is not guaranteed. Exposure to Maximum Ratings may affect device reliability. Furthermore, although the 82750LV contains protective circuitry to resist damage from static electrical discharge, this device is sensitive to ESD levels above 1000V. Always take precautions to avoid high static voltages or electric fields.

Table 5-1. Maximum Ratings

Condition	Maximum Requirement
Maximum Operating Junction Temperature	100°C
Storage Temperature	−65°C to +150°C
Voltage on Any Pin with Respect to Ground	−0.5V to +7V
Supply Voltage with Respect to V_{SS}	−0.5V to +7V
Input Current Clamp ($V_I < 0$ or $V_I > V_{CC}$)	±20 mA
Output Current Clamp ($V_O < 0$ or $V_O > V_{CC}$)	±20 mA
Continuous Output Current Low	20 mA
Continuous Output Current High	20 mA

Table 5-2. Recommended Operating Conditions

Parameter	Recommended Condition		
	Min	Nom	Max
Supply Voltage (V_{CC})	4.50V	5.00V	5.50V
Operating Temperature Range	0°C		70°C

Table 5-3. DC Characteristics

V_{CC} = 5V, T_{CASE} = 25°C

Symbol	Parameter	Min	Typ	Max	Units	Notes
V_{IL}	Input LOW Voltage			0.8	V	V_{CC} = 4.5V
V_{IH}	Input HIGH Voltage	2.0			V	V_{CC} = 5.5V
V_{OL}	Output LOW Voltage			0.5	V	V_I = 0.1 V_{CC}, I_{OL} = 4 mA
V_{OH}	Output HIGH Voltage	3.7			V	V_I = 0.9 V_{CC}, I_{OH} = 4 mA
I_{IL}	Input Leakage Current		−70		μA	V_{IL} = 0V
I_{OL}	Output Low Current			4	mA	
I_{CC}	Power Supply Current		30		mA	
C_{IN}	Input Capacitance			7	pF	
C_{OUT}	Output Capacitance			34	pF	
V_T(1)	Input Threshold Voltage		1.3		V	
V_T(2)	Input Threshold Voltage		V_{CC}/2		V	

NOTES:
1. Specified for all input pins except MD(31:0), VWE#, BE#(3:0).
2. Specified for MD(31:0), VWE#, BE#(3:0).

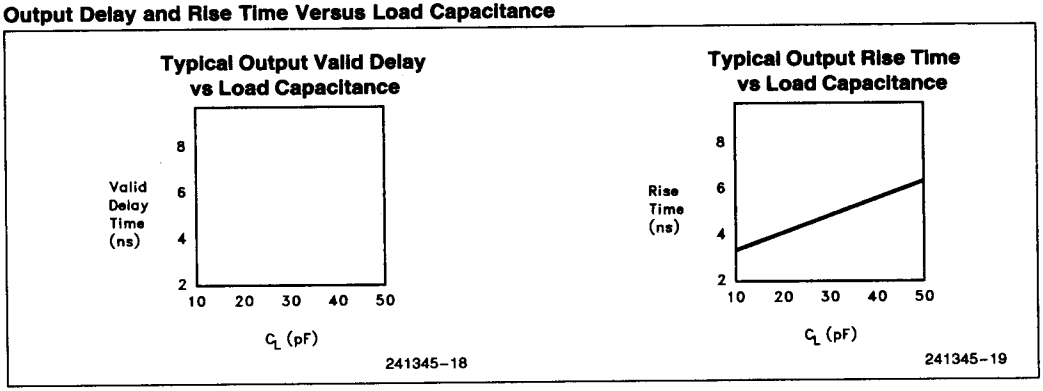
Table 5-4. CLK DC Characteristics

V_{CC} = 5V, T_{CASE} = 25°C

Symbol	Parameter	Min	Typ	Max	Units	Notes
V_{IL}	Input LOW Voltage			0.9	V	V_{CC} = 4.5V
V_{IH}	Input HIGH Voltage	3.85			V	V_{CC} = 5.5V
I_{IL}	Input LOW Leakage			±1	μA	V_{IH} = V_{CC}
I_{IH}	Input HIGH Leakage			±1	μA	V_{IL} = 0V
V_T	Input Threshold Voltage		2.5		V	
C_{IN}	Input Capacitance			7	pF	

1

Output Delay and Rise Time Versus Load Capacitance



5.2 A.C. Characteristics

NOTE:
Industry standard gate array test methodologies do not include full AC characterization. The AC characteristics below were determined through simulation and are provided as design guidelines only. These parameters are not fully tested in production. As per TI's standard gate array test methodology, two AC parametric measurements are made during production to guarantee the speed of the device. These measurements are indicated by an * in the table below.

Table 5-1. A.C. Characteristics

V_{CC} = 5V ±10%, T_A = 0°C to +70°C, C_L = 45 pF

Symbol	Parameter	Min	Max	Units	Figure	Notes
t1	V1CLK High to CHANREQ# Low	6	26	ns	5-1	
t2	V1CLK High to CHANREQ# High	5	23	ns	5-1	
t3	GAVALEN Setup before V1CLK High	1		ns	5-1	
t4	MREQ# Setup before V1CLK High	5		ns	5-1	
t5	MREQ# Hold after V1CLK High	3		ns	5-1	
t6	BUSEN# Low to VA(23:0) Enabled	2	43	ns	5-1	
t7	V1CLK High to VA(23:0) Valid		35	ns	5-1	
t8	V1CLK High to VA(23:0) Invalid	6		ns	5-1	
t9	BUSEN# High to VA(23:0) Disabled		3	ns	5-1	
t10	VWE# Setup before V1CLK High	5		ns	5-1	
t11*	V1CLK High to RAS# Low	5	32	ns	5-1	
t12	V1CLK High to RAS# High	4	27	ns	5-1	
t13	V1CLK High to CAS# Low	7	31	ns	5-1	
t14	V1CLK High to CAS# High	6	27	ns	5-1	
t15	V1CLK High to MUX Low	4	28	ns	5-1	
t16	V1CLK High to MUX High	5	34	ns	5-1	
t17	V1CLK High to MSTRB# Low	4	25	ns	5-1	
t18	V1CLK High to MSTRB# High	4	25	ns	5-1	
t19	MD(31:0) Address Setup before V1CLK High	0		ns	5-1	
t20	MD(31:0) Hold after V1CLK High	13		ns	5-1	
t21	V1CLK High to DTOE# Low	7	30	ns	5-1	
t22	V1CLK High to DTOE# High	6	24	ns	5-1	
t23	V1CLK High to MRDY# Low	6	24	ns	5-1	
t24	V1CLK High to MRDY# High	5	20	ns	5-1	
t25	V1CLK High to WE# Low	7	30	ns	5-2	
t26	V1CLK High to WE# High	7	31	ns	5-2	
t27	NXTFST# Low Setup to V1CLK High	0		ns	5-3	
t28	NXTFST# High Setup to V1CLK High	0		ns	5-3	
t29	TRNFR# Low Setup to V1CLK High	0		ns	5-5	
t30	TRNFR# High Setup to V1CLK High	0		ns	5-5	
t31	RFRSH# Low Setup to V1CLK High	0		ns	5-6	

Table 5-1. A.C. Characteristics (Continued)

V_{CC} = 5V ±10%, T_A = 0°C to +70°C, C_L = 45 pF

Symbol	Parameter	Min	Max	Units	Figure	Notes
t32	RFRSH# High Setup to V1CLK High	0		ns	5-6	
t33	V1CLK High to DSTRB# Low	6	26	ns	5-7	
t34	V1CLK High to DSTRB# High	5	24	ns	5-7	
t35	WRITE DATA Setup before V1CLK High	10		ns	5-7	
t36	WRITE DATA Hold after V1CLK High	35		ns	5-7	
t37*	V1CLK High to READ DATA Enabled and Valid		65	ns	5-8	
t38	V1CLK High to READ DATA Disabled		5	ns	5-8	
t39	BRSTREQ# Setup before V1CLK High	3		ns	5-9	
t40	YVUSEL Hold after BRSTREQ# Low	5		ns	5-9	
t41	YVUSEL# Setup before BRSTREQ# Low	3		ns	5-9	
t42	V1CLK High to CHANREQ# Low	6	26	ns	5-9	
t43	V1CLK High to CHANREQ# High	5	23	ns	5-9	
t44	BUSEN# Setup before V1CLK High	6		ns	5-9	
t45	VSCSEL# Setup before V1CLK High	5		ns	5-9	
t46	V1CLK High to BRSTACK# Transition	5	34	ns	5-9	
t47	V1CLK High to DCLK Transition	5	25	ns	5-9	

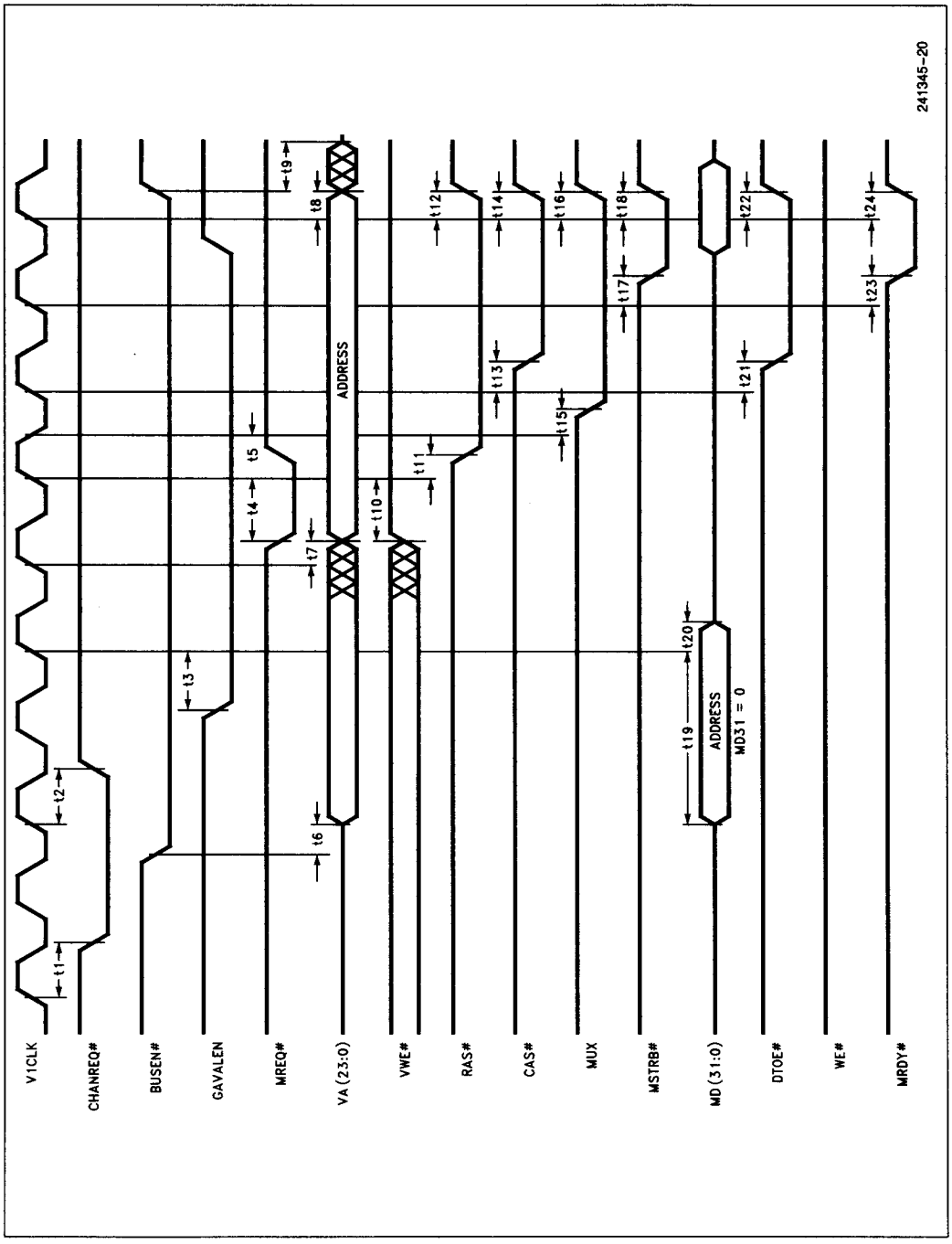


Figure 5-1. VRAM Read Cycle

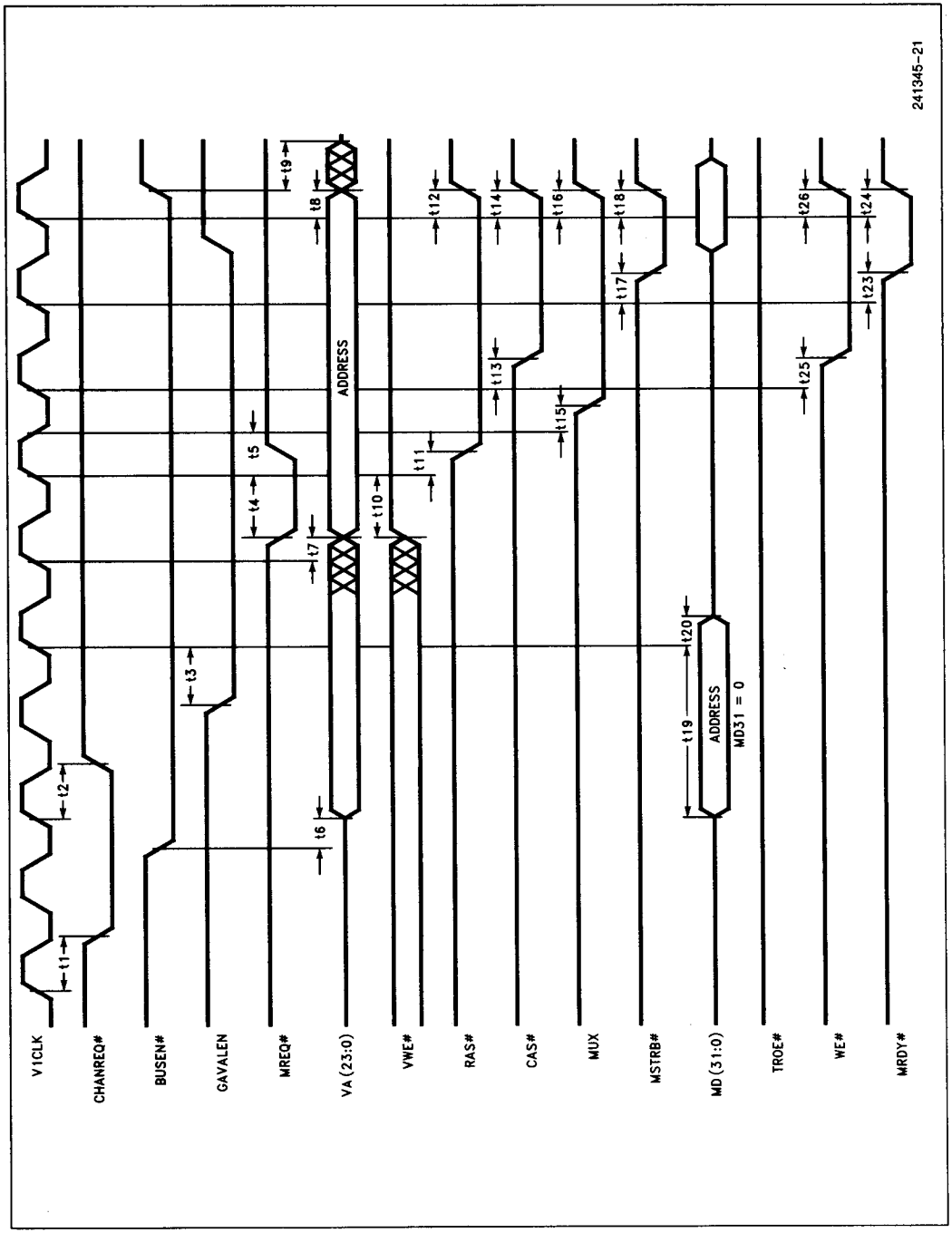


Figure 5-2. SCSI to VRAM Write Cycle

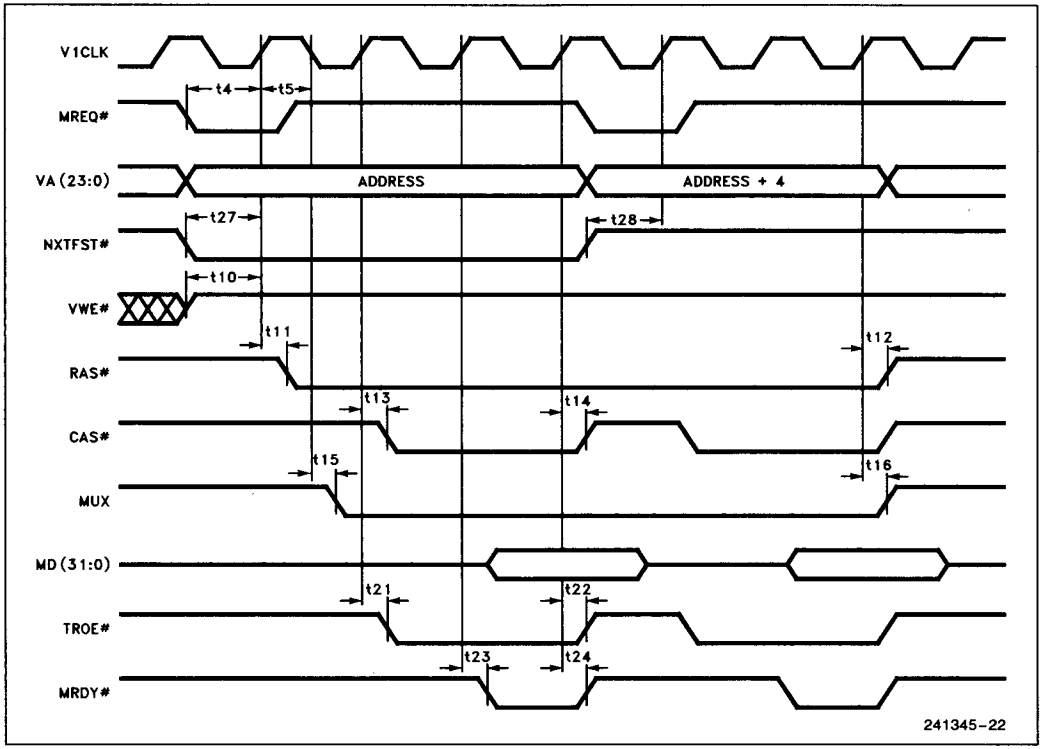


Figure 5-3. VRAM NXTFST Read Cycle

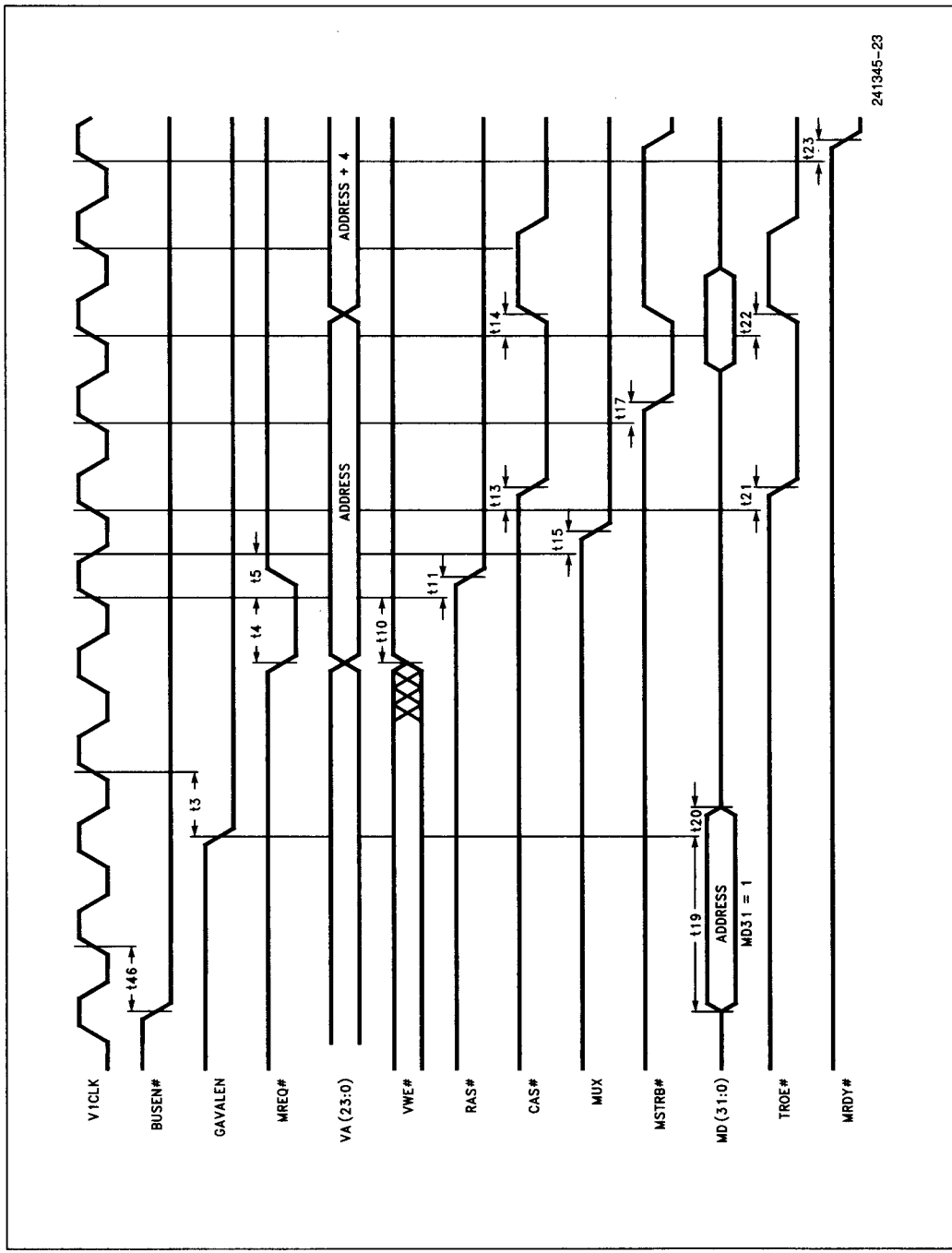


Figure 5-4. VRAM Busfast Read Cycle

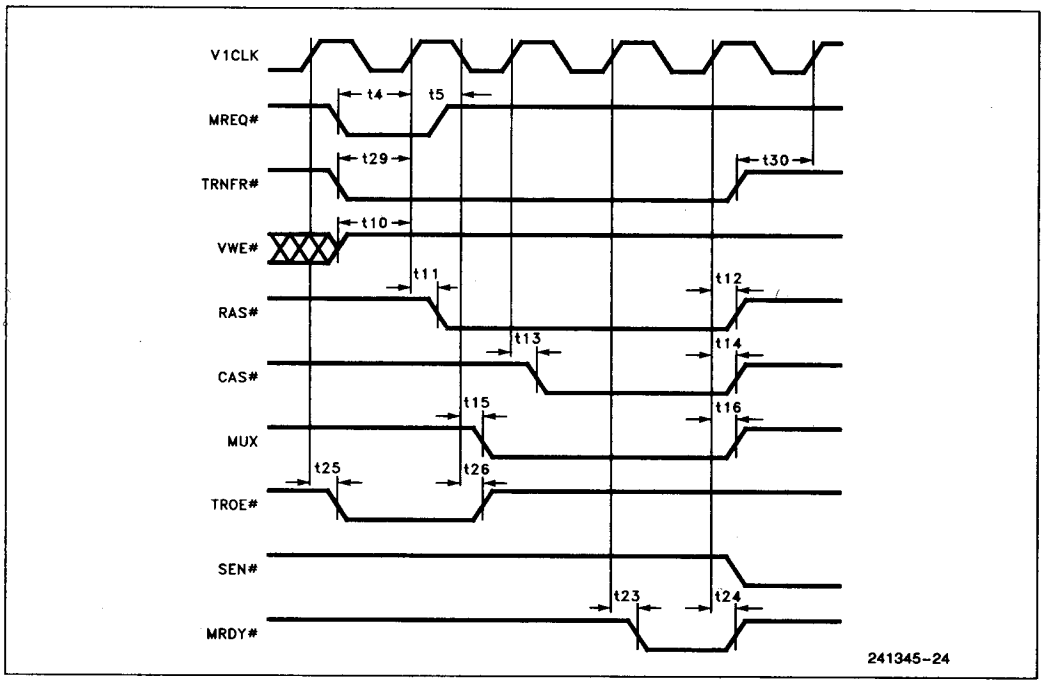


Figure 5-5. VRAM Data Transfer Cycle

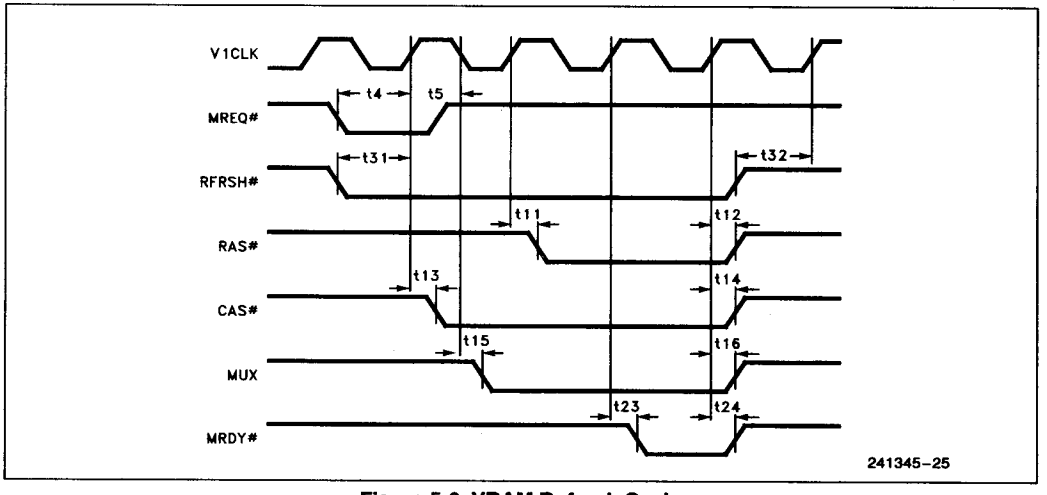


Figure 5-6. VRAM Refresh Cycle

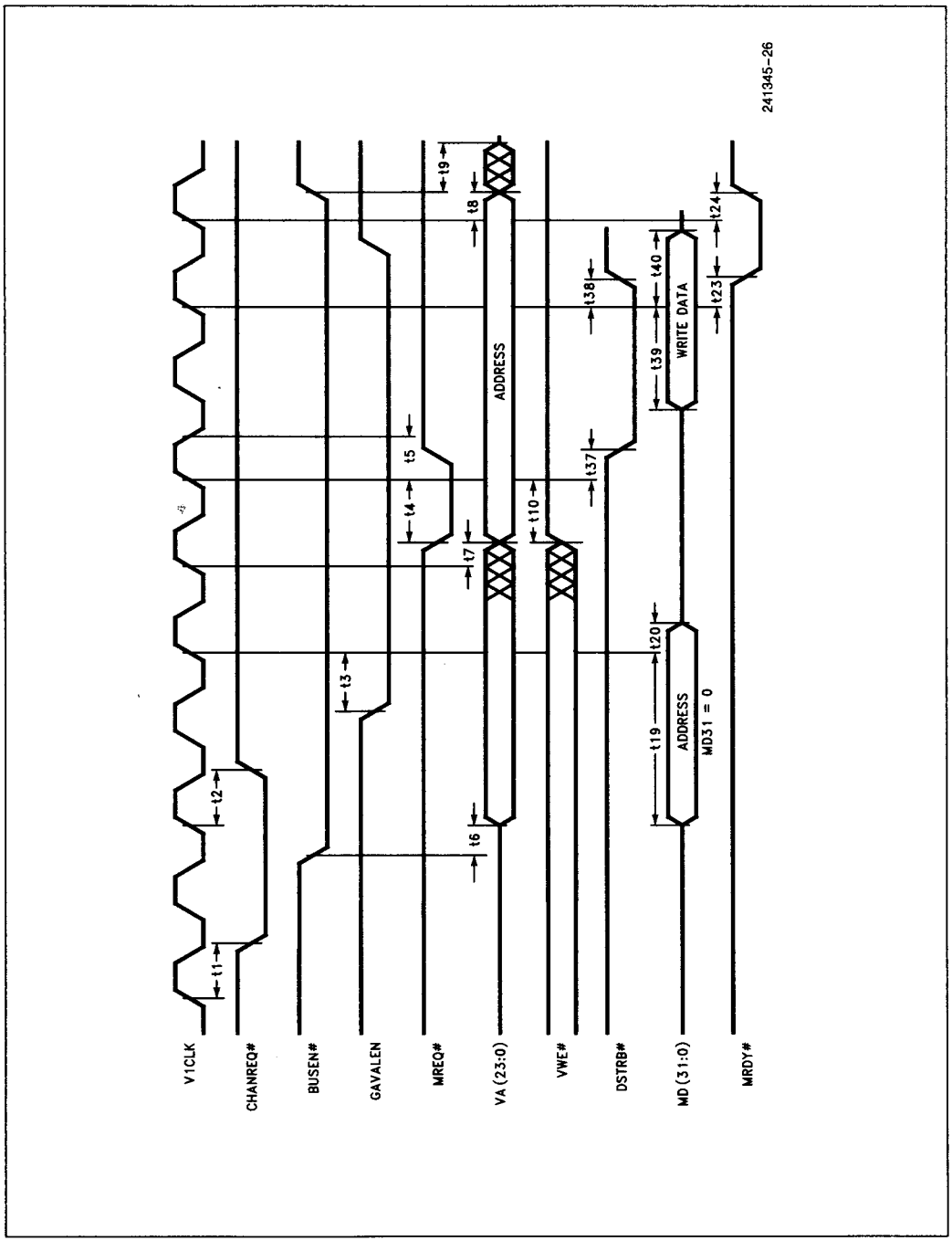


Figure 5-7. DVI Register Write Cycle

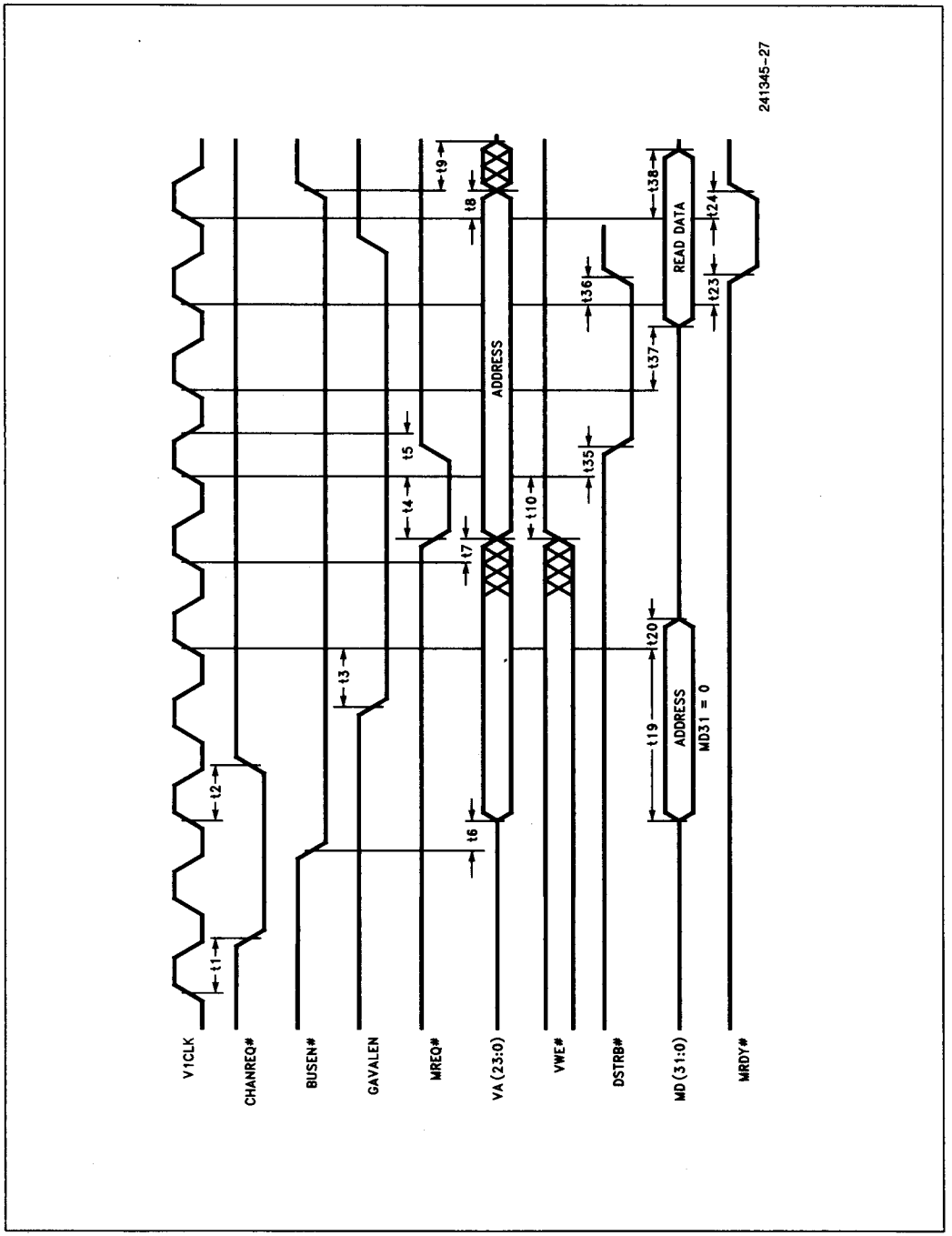


Figure 5-8. DVI Register Read Cycle

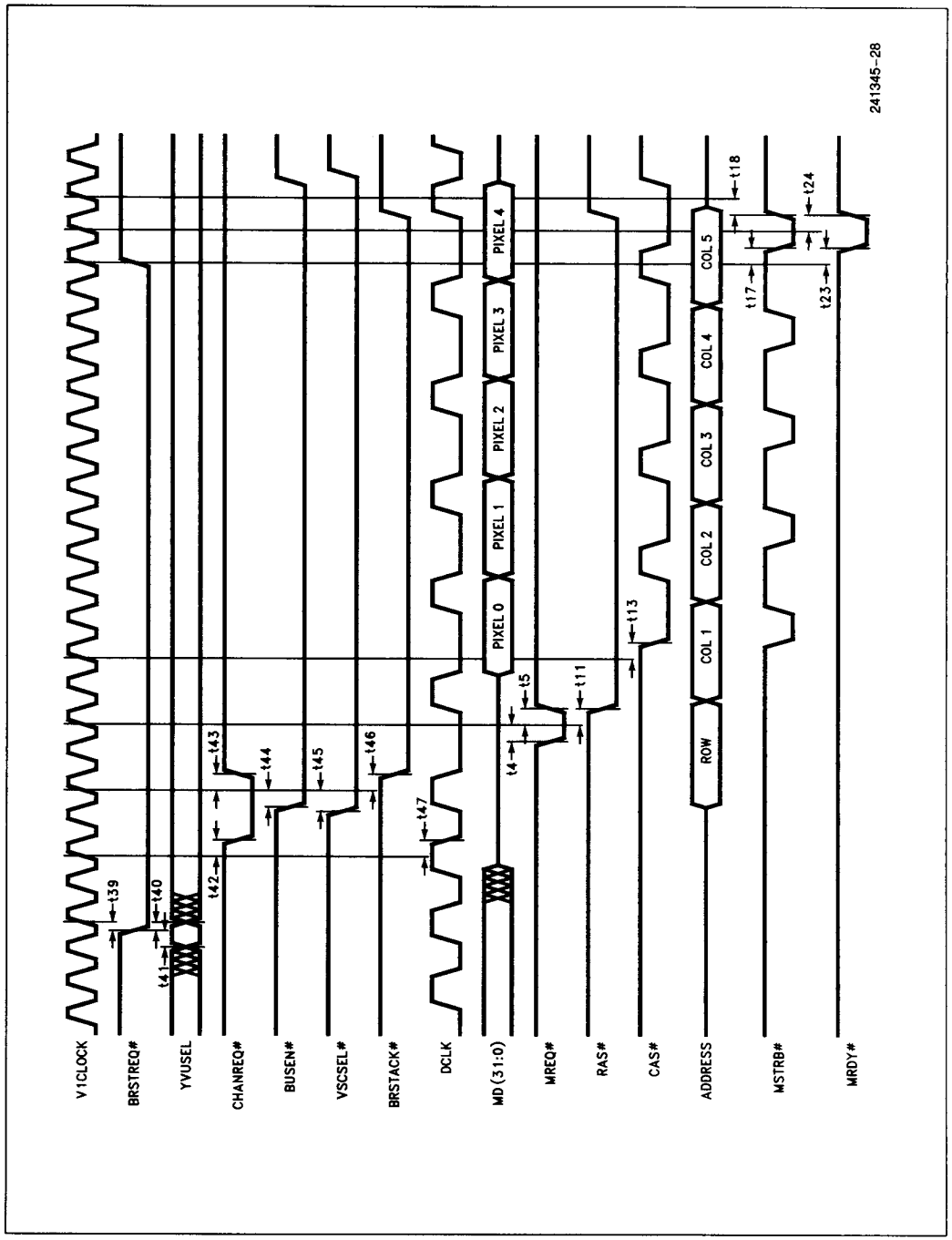
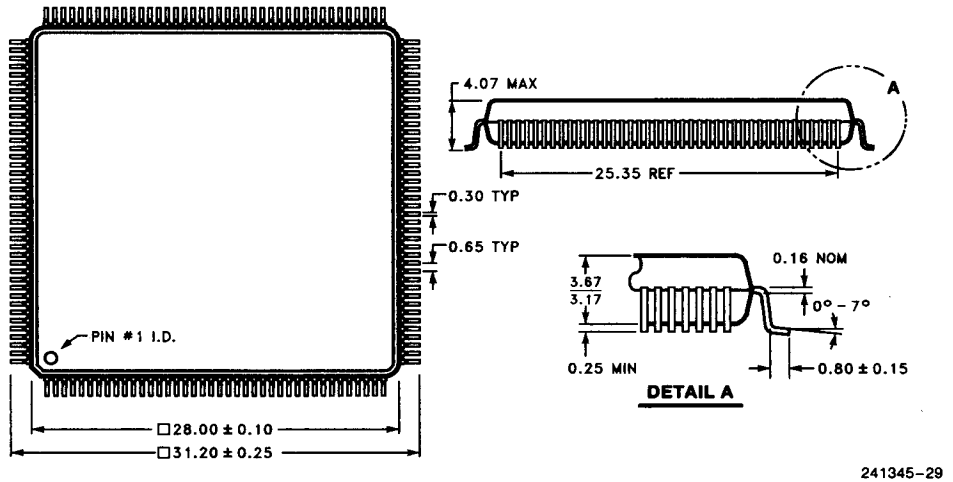


Figure 5-9. Capture Burst



NOTES:
1. All dimensions are in millimeters.
2. Co-planarity within 0.10mm.

6.0 MECHANICAL SPECIFICATIONS

6.1 Packaging Outlines and Dimensions

6.2 Package Thermal Specifications

Thermal impedance is defined as the ability to dissipate heat generated by an electronic device and is characterized by θ_{JA} and θ_{JC}. It is measured in degrees Celcius per Watt. θ_{JA} is the thermal impedance from the IC chip junction in still air ambient with the package mounted in a socket or directly mounted on a PC board. θ_{JC} is the thermal impedance from the IC junction to the external package case. Measurements are typically taken using high air flow to simulate an infinite heat sink. The thermal characteristics of the 160-lead PQFP package are as follows:

$$\theta_{JA} = 60.0°C/W$$

$$\theta_{JC} = 18.0°C/W$$