



# 3.3 Volt CMOS 8-Bit Buffers/Line Drivers

QS74FCT3540  
QS74FCT3541  
QS74FCT32540  
QS74FCT32541

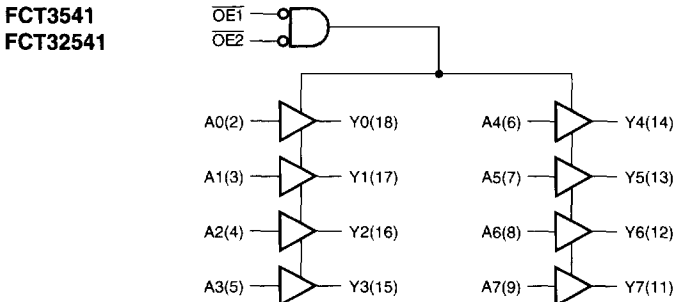
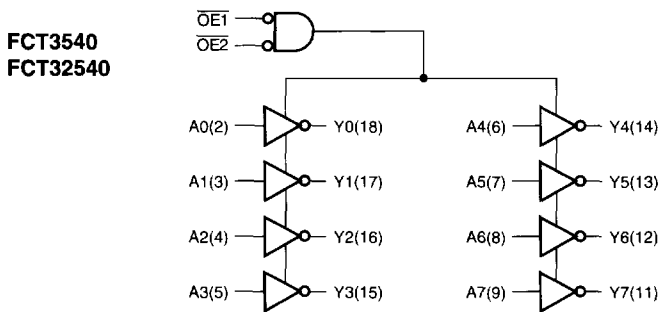
## FEATURES/BENEFITS

- Pin and function compatible to the 74F540/1 74LVT540/1 and 74FCT540T/1T
- Available in SOIC and QSOP
- Undershoot clamp diodes on all inputs
- Ground bounce controlled outputs
- Low power QCMOS: 0.03  $\mu$ W typ static
- JEDEC spec compatible
- $I_{OL} = 24$  mA Com.
- TTL-compatible input and output levels
- Extended temperature  $-40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$
- 2.7V to 3.6V Supply Voltage
- 5V compatible input pins

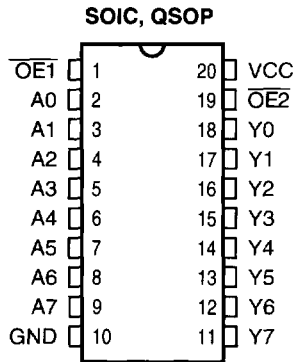
## DESCRIPTION

The FCT3540 and FCT3541 are 8-bit buffers/line drivers with three-state outputs that is ideal for driving high-capacitance loads as in memory address and data buses. All inputs have clamp diodes for undershoot noise suppression and all outputs have ground bounce suppression (see QSI Application Note AN-001). Input pins can be driven by 3.3V or 5V components allowing voltage transition in mixed supply systems. Ultra-low power QCMOS technology makes this product ideal for portable computing systems or communications devices.

## FUNCTIONAL BLOCK DIAGRAM



**PIN CONFIGURATIONS (All Pins Top View)**



**PIN DESCRIPTION**

Name	I/O	Description
A7-A0	I	Data Inputs
Y7-Y0	O	Data Outputs
$\overline{OE1}$ , $\overline{OE2}$	I	Output Enable

**FUNCTION TABLE**

$\overline{OE1}$	$\overline{OE2}$	Input A	3540	3541	Function
			Output Y	Output Y	
H	X	X	Hi-Z	Hi-Z	Disable Outputs
X	H	X	Hi-Z	Hi-Z	
L	L	L	H	L	Enable Outputs
L	L	H	L	H	

**ABSOLUTE MAXIMUM RATINGS<sup>(1)</sup>**

Supply Voltage to Ground .....	-0.5V to +4.6V
DC Output Voltage $V_{OUT}$ .....	-0.5V to $V_{CC} + 0.5V^{(2)}$
DC Input Voltage $V_{IN}$ .....	-0.5V to +7.0V
AC Input Voltage (for a pulse width $\leq 20$ ns) .....	-3.0V
DC Input Diode Current with $V_{IN} < 0$ .....	$\pm 20$ mA
DC Output Diode Current with $V_{OUT} < 0$ .....	$\pm 50$ mA
DC Output Current Max. Sink Current/Pin .....	$\pm 60$ mA
Maximum Power Dissipation .....	0.5 watts
$T_{STG}$ Storage Temperature .....	-65° to +150°C

**Note:**

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to this device resulting in functional or reliability type failures.
2. Not to exceed 4.6V

**CAPACITANCE**

$T_A = 25^\circ C$ ,  $f = 1$  MHz,  $V_{IN} = 0V$ ,  $V_{OUT} = 0V$

Pins	SOIC	QSOP	Unit
1, 19	4	4	pF
2-9, 11-18	8	8	pF

**Note:** Capacitance is characterized but not tested.

**RECOMMENDED OPERATING CONDITIONS**

Symbol	Description	Min	Max	Unit
$V_{CC}$	Supply Voltage	2.7	3.6	V
$V_{IN}$	Input Voltage	0	$V_{CC}$	V
$V_{OUT}$	Output Voltage	0	$V_{CC}$	V
$T_A$	Ambient Operating Temperature	-40	+85	°C
$\Delta t/\Delta V$	Input Transition Rise or Fall Rate <sup>(1)</sup>	0	8	ns/V

**Notes:**

1. As measured between 0.8V and 2V.

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**DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE**

Recommended operating conditions apply unless otherwise specified.

Symbol	Parameter	Test Conditions	Min	Typ <sup>(1)</sup>	Max	Unit
V <sub>IH</sub>	Input HIGH Voltage	Input Pins	2.0	—	5.5	V
		I/O Pins	2.0	—	V <sub>CC</sub> +0.5	V
V <sub>IL</sub>	Input LOW Voltage	Input Pins	-0.5	—	0.8	V
ΔV <sub>T</sub>	Input Hysteresis	V <sub>TLH</sub> - V <sub>THL</sub> for All Inputs	—	0.2	—	V
I <sub>IH</sub>    I <sub>IL</sub>	Input Current Input HIGH or LOW	V <sub>CC</sub> = Max., 0 ≤ V <sub>IN</sub> < V <sub>CC</sub>	—	—	1	μA
I <sub>OZ</sub>	Off-State Output Current (Hi-Z)	V <sub>CC</sub> = Max., 0 ≤ V <sub>IN</sub> ≤ V <sub>CC</sub>	—	—	5	μA
I <sub>OS</sub>	Short Circuit Current	V <sub>CC</sub> = Max., V <sub>OUT</sub> = GND <sup>(2,3)</sup>	-60	—	-225	mA
V <sub>IC</sub>	Input Clamp Voltage	V <sub>CC</sub> = Min., I <sub>IN</sub> = -18 mA <sup>(3)</sup>	—	-0.7	—	V
V <sub>OH</sub>	Output HIGH Voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> , V <sub>CC</sub> = Min, I <sub>OH</sub> = -100 μA	V <sub>CC</sub> -0.2	—	—	V
		V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> , V <sub>CC</sub> = 3V, I <sub>OH</sub> = -8 mA	2.4	—	—	V
V <sub>OL</sub>	Output LOW Voltage (FCT3XXX)	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> , V <sub>CC</sub> = Min, I <sub>OL</sub> = 100 μA	—	—	0.2	V
		V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> , V <sub>CC</sub> = 3V, I <sub>OL</sub> = 16 mA	—	—	0.4	V
		V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> , V <sub>CC</sub> = 3V, I <sub>OL</sub> = 24 mA	—	—	0.5	V
V <sub>OL</sub>	Output LOW Voltage (FCT32XXX-25Ω)	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> , V <sub>CC</sub> = 3V, I <sub>OL</sub> = 8 mA	—	—	0.5	V
R <sub>OUT</sub>	Output Resistance <sup>(4)</sup> (FCT32XXX-25Ω)	V <sub>CC</sub> = 3V, I <sub>OL</sub> = 8 mA	—	40	—	Ω

**Notes:**

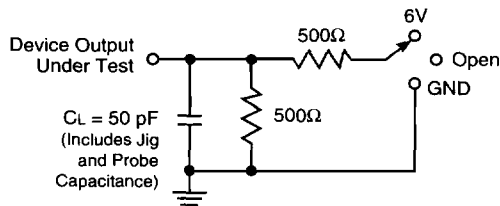
1. Typical values indicate V<sub>CC</sub> = 3.3V and T<sub>A</sub> = 25°C.
2. Not more than one output should be shorted and the duration is ≤1 second.
3. These parameters are guaranteed by design but not tested.
4. R<sub>OUT</sub> represents total output impedance and includes added series termination resistance.

**POWER SUPPLY CHARACTERISTICS**

Symbol	Parameter	Test Conditions <sup>(1)</sup>	Min	Typ	Max	Unit
I <sub>cc</sub>	Quiescent Power Supply Current	V <sub>cc</sub> = Max., freq = 0 0V ≤ V <sub>IN</sub> ≤ 0.2V or V <sub>cc</sub> -0.2V ≤ V <sub>IN</sub> ≤ V <sub>cc</sub>	—	0.01	20	μA
ΔI <sub>cc</sub>	Supply Current per Input @ TTL HIGH	V <sub>cc</sub> = Max., freq = 0, V <sub>IN</sub> = V <sub>cc</sub> - 0.6V	—	1.0	20	μA
Q <sub>ccd</sub>	Supply Current per Input per MHz	V <sub>cc</sub> = Max., Outputs Open and Enabled One Bit Toggling @ 50% Duty Cycle Other Inputs at GND or V <sub>cc</sub> <sup>(2,3)</sup>	—	40	85	μA/ MHz

**Notes:**

1. For conditions shown as Min. or Max., use the appropriate values specified under DC specifications.
2. For flip-flops, Q<sub>ccd</sub> is measured by switching one of the data input pins so that the output changes every clock cycle. This is a measurement of device power consumption only and does not include power to drive load capacitance or tester capacitance. This parameter is guaranteed by design but not tested.
3. I<sub>c</sub> can be computed using the above parameters as explained in the Technical Overview section.



Test	Switch
t <sub>PHL</sub> /t <sub>PLH</sub>	Open
t <sub>PZL</sub> /t <sub>PLZ</sub>	6V
t <sub>PZH</sub> /t <sub>PHZ</sub>	GND

**Load Circuit for Outputs**

**Notes**

1. Input pulse characteristics: 0V to 2.7V, t<sub>r</sub> = t<sub>f</sub> = 2.5 ns (10% to 90%), transition measured at 1.5V, pulse generator Z<sub>out</sub> = 50Ω.

**SWITCHING CHARACTERISTICS OVER OPERATING RANGE**

Recommended operating conditions apply unless otherwise specified.

**FCT3540/32540**

Symbol	Description <sup>(1)</sup>	3540, 32540 (V <sub>CC</sub> = 3.3V ± 0.3V)		3540A, 32540A (V <sub>CC</sub> = 3.3V ± 0.3V)		Unit
		Min	Max	Min	Max	
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay A <sub>i</sub> to Y <sub>i</sub> , FCT3540	1.5	8.5	1.5	4.8	ns
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay A <sub>i</sub> to Y <sub>i</sub> , FCT32540	1.5	8.5	1.5	4.8	ns
t <sub>PZH</sub> t <sub>PZL</sub>	Output Enable $\overline{OE}$ to Y <sub>i</sub> , FCT3540	1.5	10	1.5	6.2	ns
t <sub>PZH</sub> t <sub>PZL</sub>	Output Enable $\overline{OE}$ to Y <sub>i</sub> , FCT32540	1.5	10	1.5	6.2	ns
t <sub>PLZ</sub> t <sub>PHZ</sub>	Disable Time <sup>(2)</sup>	1.5	9.5	1.5	5.6	ns

**Notes:**

1. Minimums guaranteed but not tested.
2. This parameter is guaranteed by design but not tested.
3. See Test Circuit and Waveforms.

**FCT3541/32541**

Symbol	Description <sup>(1)</sup>	3541, 32541 (V <sub>CC</sub> = 3.3V ± 0.3V)		3541A, 32541A (V <sub>CC</sub> = 3.3V ± 0.3V)		Unit
		Min	Max	Min	Max	
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay A <sub>i</sub> to Y <sub>i</sub> , FCT3541	1.5	8	1.5	4.8	ns
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay A <sub>i</sub> to Y <sub>i</sub> , FCT32541	1.5	8	1.5	4.8	ns
t <sub>PZH</sub> t <sub>PZL</sub>	Output Enable $\overline{OE}$ to Y <sub>i</sub> , FCT3541	1.5	10	1.5	6.2	ns
t <sub>PZH</sub> t <sub>PZL</sub>	Output Enable <sup>(2)</sup> $\overline{OE}$ to Y <sub>i</sub> , FCT32541	1.5	10	1.5	6.2	ns
t <sub>PLZ</sub> t <sub>PHZ</sub>	Disable Time <sup>(2)</sup>	1.5	9.5	1.5	5.6	ns

**Notes:**

1. Minimums guaranteed but not tested.
2. This parameter is guaranteed by design but not tested.
3. See Test Circuit and Waveforms.