STANDARD MICROSYSTEMS CORPORATION

FDC91C36/ FDC92C36

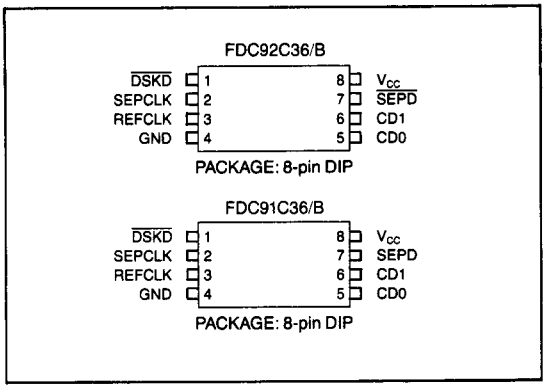
PRELIMINARY

CMOS Floppy Disk Data Separator

FEATURES

- ☐ High Performance Digital Data Separator
- ☐ Pin Replacement for FDC9216 (FDC92C36)
- ☐ Performs complete data separation function for floppy disk drives
- ☐ Eliminates all adjustments normally associated with high performance data separators
- ☐ Single +5 Volt Supply
- ☐ Fully TTL compatible
- ☐ Fabricated in power saving CMOS
- ☐ Compatible with 3.5", 5.25" and 8" drives and data rates up to 500 Kb/s
- ☐ 16-Bit half Cell Divide Algorithm greatly improves performance over conventional digital designs

PIN CONFIGURATION



FUNCTIONAL DESCRIPTION

The FDC92C36 is a direct high performance CMOS pin for pin replacement for the FDC9216 in systems using data transfer rates of 250Kb/s or 125Kb/s.

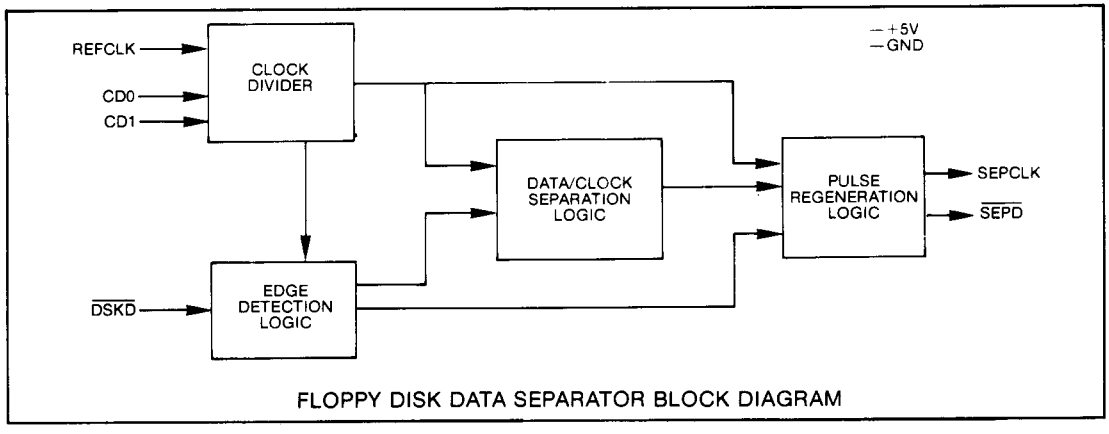
The FDC92C36B can be used in systems having a 500Kb/s data transfer rate by applying a 16MHz input clock to pin 3 and applying a low level to pin 6 and a high level to pin 5.

The FDC91C36/B is designed for use with the FDC765A, 8272A or FDC72C65 floppy disk controller. The FDC91C36/B provides an active high SEPD output, eliminating the inverter required when using the FDC9216/B.

The FDC91C36/FDC92C36 incorporates a high performance, synthetic phase locked loop digital data separator in a 300 mil wide 8 pin package.

The use of a high performance synthetic phase locked loop allows the system designer to replace a costly and board consuming analog data separator (and the tuning normally required with an analog design) with a cost effective, single chip digital circuit.

The FDC92C36 and the FDC91C36 are available in two versions: the parts without a "B" suffix (FDC92C36, FDC91C36) are intended for 5.25" drives using data rates of 250 Kb/s, and the parts with a "B" suffix (FDC92C36B, FDC91C36B) are intended for 3.5", 5.25" and 8" drives using data rates of 500 Kb/s.



FLOPPY DISK DATA SEPARATOR BLOCK DIAGRAM

SECTION VI

DESCRIPTION OF PIN FUNCTIONS

PIN NO.	NAME	SYMBOL	FUNCTION
1	Disk Data	$\overline{DSKD}$	Data input signal direct from disk drive. Contains combined clock and data waveform.
2	Separated Clock	SEPCLK	Clock signal output from the FDDS derived from floppy disk drive serial bit stream.
3	Reference Clock	REFCLK	Reference clock input
4	Ground	GND	Ground
5,6	Clock Divisor	CD0, CD1	CD0 and CD1 control the internal clock divider circuit. Refer to Table 1.
7	Separated Data Separated Data	SEPD $\overline{SEPD}$	(FDC91C36) (FDC92C36) This output is the regenerated data pulse derived from the raw data input. This output is positive for the FDC91C36 and negative for the FDC92C36.
8	Power Supply	V_{DD}	+5 volt power supply

OPERATION

A reference clock (REFCLK) of 8 or 16 MHz is divided by the FDDS to provide an internal clock. The division ratio is selected by inputs CD0 and CD1. The reference clock and division ratio should be chosen per table 1.

The FDDS detects the leading edges of the disk data pulses and adjusts the phase of the internal clock to provide the SEPARATED CLOCK output.

Separate short and long term timing correctors assure accurate clock separation.

The SEPCLK frequency is nominally 1/32 the internal clock frequency. Depending on the internal timing correction, the duration of any SEPCLK half-cycle may vary from a nominal of 16 to a minimum of 12 and a maximum of 21 internal clock cycles.

The reference clock (REFCLK) is divided to provide the internal clock according to pins CD0 and CD1.

TABLE 1

CD1	CD0	8MHz REFCLK	9.6 MHz	16MHz REFCLK	DIVISOR f(REFCLK)/f(INTCLK)
0	0	not used	not used	5 1/4" SD 3 1/2" SD①	4
0	1	8" SD 5 1/4" DD 3 1/2" DD①	5 1/4" QD②	8" DD 5 1/4" QD	1
1	0	5 1/4" SD 3 1/2" SD①	not used	8" SD 5 1/4" DD 3 1/2" DD①	2
1	1	Illegal	Illegal	Illegal	Illegal

NOTES: ①Some 3 1/2" drives are 8" compatible (instead of 5 1/4" as assumed in Table 1). For these drives, use 8" values.
②9.6 MHz clock is used to read or write a 5 1/4" double density diskette on a quad density drive.

PERFORMANCE SPECIFICATIONS

PARAMETER		MFM 500KHZ	MFM 250KHZ	UNITS
BIT JITTER				
	NOMINAL SPEED	+/−260	+/−540	nsec
	+5% SPEED	+/−260	+/−480	nsec
	−5% SPEED	+/−320	+/−640	nsec
WINDOW MARGIN	EARLY	500	980	nsec
	LATE	500	980	nsec
	COMBINED	+/−400	+/−740	nsec

MAXIMUM GUARANTEED RATINGS*

Operating Temperature Range ..... 0°C to +70°C
Storage Temperature Range ..... −55° to +150°C
Lead Temperature (soldering, 10 sec.) ..... +300°C
Positive Voltage on any I/O Pin, with respect to ground ..... V_{CC} +0.3V
Negative Voltage on any I/O Pin, with respect to ground ..... −0.3V
Power Dissipation 0.75W
Maximum Voltage on V_{CC} Pin, with respect to ground 7.0V

*Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied.

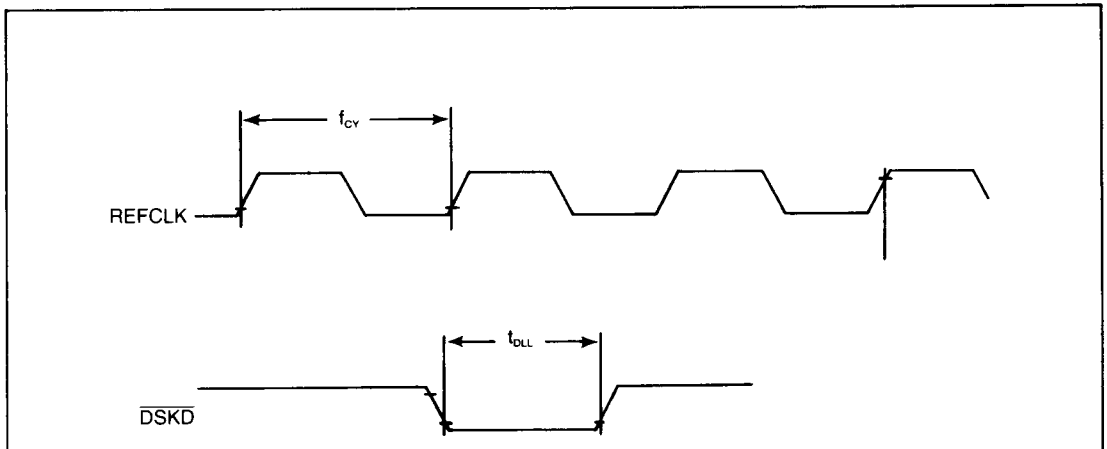
NOTE: When powering this device from laboratory or system power supplies, it is important that the Absolute Maximum Ratings not be exceeded or device failure can result. Some power supplies exhibit voltage spikes or "glitches" on their outputs when the AC power is switched on and off. In addition, voltage transients on the AC power line may appear on the DC output. If this possibility exists it is suggested that a clamp circuit be used.

ELECTRICAL CHARACTERISTICS (T_A = 0°C to 70°C, V_{DD} = +5V ± 5%, unless otherwise noted)

Parameter	SYMBOL	Min.	Typ.	Max.	Units	Comments
D.C. CHARACTERISTICS						
INPUT VOLTAGE LEVELS						
Low Level V_{IL}				0.8	V	
High Level V_{IH}		2.0			V	
OUTPUT VOLTAGE LEVELS						
Low Level V_{OL}				0.4	V	I_{OL} = 1.6mA
High Level V_{OH}		2.4			V	I_{OH} = −100 µA
INPUT CURRENT						
Leakage I_{IL}				10.0	µA	$O<V_{IN}<V_{DD}$
INPUT CAPACITANCE						
All Inputs				10.0	pF	
POWER SUPPLY CURRENT						
I_{DD}				20.0	mA	
A.C. CHARACTERISTICS						
REFCLK Frequency	f_{cy}	1.0	8.0	8.1	MHz	FDC 92C36/FDC 91C36
REFCLK Frequency	f_{cy}	1.0	16.0	16.2.	MHz	FDC 92C36B/FDC 91C36B
$\overline{DSKD}$ Active Low Time	t_{DLL}	0.05		100.0	µs	
$\overline{CLKIN}$ Duty Cycle		40		60	%	

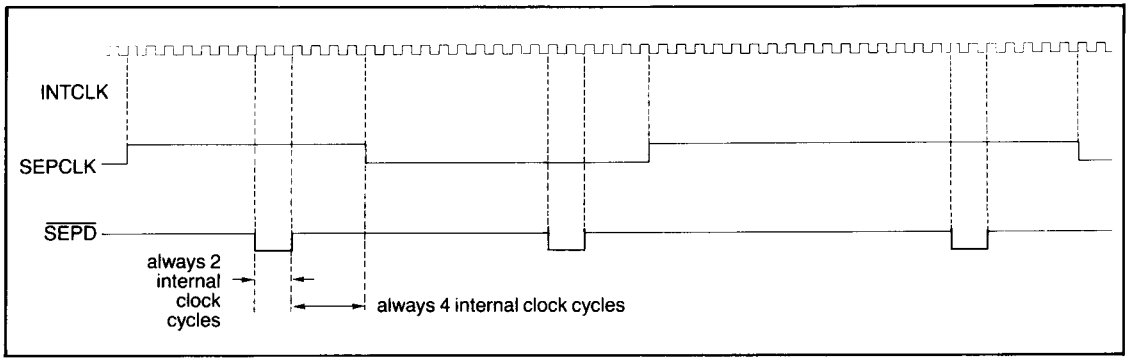
PRELIMINARY
Notice: This is not a final specification. Some parameter limits are subject to change.

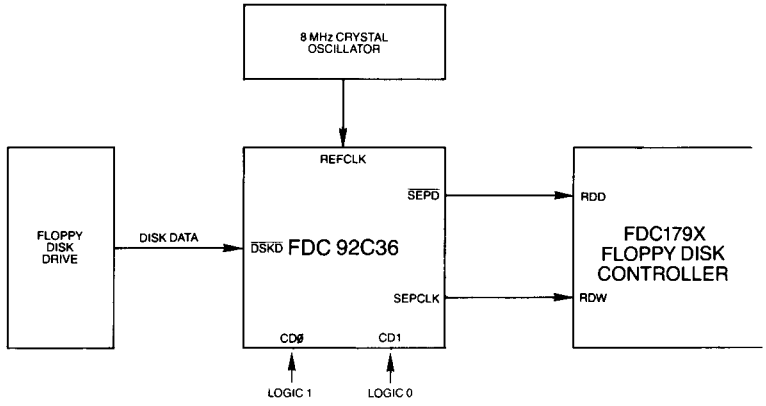
*All times assume XTAL/CLKIN = 16 MHz unless otherwise specified.



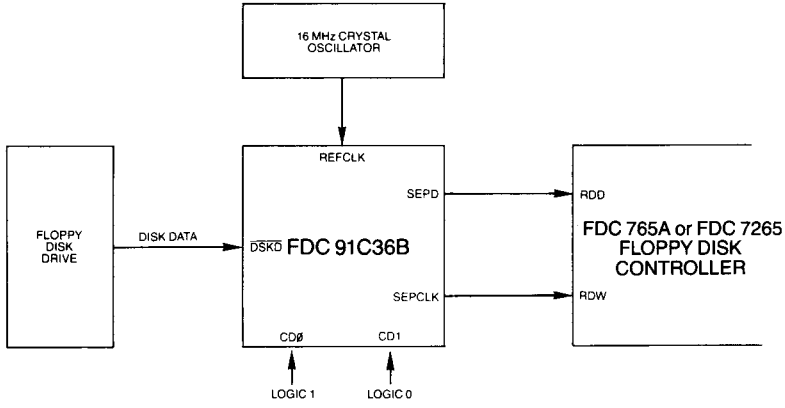
AC CHARACTERISTICS

SECTION VI





TYPICAL SYSTEM CONFIGURATION FOR THE FDC92C36/B
(FDC179X Floppy Disk Controller, 5¼" Drive, Double Density)



TYPICAL SYSTEM CONFIGURATION FOR THE FDC91C36/B
(FDC765A Floppy Disk Controller, 1.2 MB 5 1/4" Drive)