Rochester Electronics

Datasheet

PART NUMBER

CLC502ABPA-ROCS

Rochester Electronics Manufactured Components

Rochester branded components are manufactured using either die/wafers purchased from the original suppliers or Rochester wafers recreated from the original IP. All re-creations are done with the approval of the Original Component Manufacturer. (OCM)

Parts are tested using original factory test programs or Rochester developed test solutions to guarantee product meets or exceeds the OCM data sheet.

Quality Overview

- ISO-9001
- AS9120 certification
- Qualified Manufacturers List (QML) MIL-PRF-38535
    - Class Q Military
    - Class V Space Level

Qualified Suppliers List of Distributors (QSLD)

- Rochester is a critical supplier to DLA and meets all industry and DLA standards.

Rochester Electronics, LLC is committed to supplying products that satisfy customer expectations for quality and are equal to those originally supplied by industry manufacturers.

The original manufacturer's datasheet accompanying this document reflects the performance and specifications of the Rochester manufactured version of this device. Rochester Electronics guarantees the performance of its semiconductor products to the original OCM specifications. 'Typical' values are for reference purposes only. Certain minimum or maximum ratings may be based on product characterization, design, simulation, or sample testing.

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MICROCIRCUIT DATA SHEET

MNCLC502A-X REV 0A0

Original Creation Date: 07/29/98
Last Update Date: 08/26/99
Last Major Revision Date: 07/29/98

CLAMPING, LOW-GAIN OP AMP WITH FAST 14-BIT SETTLING

General Description

The CLC502 is an operational amplifier designed for low-gain applications requiring output voltage clamping. This feature allows the designer to set maximum positive and negative output voltage levels for the amplifier - thus allowing the CLC502 to protect downstream circuitry, such as delicate converter systems, from destructive transients or signals which would otherwise cause saturation. The overload recovery time of only 8ns permits systems to resume operation quickly after overdrive.

High-accuracy systems will also benefit from the CLC502's fast, accurate settling. Settling to 0.0025% in 25ns (32ns guaranteed over temperature), the CLC502 is ideal as the input amplifier in high-accuracy (12 bits and above) A/D systems. Unlike most other high-speed op amps, the CLC502 is free of settling tails. And, as the settling plots show, settling to 0.01% accuracy is an even faster 18ns typical.

The CLC502 is also useful in other applications which require low-gain amplification ($\pm$1 to $\pm$8) and the clamping or overload recovery features. For example, even low-resolution imaging circuits, which often have to cope with overloading signal levels, can benefit from clamping and overload recovery.

Industry Part Number

CLC502A

NS Part Numbers

CLC502AE-QML
CLC502AJ-QML

Prime Die

VB1302A

Controlling Document

5962-9174301MPA, M2A

Processing

MIL-STD-883, Method 5004

Quality Conformance Inspection

MIL-STD-883, Method 5005

Subgrp	Description	Temp (^{o}C)
1	Static tests at	+25
2	Static tests at	+125
3	Static tests at	-55
4	Dynamic tests at	+25
5	Dynamic tests at	+125
6	Dynamic tests at	-55
7	Functional tests at	+25
8A	Functional tests at	+125
8B	Functional tests at	-55
9	Switching tests at	+25
10	Switching tests at	+125
11	Switching tests at	-55

Features

- Output clamping with fast recovery
- 0.0025% settling in 25ns (32ns max.)
- Low power, 170mW
- Low distortion. -50dBc at 20MHz

Applications

- Output clamping applications
- High-accuracy A/D systems (12-14 bits)
- High-accuracy D/A converters
- Pulse amplitude modulation systems

(Absolute Maximum Ratings)
(Note 1)

Supply Voltage (V±)	±7 Vdc
Output Current (Iout)	70 mA
Junction Temperature (Tj)	+175 C
Storage Temperature Range	-65 C to +150 C
Lead Temperature (Soldering, 10 seconds)	+300 C
Power Dissipation (Pd) (Note 2)	1.2W
Common Mode Input Voltage (Vcm)	V±
Thermal Resistance	
Junction-to-ambient (ThetaJA)	
Ceramic DIP (Still Air)	TBD
(500 LFPM)	TBD
LCC (Still Air)	TBD
(500 LFPM)	TBD
Junction-to-case (ThetaJC)	
Ceramic DIP	TBD
LCC	TBD
Package Weight (Typical)	
CERAMIC DIP	TBD
LCC	TBD
ESD Tolerance (Note 3)	1000V

Note 1: Absolute Maximum Ratings are limits beyond which damage to the device may occur. Operating Ratings are conditions for which the device is functional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions see the Electrical Characterisitics. The guaranteed specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.

Note 2: The maximum power dissipation must be derated at elevated temperatures and is dictated by Tjmax (maximum junction temperature), ThetaJA (package junction to ambient thermal resistance), and TA (ambient temperature). The maximum allowable power dissipation at any temperature is Pdmax = (Tjmax - TA) /ThetaJA or the number given in the Absolute Maximum Ratings, whichever is lower.

Note 3: Human body model, 100pF discharged through 1.5k Ohms.

Recommended Operating Conditions

Supply Voltage (V±)	±5 Vdc
Gain Range (Av)	+1 to +10 and -1 to -10
Ambient Operating Temperature Range (Ta)	-55 C to +125 C

Electrical Characteristics

DC PARAMETERS: Open Loop Characteristics

(The following conditions apply to all the following parameters, unless otherwise specified.)
DC: Rl = 100 Ohms, V± = ±5 Vdc, Vhigh = +3 V, Vlow = -3 V, Av = +2, and feedback resistance (Rf) = 250 Ohms. -55 C ≤ Ta ≤ +125 C (Note 3)

SYMBOL	PARAMETER	CONDITIONS	NOTES	PIN-NAME	MIN	MAX	UNIT	SUB-GROUPS
+Iin	Input Bias Current (NonInverting)	Rs = 50 Ohms			-25	+25	uA	1
					-35	+35	uA	2
					-45	+45	uA	3
-Iin	Input Bias Current (Inverting)	Rs = 50 Ohms			-30	+30	uA	1
					-40	+40	uA	2
					-50	+50	uA	3
Vio	Input Offset Voltage	Rs = 50 Ohms			-1.6	+1.6	mV	1
					-2.8	+2.8	mV	2
					-2.6	+2.6	mV	3
Tc (+Iin)	Average +Input Bias Current Drift	Rs = 50 Ohms	1		-100	+100	nA/C	2
			1		-250	+250	nA/C	3
Tc (-Iin)	Average -Input Bias Current Drift	Rs = 50 Ohms	1		-100	+100	nA/C	2
			1		-250	+250	nA/C	3
Tc (Vio)	Average Input Offset Voltage Drift	Rs = 50 Ohms	1		-12	+12	uV/C	2, 3
Is	Quiescent Supply Current	No Load				23	mA	1, 2, 3
PSRR	Power Supply Rejection Ratio	V+ = +4.5V to +5.0V, V- = -4.5V to -5.0V	2		60		dB	1, 2
			2		55		dB	3
CMRR	Common Mode Rejection Ratio	Vcm = ±1V	1		60		dB	4, 5
			1		55		dB	6
+Vcm	Common Mode Input Voltage		1		+2.5		V	4, 5
			1		+2.0		V	6
-Vcm	Common Mode Input Voltage		1			-2.5	V	4, 5
			1			-2.0	V	6
+Iout	Output Current		1		+45		mA	1, 2
			1		+25		mA	3
-Iout	Output Current		1			-45	mA	1, 2
			1			-25	mA	3
Rout	Output Impedance at dc	Vin = 0V	1			0.2	Ohms	1, 2, 3

Electrical Characteristics

DC PARAMETERS: Open Loop Characteristics(Continued)

(The following conditions apply to all the following parameters, unless otherwise specified.)
DC: Rl = 100 Ohms, V± = ±5 Vdc, Vhigh = +3 V, Vlow = -3 V, Av = +2, and feedback resistance (Rf) = 250 Ohms. -55 C ≤ Ta ≤ +125 C (Note 3)

SYMBOL	PARAMETER	CONDITIONS	NOTES	PIN-NAME	MIN	MAX	UNIT	SUB-GROUPS
+Rin	Noninverting Input Resistance		1		85		KOhms	1, 2
			1		50		KOhms	3
+Cin	Noninverting Input Capacitance		1			5.5	pF	4, 5, 6
+Vout	Output Voltage Swing	Rl = 100 Ohms	2		+2.4		V	4, 5, 6
-Vout	Output Voltage Swing	Rl = 100 Ohms	2			-2.4	V	4, 5, 6

AC PARAMETERS: CLAMPING CHARACTERISTICS

(The following conditions apply to all the following parameters, unless otherwise specified.)
DC:
AC: Rl = 100 Ohms, V± = ±5 Vdc, Vhigh = +3 V, Vlow = -3 V, Av = +2, and feedback resistance (Rf) = 250 Ohms. -55 C ≤ Ta ≤ +125 C (Note 3)

Voc	Clamp Accuracy				-0.3	+0.3	V	1, 2, 3
Icl	Input Bias Current on Vhigh and Vlow		1		-35	+35	uA	1, 2
			1		-75	+75	uA	3
OVC	Overshoot In Clamp	Ta = +25 C	1			10	%	4
CMC	Clamping Range	At Vhigh or Vlow	1		-3.3	+3.3	V	4, 5
			1		-3.0	+3.0	V	6
TSO	Overload Recovery From Clamp		1			15	ns	9, 10, 11

Electrical Characteristics

AC PARAMETERS: Frequency Domain Characteristics

(The following conditions apply to all the following parameters, unless otherwise specified.)
AC: Rl = 100 Ohms, V± = ±5 Vdc, Vhigh = +3 V, Vlow = -3 V, Av = +2, and feedback resistance (Rf) = 250 Ohms. -55 C ≤ Ta ≤ +125 C (Note 3)

SYMBOL	PARAMETER	CONDITIONS	NOTES	PIN-NAME	MIN	MAX	UNIT	SUB-GROUPS
SSBW	Small Signal Bandwidth	-3 dB bandwidth, Vout < 0.5 Vpp			110		MHz	4
			2		100		MHz	5, 6
LSBW	Large Signal Bandwidth	-3 dB bandwidth, Vout < 5 Vpp	1		40		MHz	4, 5, 6
GFPL	Gain Flatness, peaking low	0.1 MHz to 25 MHz, Vout < 0.5 Vpp				0.3	dB	4
			2			0.4	dB	5, 6
GFPH	Gain Flatness, peaking high	At > 25 MHz, Vout < 0.5 Vpp				0.5	dB	4
			2			0.7	dB	5, 6
GFR	Gain Flatness, rolloff	0.1 MHz to 50 MHz, Vpp < 0.5 Vpp				1.0	dB	4
			2			1.0	dB	5, 6
LPD	Linear Phase Deviation	Tested at 0.1 MHz to 50 MHz	1			1.0	Deg	4
			1			1.2	Deg	5, 6

AC PARAMETERS: Distortion and Noise Characteristics

(The following conditions apply to all the following parameters, unless otherwise specified.)
AC: Rl = 100 Ohms, V± = ±5 Vdc, Vhigh = +3 V, Vlow = -3 V, Av = +2, and feedback resistance (Rf) = 250 Ohms. -55 C ≤ Ta ≤ +125 C (Note 3)

HD2	2nd Harmonic Distortion	2 Vpp at 20 MHz				-43	dBc	4
			2			-43	dBc	5
			2			-38	dBc	6
HD3	3rd Harmonic Distortion	2 Vpp at 20 MHz				-53	dBc	4
			2			-53	dBc	5, 6
SNF	Equivalent Input Noise Floor	At > 1 MHz	1			-155	dBm	4, 5, 6
INV	Equivalent Input Integrated Noise	At 1 MHz to 150 MHz	1			49	uV	4, 5, 6

Electrical Characteristics

AC PARAMETERS: Time Domain Characteristics

(The following conditions apply to all the following parameters, unless otherwise specified.)
AC: Rl = 100 Ohms, V± = ±5 Vdc, Vhigh = +3 V, Vlow = -3 V, Av = +2, and feedback resistance (Rf) = 250 Ohms. -55 C ≤ Ta ≤ +125 C (Note 3)

SYMBOL	PARAMETER	CONDITIONS	NOTES	PIN-NAME	MIN	MAX	UNIT	SUB-GROUPS
+SR	Slew Rate	Rising Edge, Cl < 10 pF, measured at ±1V with 3V step	1		500		V/uS	4, 5, 6
-SR	Slew Rate	Falling Edge, Cl < 10 pF, measured at ±1V with 3V step	1		500		V/uS	4, 5, 6
Trs	Rise and Fall Time	0.5V step, Cl < 10 pF, measured between 10% and 90% point	1			3.2	ns	9
			1			3.5	ns	10, 11
Trl	Rise and Fall Time	5V step, Cl < 10 pF, measured between 90% and 10% point	1			8	ns	9, 10, 11
Ts	Settling Time	2V step at ±0.0025% of the fixed value, Cl < 10 pF	1			32	ns	9, 10, 11
		2V step at ±0.01% of the fixed value, Cl < 10 pF	1			25	ns	9, 10, 11
		2V step at ±0.1% of the fixed value, Cl < 10 pF	1			15	ns	9, 10, 11
OS	Overshoot	0.5V step, Cl < 10 pF	1			10	%	9, 10, 11

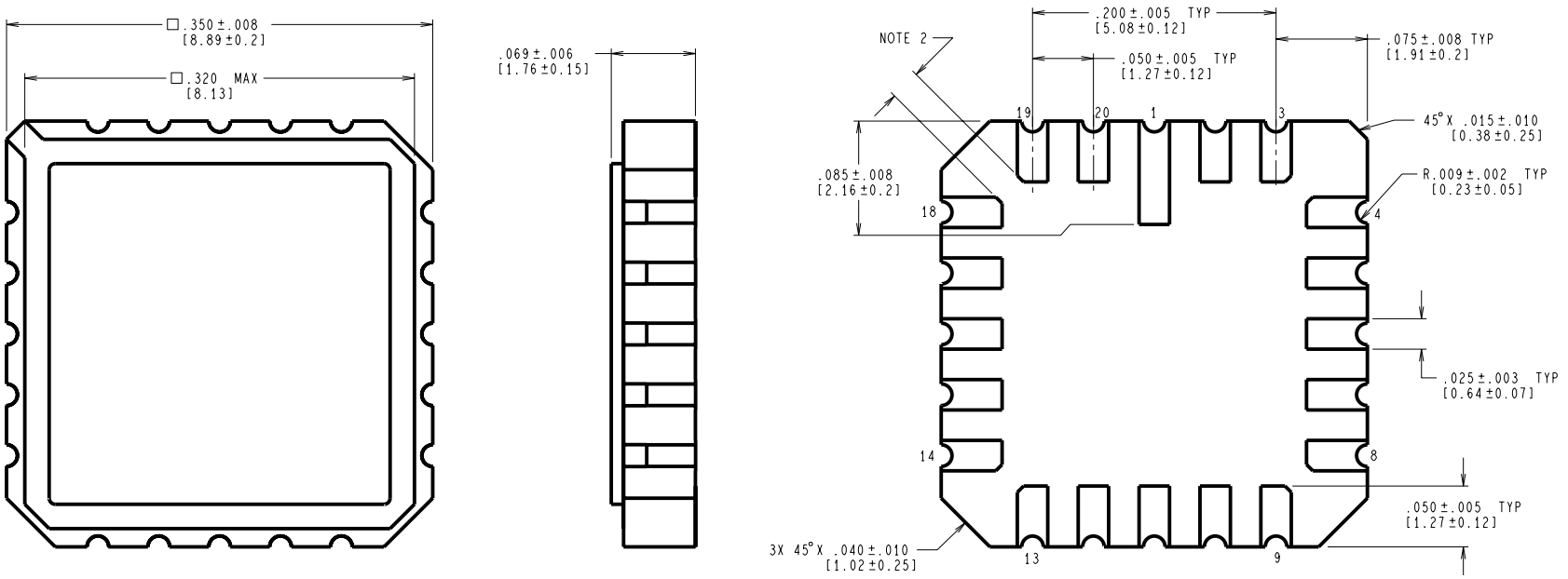
Note 1: If not tested, shall be guaranteed to the limits specified in table 1 herein.
Note 2: Group A testing only.
Note 3: The algebraic convention, whereby the most negative value is a minimum and the most positive is a maximum, is used in this table. Negative current shall be defined as conventional current flow out of a device terminal.

Graphics and Diagrams

GRAPHICS#	DESCRIPTION
07081HRA3	CERDIP (J), 8 LEAD (B/I CKT)
07086HRA2	LCC (E), TYPE C, 20 TERMINAL (B/I CKT)
E20ARE	LCC (E), TYPE C, 20 TERMINAL(P/P DWG)
J08ARL	CERDIP (J), 8 LEAD (P/P DWG)
P000400A	CERDIP (J), 8 LEAD (PINOUT)
P000470A	LCC (E), TYPE C, 20 TERMINAL (PIN OUT)

See attached graphics following this page.

REVISIONS				
LTR	DESCRIPTION	E.C.N.	DATE	BY/APP'D
E	REVISE AND REDRAW.	10005	02/10/94	DEG/



CONTROLLING DIMENSION IS INCH
VALUES IN [ ] ARE MILLIMETERS

NOTES: UNLESS OTHERWISE SPECIFIED.

1. LEAD FINISH TO BE ONE OF THE FOLLOWING:

   a. 50 MICROINCHES/12.7 MICROMETERS MINIMUM GOLD PLATING OVER 50-350 MICROINCHES/1.27-8.89 MICROMETERS NICKEL.

   b. SOLDER DIP.
   SOLDER THICKNESS PER LATEST REVISION OF MIL-STD-1835.

2. CORNER PADS MAY HAVE A 45°X.020IN/0.51mm MAXIMUM CHAMFER TO ACCOMPLISH THE .015IN/0.38mm DIMENSION.

4. REFERENCE JEDEC REGISTRATION MS-004, VARIATION CB, DATED 7/90.

MIL/AERO
CONFIGURATION CONTROL

APPROVALS	DATE
DRAWN *Dwayne Grady*	02/10/94
DFTG. CHK.	
ENGR. CHK.	
APPROVAL	

PROJECTION INCH [MM]

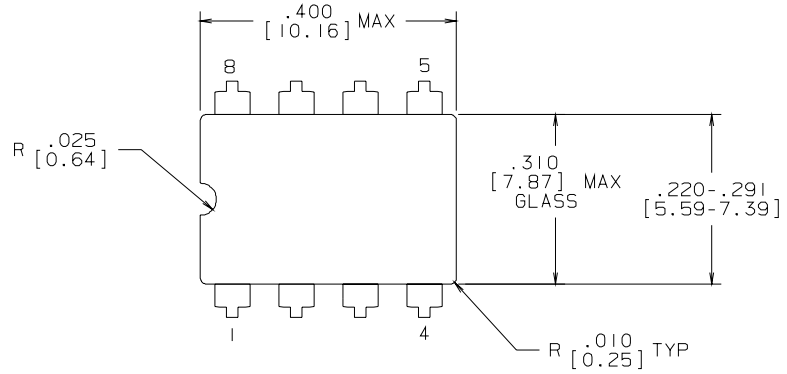
NATIONAL SEMICONDUCTOR CORPORATION
2900 Semiconductor Drive, Santa Clara, CA 95052-8090

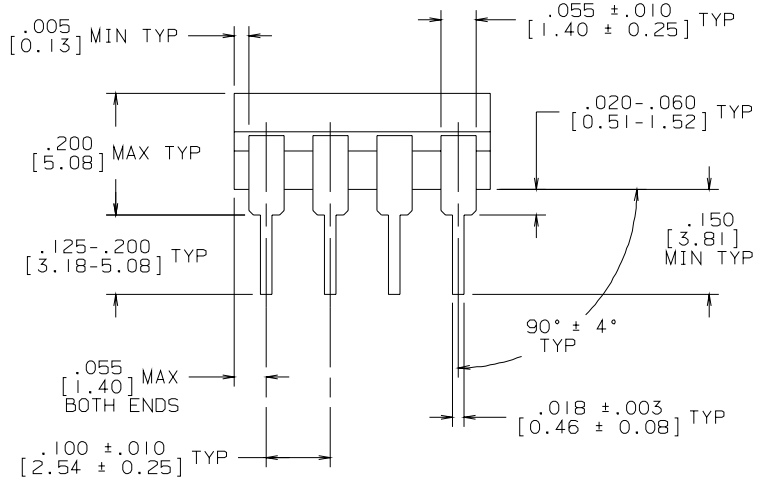
LEADLESS CHIP CARRIER,
TYPE C,
20 TERMINAL

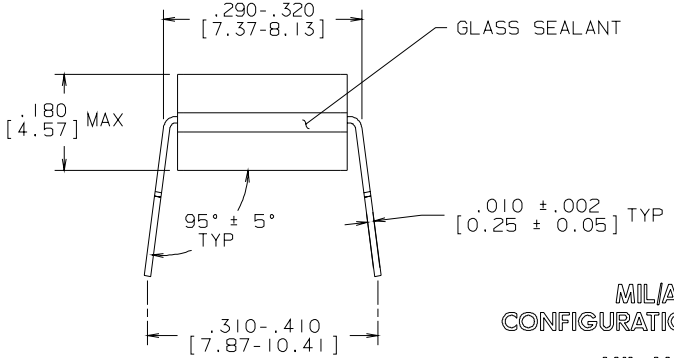
SCALE	SIZE	DRAWING NUMBER	REV
N/A	C	MKT-E20A	E

DO NOT SCALE DRAWING | SHEET 1 of 1

REVISIONS				
LTR	DESCRIPTION	E.C.N.	DATE	BY/APP'D
L	REVISE PER CURRENT STD; REDRAW	I0002	09/21/93	TL/







MIL/AERO
CONFIGURATION CONTROL

MIL-M-38510
CONFIGURATION CONTROL

NOTES: UNLESS OTHERWISE SPECIFIED

1. LEAD FINISH TO BE 200 MICROINCHES / 5.08 MICROMETERS MINIMUM SOLDER MEASURED AT THE CREST OF THE MAJOR FLATS.
2. JEDEC REGISTRATION MO-036, VARIATION AA, DATED 04/1981.

CONTROLLING DIMENSION: INCH

APPROVALS	DATE
DRAWN T. LEQUANG	09/21/93
DFTG. CHK.	
ENGR. CHK.	
APPROVAL	

PROJECTION

INCH
[MM]

NATIONAL SEMICONDUCTOR CORPORATION
2900 Semiconductor Drive, Santa Clara, CA 95052-8090

CERDIP (J),
8 LEAD

SCALE	SIZE	DRAWING NUMBER	REV
N/A	B	MKT-J08A	L

DO NOT SCALE DRAWING | SHEET 1 OF 1

CLC502J

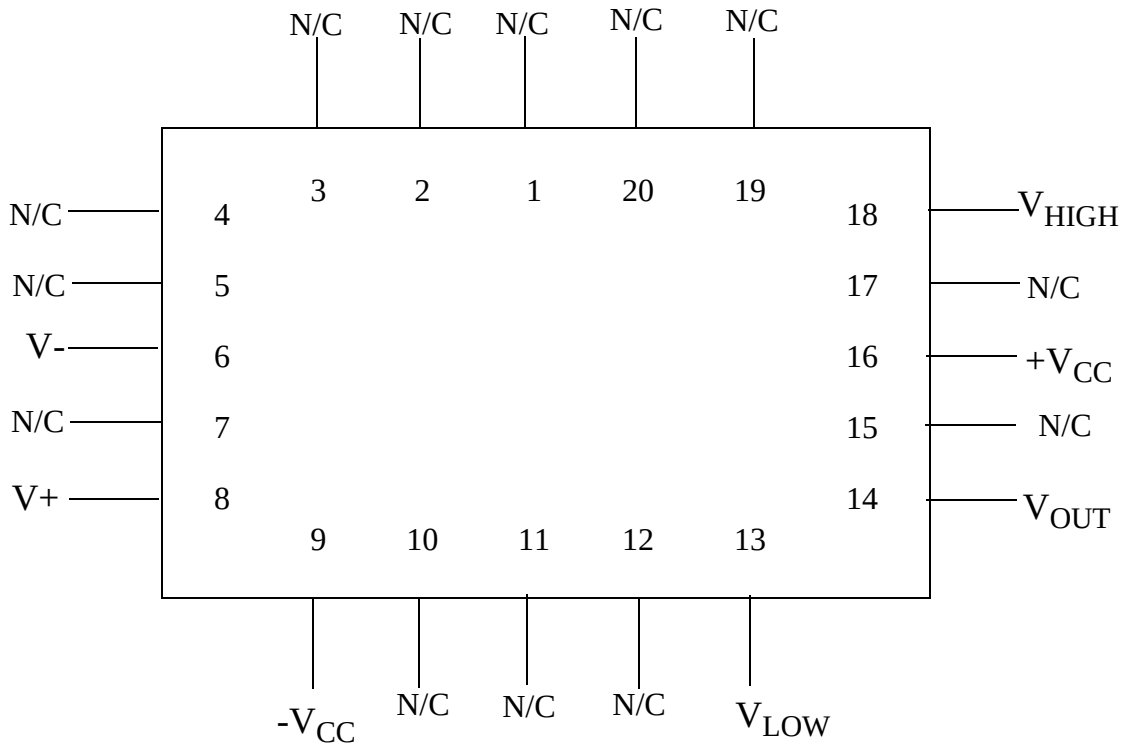
8 - LEAD DIP

CONNECTION DIAGRAM

TOP VIEW

P000400A

National Semiconductor™
MIL/AEROSPACE OPERATIONS
2900 SEMICONDUCTOR DRIVE
SANTA CLARA, CA 95050



CLC502AE

20 - LEAD LCC

CONNECTION DIAGRAM

TOP VIEW

P000470A

National Semiconductor™
MIL/AEROSPACE OPERATIONS
2900 SEMICONDUCTOR DRIVE
SANTA CLARA, CA 95050

Revision History

Rev	ECN #	Rel Date	Originator	Changes
0A0	M0003528	08/26/99	Shaw Mead	Initial MDS Release