TEXAS INSTRUMENTS

TLK3114SA

10-Gbps XAUI Transceiver

Data Manual

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MSDS Multimedia

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1 Description

The TLK3114SA device is a flexible quad serial transceiver, delivering high-speed, bidirectional, point-to-point data transmissions to provide up to 10 Gbps of data transmission capacity. The TLK3114SA device is terminal compatible with the TLK3104SA quad serial transceiver and supports an operating range of serial data rates from 2.5 Gbps to 3.125 Gbps. The primary application of this device is to provide building blocks for developing point-to-point baseband data transmission over controlled-impedance media of approximately 50 Ω. The transmission media can be printed-circuit board (PCB) traces, copper cables, or fiber-optical media. The ultimate rate and distance of data transfer is dependent upon the attenuation characteristics of the media and the noise coupling into the lines.

The TLK3114SA device performs the parallel-to-serial, serial-to-parallel conversion, and clock extraction functions for a physical layer interface. The TLK3114SA device also provides a selectable 8-b/10-b encode/decode function. The serial transmitter is implemented using differential pseudoemitter controlled logic (PECL) compatible signaling called voltage mode logic (VML) that eliminates the need for external components. The serial receiver employs an equalization circuit to maximize receive capabilities.

The four transceivers in the TLK3114SA device can be configured as either four separate links or synchronized together as a single data path. The TLK3114SA device supports both the 32-bit data path, 4-bit control, 10-gigabit media independent interface (XGMII), and the extended auxiliary unit interface (XAUI) specified in the IEEE 802.3ae 10-Gigabit Ethernet standard. Figure 1−1 shows an example system block diagram for the TLK3114SA device used as an XGMII extended sublayer (XGXS) device to provide an additional trace distance on PCB for data being transferred between the switching fabric and optical transceiver modules.

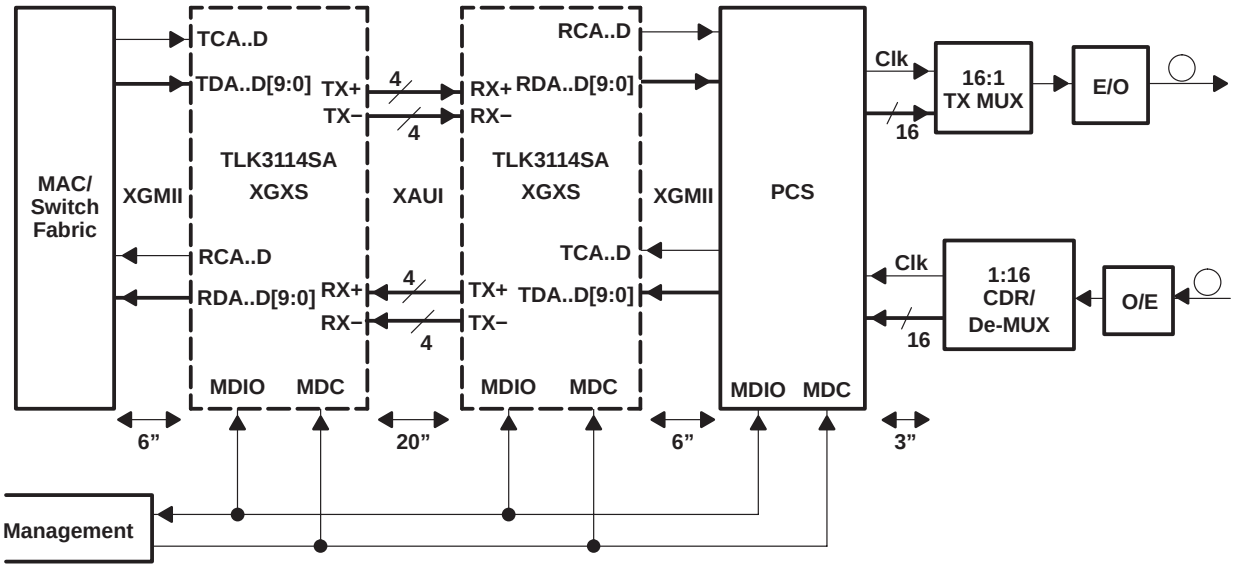


Figure 1−1. System Block Diagram (Chip-to-Chip Implementation)

Figure 1−2 shows an example system block diagram for TLK3114SA device used to provide the 10-Gbps Ethernet physical coding sublayer (as defined in IEEE802.3ae Clause 48) to coarse wavelength division multiplexed optical transceiver.

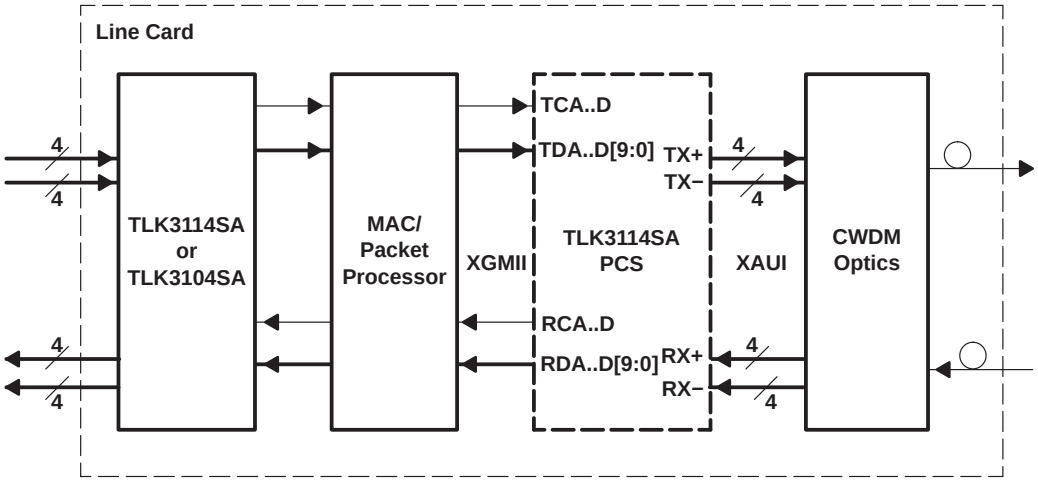


Figure 1−2. System Block Diagram (PCS Implementation)

Figure 1−3 shows an example system block diagram for the TLK3114SA device used to provide the system backplane interconnect.

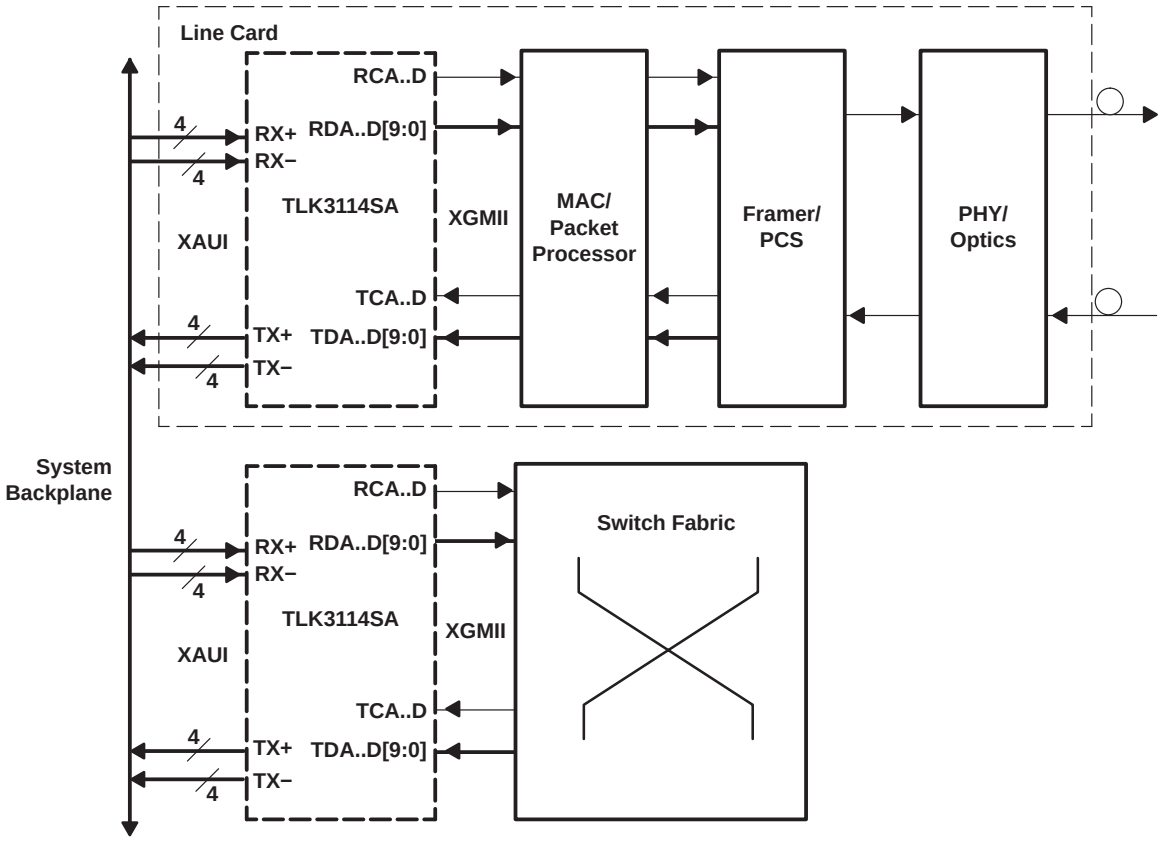


Figure 1−3. System Block Diagram (Backplane Interconnect Implementation)

The TLK3114SA device supports the IEEE 802.3 defined management data input/output (MDIO) interface to allow ease in configuration and status monitoring of the link.

The TLK3114SA device supports the IEEE 1149.1 defined JTAG test port for ease in board manufacturing test. It also supports a comprehensive series of built-in tests for self-test purposes including internal serial loopback and pseudorandom bit stream (PRBS) generation and verification.

The TLK3114SA device operates with a single 2.5-V supply and dissipates less than 3 W. The device is packaged in a 19-mm × 19-mm, 289-terminal plastic ball grid array (PBGA) package and is characterized for operation from 0°C to 70°C.

The TLK3114SA device is a member of a family of CMOS multi-gigabit transceivers, intended for use in high-speed bidirectional point-to-point data transmission systems.

Figure 1−4 provides a high-level description of the TLK3114SA device. For a detailed diagram of the individual channels, see Figure 1−5.

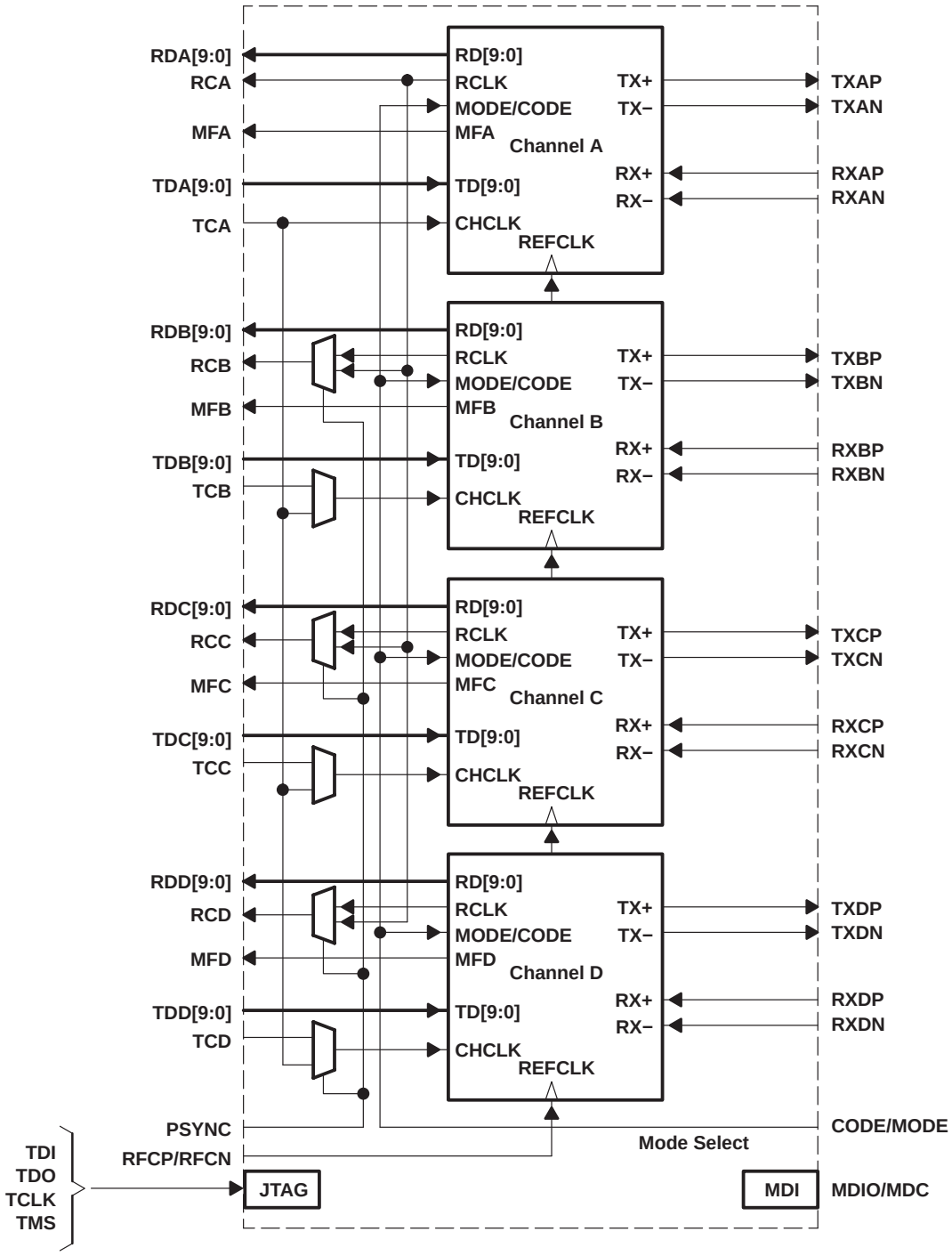


Figure 1−4. TLK3114SA Block Diagram

Figure 1−5 is a more detailed block diagram description of each channel core.

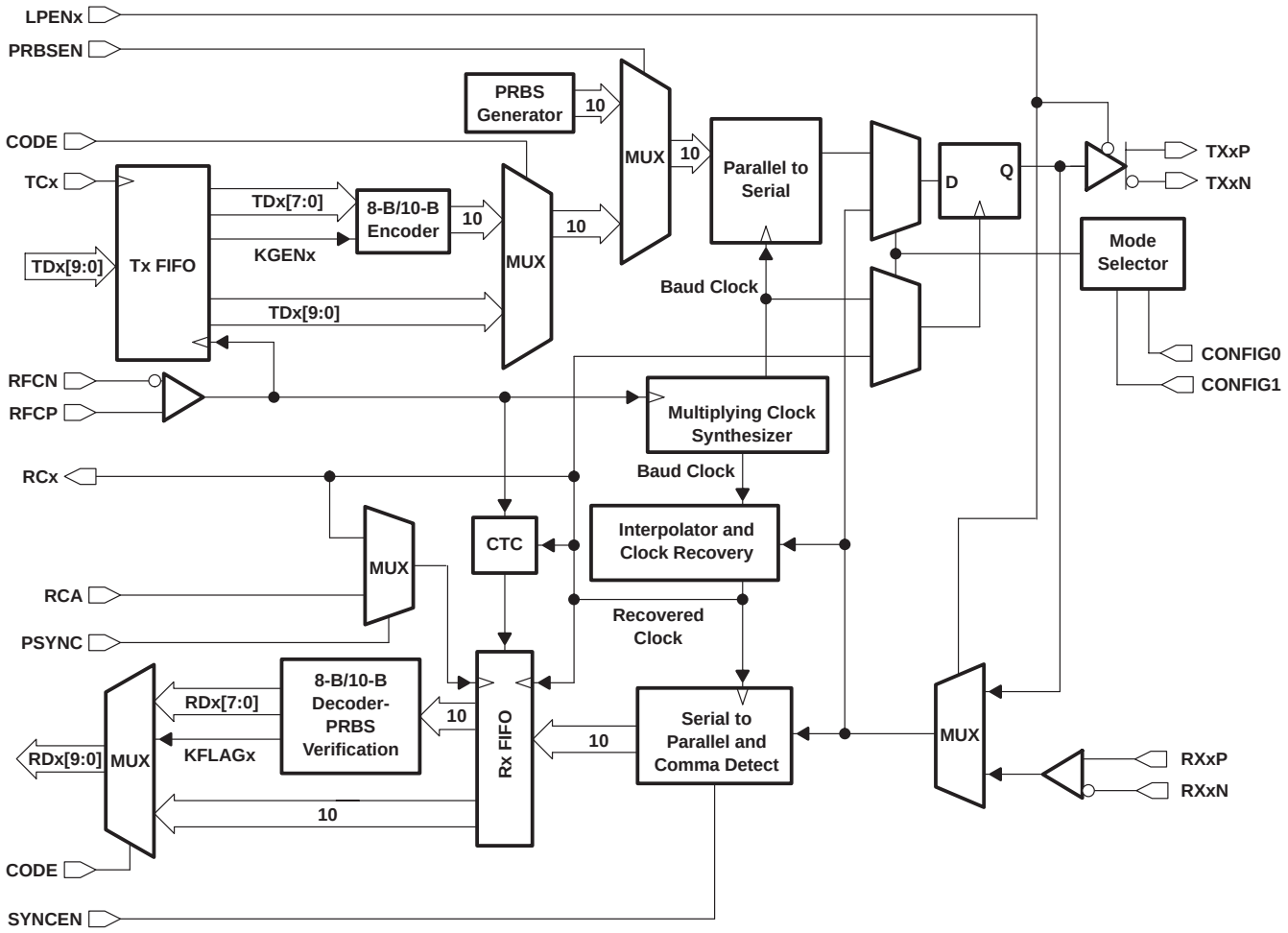


Figure 1−5. Block Diagram of Individual Channel

1.1 Features

- Quad 3.125 Gbps per channel transceiver providing 10-Gbps data throughput
- P802.3ae 10-Gbps Ethernet XGXS compliant including:
  - XGMII parallel interface to MAC and XAUI serial interfaces
  - Clock tolerance compensation with column add/drop
  - XAUI interpacket gap /A/, /K/, and /R/ code generation and stripping
  - Remote and local fault reporting on the XGMII as defined
- MDIO interface
- Selectable synchronized or independent channel operation
- Selectable transmit-only, receiver-only, transceiver, and repeater functions
- Selectable on-chip 8-b/10-b ENDEC
- On-chip receive equalization
- Receiver differential input thresholds 200 mV_{P-P}
- On-chip 100-Ω differential receiver termination

- No external filter capacitors required
- VML serial driver providing PECL-compatible differential signaling with no external components
- Auto-selects between HSTL or SSTL_2 Class 1 I/O with on-chip 50-Ω series termination on outputs
- Able to operate with a single 2.5-V power supply
- On-chip PRBS generation and verification controlled from external terminal
- IEEE 1149.1 JTAG test interface
- Hot-plug protection
- Mainstream 250-nm CMOS technology
- Small-footprint, 19-mm × 19-mm, 289-ball PBGA package

1.2 Ordering Information

Device: TLK3114SAGNT/GPV
GNT and GPV: Plastic ball grid arrays

2 Terminal Descriptions

The TLK3114SA device is available in a 289-terminal MicroStar BGA™ package (GNT/GPV). The terminal layout for the GNT and GPV packages is shown in Figure 2−1. The TLK3114SA pinout is compatible with TLK3104SA board designs.

Pin Out
(Top View)

	A	B	C	D	E	F	G	H	J	K	L	M	N	P	R	T	U	
17	VDDQ	GND	RDB3	VDDQ	GND	RCB	VDDQ	GND	VREF	GND	VDDQ	RCC	GND	VDDQ	RDC3	GND	VDDQ	17
16	MFA	MFB	RDB2	RDB6	RDB9	TCB	TDB5	TDB8	VDDQ	TDC8	TDC5	TCC	RDC9	RDC6	RDC2	MFC	MFD	16
15	VDDQ	GND	RDB1	RDB5	RDB8	TDB2	TDB4	TDB7	TDC9	TDC7	TDC4	TDC2	RDC8	RDC5	RDC1	GND	VDDQ	15
14	RDA9	RDA8	RDB0	VDDQ	GND	TDB1	VDDQ	GND	VDDQ	GND	VDDQ	TDC1	GND	VDDQ	RDC0	RDD8	RDD9	14
13	RDA7	RDA6	RDA5	RDB4	RDB7	TDB0	TDB3	TDB6	TDB9	TDC6	TDC3	TDC0	RDC7	RDC4	RDD5	RDD6	RDD7	13
12	VDDQ	GND	RDA4	RDA3	RDA2	T−GND	T−GND	T−GND	T−GND	T−GND	T−GND	T−GND	RDD2	RDD3	RDD4	GND	VDDQ	12
11	RCA	RDA1	RDA0	VDDQ	GND	T−GND	T−GND	T−GND	T−GND	T−GND	T−GND	T−GND	GND	VDDQ	RDD0	RDD1	RCD	11
10	TCA	TDA9	TDA8	TDA7	TDA6	T−GND	T−GND	T−GND	T−GND	T−GND	T−GND	T−GND	TDD6	TDD7	TDD8	TDD9	TCD	10
9	VDDQ	GND	TDA5	TDA4	TDA3	T−GND	T−GND	T−GND	T−GND	T−GND	T−GND	T−GND	TDD3	TDD4	TDD5	GND	VDDQ	9
8	TDA2	TDA1	TDA0	VDDQ	GND	T−GND	T−GND	T−GND	T−GND	T−GND	T−GND	T−GND	GND	VDDQ	TDD0	TDD1	TDD2	8
7	VDDA	GNDA	GNDA	VDD	GND	T−GND	T−GND	T−GND	T−GND	T−GND	T−GND	T−GND	GND	VDD	GNDA	GNDA	VDDA	7
6	VDDA	RXAN	VDDA	TXAN	GND	T−GND	T−GND	T−GND	T−GND	T−GND	T−GND	T−GND	GND	TXDN	VDDA	RXDN	VDDA	6
5	VDDA	RXAP	VDDA	TXAP	GND	GNDA	GNDA	GND	GND	GND	GNDA	GNDA	GND	TXDP	VDDA	RXDP	VDDA	5
4	GNDA	GNDA	GNDA	VDD	VDD	TXBP	TXBN	VDD	VDD	VDD	TXCN	TXCP	VDD	VDD	GNDA	GNDA	GNDA	4
3	TCLK	TDI	LPENA	LPENB	GNDA	VDDA	VDDA	GND	RFCP	GND	VDDA	VDDA	GNDA	LPENC	LPEND	PADR2	MDIO	3
2	TDO	TMS	CONFIG0	CONFIG1	GNDA	RXBP	RXBN	GND	RFCN	GND	RXCN	RXCP	GNDA	TESTEN	PADR4	PADR3	MDC	2
1	ENABLE	RSTN	PSYNC	SYNCEN	GNDA	VDDA	VDDA	VDD	PRBSEN	VDD	VDDA	VDDA	GNDA	CODE	PADR0	PADR1	DADR0	1
	A	B	C	D	E	F	G	H	J	K	L	M	N	P	R	T	U	

Figure 2−1. TLK3114SA GNT/GPV-Package Terminal Diagram

The terminals are grouped in tables by functionality, such as clocks, serial side data, parallel data, etc. The terminal numbers are also listed for convenient reference.

Table 2−1. Clock Terminals

TERMINAL		XGMII NAME	TYPE	DESCRIPTION
NAME	NUMBER			
RCA	A11	RX_CLK	HSTL/SSTL_2 output	Receive data clock, channel A. The data on RDA(0–9) is output on the rising and falling edges of RCA. When PSYNC is high, RCA acts as the receive clock for all channels. This terminal has internal series termination to provide direct connection to a 50-Ω transmission line.
RCB RCC RCD	F17 M17 U11	N/A	HSTL/SSTL_2 output	Receive data clock, channels B–D. When PSYNC is low, the data on RDx(0–9) is output on the rising and falling edges of the receive clocks. When PSYNC is high, these terminals are duplicates of RCA. These terminals have internal series termination to provide direct connection to a 50-Ω transmission line.
RFCP RFCN	J3 J2	N/A	PECL compatible or LVDS input	Differential reference input clock. This differential pair accepts LVDS- or PECL-compatible signals. When interfacing with 3.3-V PECL, ac-coupling is required. An on-chip 100-Ω termination resistor is placed differentially between the terminals. Internal biasing is provided.
TCA	A10	TX_CLK	HSTL/SSTL_2 input	Transmit data clock, channel A. The data on TDA(0–9) is latched on the rising and falling edges of TCA. When PSYNC is high, TCA acts as the transmit clock for all channels.
TCB TCC TCD	F16 M16 U10	N/A	HSTL/SSTL_2 input	Transmit data clock, channels B–D. When PSYNC is low, the data on TDx(0–9) is latched on the rising and falling edges of the transmit clocks. When PSYNC is high, these terminals are undefined.

Table 2−2. Serial Side Data Terminals

TERMINAL		TYPE	DESCRIPTION
NAME	NUMBER		
RXAP, RXAN RXBP, RXBN RXCP, RXCN RXDP, RXDN	B5, B6 F2, G2 M2, L2 T5, T6	PECL-compatible input	Receive differential pairs, channels A–D. High-speed serial inputs with on-chip 100-Ω differential termination. Each input pair is terminated differentially across an on-chip 100-Ω resistor (see Figure 4−9 and Figure 4−10). These terminals have internal biasing.
TXAP, TXAN TXBP, TXBN TXCP, TXCN TXDP, TXDN	D5, D6 F4, G4 M4, L4 P5, P6	PECL-compatible output	Transmit differential pairs, channels A–D. High-speed serial outputs.

Table 2−3. Parallel Data Terminals

TERMINAL		XGMII NAME	TYPE	DESCRIPTION
NAME	NUMBER			
RDA[0:7]	C11, B11, E12, D12, C12, C13, B13, A13	RXD[0:7]	HSTL/SSTL_2 output	Receive data terminals, channel A. Parallel data on this bus is valid on the rising and falling edges of RCA. These terminals have internal series termination to provide direct connection to a 50-Ω transmission line.
RDA8	B14	RXC0	HSTL/SSTL_2 output	Receive data/K-flag, channel A. When CODE is low, this terminal is the ninth bit of a received 8-b/10-b encoded byte. When CODE is high, this terminal acts as the K-character flag. When this terminal is high, it indicates the data on RDA(0–7) is a valid K-character. Data on this terminal is valid on the rising and falling edges of RCA. This terminal has internal series termination to provide direct connection to a 50-Ω transmission line.
RDA9	A14	N/A	HSTL/SSTL_2 output	Receive data terminal/error detect, channel A. When CODE is low, this terminal is the tenth bit of an 8-b/10-b encoded byte. When CODE is high, this terminal goes high to signify the occurrence of either a disparity error or an invalid code word during the decoding of the received data. Data on this terminal is valid on the rising and falling edges of RCA. This terminal has internal series termination to provide direct connection to a 50-Ω transmission line.
RDB[0:7]	C14, C15, C16, C17, D13, D15, D16, E13	RXD[8:15]	HSTL/SSTL_2 output	Receive data terminals, channels B–D. When PSYNC is low, parallel data on these buses is valid on the rising and falling edges of the recovered data clock (RCB, RCC, or RCD). When PSYNC is high, data on each bus is valid on the rising and falling edges of RCA. These terminals are series terminated to provide direct connection to a 50-Ω transmission line.
RDC[0:7]	R14, R15, R16, R17, P13, P15, P16, N13	RXD[16:23]		
RDD[0:7]	R11, T11, N12, P12, R12, R13, T13, U13	RXD[24:31]		
RDB8 RDC8 RDD8	E15 N15 T14	RXC1 RXC2 RXC3	HSTL/SSTL_2 output	Receive data/K-flag, channels B–D. When PSYNC is low, data on these terminals is valid on the rising and falling edges of the recovered clock (RCB, RCC, or RCD). When PSYNC is high, data on these terminals is valid on the rising and falling edges of RCA. When CODE is low, these terminals are the ninth bit of a received 8-b/10-b encoded byte. When CODE is high, these terminals act as the K-character flag. When asserted high, this indicates the data on RDx[0:7] is a valid K-character. These terminals are series terminated to provide direct connection to a 50-Ω transmission line.
RDB9 RDC9 RDD9	E16 N16 U14	N/A	HSTL/SSTL_2 output	Receive data terminal/error detect, channels B–D. When PSYNC is low, data on these terminals is valid on the rising and falling edges of recovered channel clock (RCB, RCC, RCD). When PSYNC is high, data on these terminals is valid on the rising and falling edges of RCA. When CODE is low, these terminals are the tenth bit of an 8-b/10-b encoded byte. When CODE is high, these terminals provide an error detection flag. The error detect is asserted high to signify the occurrence of either a disparity error or an invalid code word during the decoding of the received data. These terminals have internal series termination to provide direct connection to a 50-Ω transmission line.

Table 2−3. Parallel Data Terminals (Continued)

TERMINAL		XGMII NAME	TYPE	DESCRIPTION
NAME	NUMBER			
TDA[0:7]	C8, B8, A8, E9, D9, C9, E10, D10	TXD[0:7]	HSTL/SSTL_2 input	Transmit data terminals, channel A. Parallel data on this bus is clocked on the rising and falling edges of TCA.
TDA8	C10	TXC0	HSTL/SSTL_2 input	Transmit data/KGEN, channel A. When CODE is low, this terminal is the ninth bit of an 8-b/10-b encoded byte to be transmitted. When CODE is high, this terminal acts as the K-character generator indicator. When this terminal is high, it causes the data on TDA(0−7) to be encoded into a K-character.
TDA9	B10	N/A	HSTL/SSTL_2 input	Transmit data terminal, channel A. When CODE is low, this terminal is the tenth bit of an 8-b/10-b encoded byte. When CODE is high, this terminal is ignored.
TDB[0:7]	F13, F14, F15, G13, G15, G16, H13, H15	TXD[8:15]	HSTL/SSTL_2 input	Transmit data terminals, channels B–D. When PSYNC is low, parallel data on this bus is clocked on the rising and falling edges of the transmit channel clock (TCB, TCC, TCD). When PSYNC is high, data on these buses is clocked on the rising and falling edges of TCA.
TDC[0:7]	M13, M14, M15, L13, L15, L16, K13, K15	TXD[16:23]		
TDD[0:7]	R8, T8, U8, N9, P9, R9, N10, P10	TXD[24:31]		
TDB8 TDC8 TDD8	H16 K16 R10	TXC1 TXC2 TXC3	HSTL/SSTL_2 input	Transmit data/KGEN, channels B–D. When PSYNC is low, data on these terminals is clocked on the rising and falling edges of the transmit channel clock (TCB, TCC, or TCD). When PSYNC is high, data on these terminals is clocked on the rising and falling edges of TCA. When CODE is low, these terminals are the ninth bit of an 8-b/10-b encoded byte to be transmitted. When CODE is high, these terminals act as the K-character generator indicator. When driven high, these terminals cause the data on TDx(0−7) to be encoded into a K-character.
TDB9 TDC9 TDD9	J13 J15 T10	N/A	HSTL/SSTL_2 input	Transmit data terminal, channels B–D. When PSYNC is low, data on these terminals is clocked on the rising and falling edges of the transmit channel clock (TCB, TCC, TCD). When PSYNC is high, data on these terminals is clocked on the rising and falling edges of TCA. When CODE is low, these terminals are the tenth bit of an 8-b/10-b encoded byte. When CODE is high, these terminals are ignored.

Table 2−4. JTAG Test Port Interface

TERMINAL		TYPE	DESCRIPTION
NAME	NUMBER		
TCLK	A3	LVTTL input	JTAG clock. TCLK clocks state information and test data into and out of the device during the operation of the test port.
TDI	B3	LVTTL input†	JTAG input data. TDI serially shifts test data and test instructions into the device during the operation of the test port.
TDO	A2	LVTTL output	JTAG output data. TDO serially shifts test data and test instructions out of the device during operation of the test port. When the JTAG port is not in use, TDO is in a high-impedance state.
TMS	B2	LVTTL input†	JTAG mode select. TMS controls the state of the internal test-port controller.

† With an internal pullup resistor

Table 2−5. Management Data Interface

TERMINAL		TYPE	DESCRIPTION
NAME	NUMBER		
DADR0	U1	LVTTL input	Management MMD address. DADR0 is the externally set device address, which configures PHY XS or DTE XS according to Table 3−11.
MDC	U2	LVTTL input	Management data clock. MDC is the clock reference for the transfer of management data to and from the protocol device.
MDIO	U3	LVTTL I/O	Management data I/O. MDIO is the bidirectional serial data path for the transfer of management data to and from the protocol device.
PADR(0−4)	R1, T1, T3, T2, R2	LVTTL input	Management PHY address. Device address PADR(0−4) is the externally set physical address given to this device used to distinguish one device from another.

Table 2−6. Miscellaneous Terminals

TERMINAL		TYPE	DESCRIPTION
NAME	NUMBER		
CODE	P1	LVTTL input†	Encode enable. When CODE is high, the 8-b/10-b encoder and decoder is enabled.
CONFIG0 CONFIG1	C2, D2	LVTTL input‡	Configuration terminals. These terminals put the device under one of the three operation modes: 00 = Transceiver mode 01 = Transmit-only mode 10 = Receive-only mode 11 = Repeater mode
ENABLE	A1	LVTTL input†	Standby enable. When this terminal is held low, the device is in a low-power state. When high, the device operates normally.
LPEN(A−D)	C3, D3, P3, R3	LVTTL input‡	Internal loop enable, channels A−D. When high, the serial output for each channel is internally looped back to its serial input.
MF(A−D)	A16, B16, T16, U16	LVTTL output	Multifunction outputs, channels A−D. The functions of these terminals are enabled via the MDIO. Currently defined functions are: Terminal indicates 1 for HSTL, 0 for SSTL_2 signaling (default), LOS (loss of signal) for each channel, COMMA_DET (K28.5 character detected) for each channel, and PRBS_STATUS (pseudorandom bit stream test status) for each channel.
PRBSEN	J1	LVTTL input‡	PRBS enable. When this terminal is asserted high, the PRBS generator and comparator circuits are inserted into the transmit and receive data paths on all channels. PRBS_PASS is indicated on the MFx terminals once they are enabled using MDIO.
PSYNC	C1	LVTTL input‡	Channel synchronization enable. When PSYNC is high, all transmit data is latched on the rising and falling edges of TCA and all receive data is valid on the rising and falling edges of RCA.
RSTN	B1	LVTTL input†	Chip reset (FIFO clear). Pulling this terminal low recenters the transmit skew buffers, receive channel synchronization FIFOs, and resets MDIO flags.
SYNCEN	D1	LVTTL input†	Comma detect enable. When this terminal is high, comma detection and byte alignment for all channels are enabled.
TESTEN	P2	LVTTL input‡	Test mode enable. This terminal is used for manufacturing test. This terminal must be left unconnected or tied low.

† With an internal pullup resistor
‡ With an internal pulldown resistor

Table 2−7. Voltage Supply and Reference Terminals

TERMINAL		TYPE	DESCRIPTION
NAME	NUMBER		
GND	B9, B12, B15, B17, E5, E6, E7, E8, E11, E14, E17, H2, H3, H5, H14, H17, J5, K2, K3, K5, K14, K17, N5, N6, N7, N8, N11, N14, N17, T9, T12, T15, T17	Ground	Digital logic ground. Supply reference for core logic and SSTL_2 Class 1 buffers.
GNDA	A4, B4, B7, C4, C7, E1, E2, E3, F5, G5, L5, M5, N1, N2, N3, R4, R7, T4, T7, U4	Ground	Analog ground. Supply reference for analog circuitry.
T-GND	F6−F12, G6−G12, H6−H12, J6−J12, K6−K12, L6−L12, M6−M12	Ground	Thermal grounds. Electrically connected to GND, these terminals provide a thermal path for heat dissipation.
V_{DD}	D4, D7, E4, H1, H4, J4, K1, K4, N4, P4, P7	Supply	Core supply (2.5 V). Digital logic power. Provides power for all digital circuitry.
V_{DDA}	A5, A6, A7, C5, C6, F1, F3, G1, G3, L1, L3, M1, M3, R5, R6, U5, U6, U7	Supply	Analog voltage supply (2.5 V). Provides power for all analog circuitry.
V_{DDQ}	A9, A12, A15, A17, D8, D11, D14, D17, G14, G17, J14, J16, L14, L17, P8, P11, P14, P17, U9, U12, U15, U17	Supply	HSTL/SSTL_2 Class 1 supply voltage. Nominally 1.5 V for HSTL or 2.5 V for SSTL_2 Class 1.
VREF	J17	Input	Input voltage reference for HSTL/SSTL_2 Class 1 I/O

3 Detailed Description

The TLK3114SA device has four operational interface modes controlled by the states of terminals CODE and PSYNC. These operational interface modes are listed in Table 3−1.

Table 3−1. Operational Interface Modes

CODE	PSYNC	DESCRIPTION
Low	Low	Four independent serializer/deserializers (serdes)
Low	High	Four synchronized serdes
High	Low	Four independent transceivers with on-chip 8-b/10-b encode/decode
High	High	10-gigabit ethernet XGMII extended sublayer (XGXS) transceiver

3.1 Serdes Modes

When CODE is deasserted, the TLK3114SA device performs serialization and deserialization of encoded data across four ten-bit interfaces (TBI) similar to that done in fibre channel and 802.3z gigabit ethernet serdes devices. The channels can be synchronized to allow use of one transmit data clock and one receive data clock.

3.2 10-Gbps Ethernet Transceiver Modes

When CODE and PSYNC are asserted, the TLK3114SA device supports the 32-bit data path, 4-bit control, 10-gigabit media independent interface (XGMII), and full encoding scheme specified in the IEEE 802.3ae 10-Gigabit Ethernet standard. In these modes, the TLK3114SA device performs the serialization/deserialization and channel synchronization function of an extended auxiliary unit interface (XAUI), also specified in the IEEE 802.3ae 10 Gigabit Ethernet standard.

3.3 Parallel Interface Clocking

Two clocking choices are selectable via the PSYNC terminal detailed in Table 3−2. Under channel sync mode (PSYNC is high), TCA is used as the transmit data clock for all four channels. Under independent channel mode (PSYNC is low), each channel uses its own transmit data clock (TCA−TCD) to latch data into the TLK3114SA device. A data FIFO is placed in the transmit data path to resolve any phase difference between the transmit data clocks and differential reference clock, RFCP/N.

Table 3−2. Parallel Interface Clocking Modes

PSYNC	PARALLEL INTERFACE CLOCKING OPERATION
Low	Independent channel mode. TC[A−D]/RC[A−D] clock in/out each individual channel
High	Channel sync mode. TCA/RCA clock in/out all channels of data

On the receive data path, in independent channel mode, the data for each channel is output referenced to each channel's extracted receive clock. In channel sync mode, the data on all channels are synchronized and output referenced to the extracted receive clock for channel A, RCA. A FIFO is enabled in the parallel receive data path on each channel to compensate for channel skew and clock phase tolerance differences between the recovered clocks for each channel and the receive output clock, RCA. This FIFO has a total depth of 11 bytes.

3.4 Parallel Interface Data

Two data mode choices are selectable via the CODE terminal detailed in Table 3−3. In serdes mode, the transmit data bus for each channel accepts 10-bit wide 8-b/10-b encoded data at the TDx[0:9] terminals. Data is latched on the rising and falling edge of the transmit data clock. The 8-b/10-b encoded data is then phase aligned to the reference clock (RFCP/RFCN), serialized, then transmitted sequentially beginning with bit 0 (TDx0) over the differential high-speed serial transmit terminals.

In serdes mode, the receive data bus for each channel outputs 10-bit wide 8-b/10-b encoded data on RDx[0:9]. The 8-b/10-b encoded data input to the differential high-speed serial receive terminals is deserialized with the first bit (bit 0) output on RDx0 and the last bit (bit 9) output on RDx9. Data is output relative to both the rising and falling edges of the receive clock.

Table 3−3. Parallel Data Modes

CODE	PARALLEL INTERFACE DATA OPERATION
Low	Serdes mode. On-chip 8-b/10-b encoder/decoder is disabled. Data on TDx[0:9] and RDx[0:9] is treated as 8-b/10-b encoded data.
High	Transceiver mode. Enables 8-b/10-b encode/decode for each channel. Data TDx[0:7] and RDx[0:7] are treated as uncoded data. TDx8 is used as the K-character generator control. RDx8 is the K-character indicator to the host device. Data on TDx9 is ignored. RDx9 goes high on either a disparity or code error.

In transceiver mode, the transmit data bus for each channel accepts 8-bit wide parallel data at the TDx[0:7] terminals. Data is sampled on the rising and falling edges of the transmit clock as shown in Figure 3−1. The data is first aligned to the reference clock (RFCP/RFCN), then 8-b/10-b encoded and passed to the serializer. The generation of K-characters on each channel is controlled by TDx8 (KGEN). When KGEN is asserted along with the 8 bits of data TDx[0:7], the appropriate 8-b/10-b K-character is transmitted.

In transceiver mode, the receive data bus for each channel outputs an 8-bit wide parallel data on RDx[0:7]. Reception of K-characters is reported on RDx8 (KFLAG). When KFLAG is asserted, the 8 bits of data on RDx[0:7] must be interpreted as a K-character. If an error is uncovered in decoding the data, KFLAG and RDx9 (RX_ER) are asserted and 0xFE is placed on the receive data bus for that channel.

3.5 Transmit Data Bus Timing

For each channel, the transmitter portion of the TLK3114SA device latches the data on transmit data bus TDx[0:9] on both the rising and falling edges of the transmit data clock, as shown in Figure 3−1. Depending on the state of the PSYNC terminal, the transmit data clock is either TCA (channel sync mode) or the individual transmit channel clocks, TCA−TCD (independent channel mode). When in the channel sync mode, signals on TCB, TCC, and TCD are ignored.

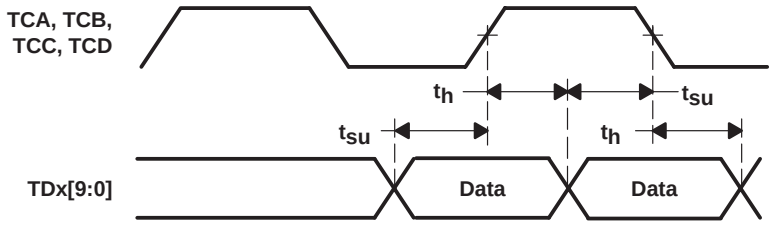


Figure 3−1. Transmit Interface Timing

3.6 Transmission Latency

For each channel, the data transmission latency of the TLK3114SA device is defined as the delay from the rising or falling edge of the selected transmit clock when valid data is on the transmit data terminals to the serial transmission of bit 0, as shown in Figure 3−2. The minimum latency ($T_{LATENCY}$) is 71 bit times; the maximum is 120 bit times. There are approximately 20 bit times required for the 8-b/10-b encoder.

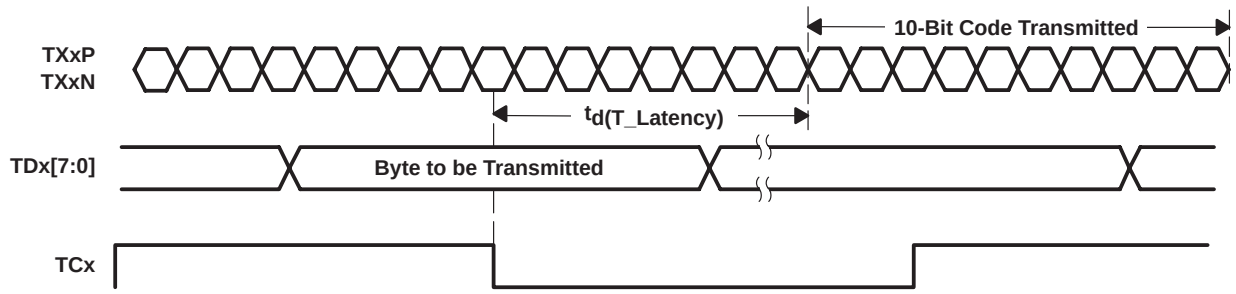


Figure 3−2. Transmitter Latency

3.7 Channel Clock to Serial Transmit Clock Synchronization

The TLK3114SA device requires an external differential reference clock, RFCP/N, for the on-chip phase-locked loop (PLL) and the clock/data recovery loop. To compensate for arbitrary clock phase tolerance differences between the reference clock and the data aligned to the transmit clock, a small FIFO in the parallel transmit data path on each channel is employed. This FIFO has a depth of four bytes.

The reference clock and the transmit data clock(s) are assumed to be from a common source and only phase misaligned due to different path delays as shown in Figure 3−3 and Figure 3−4. The reference clock is multiplied in frequency 10x to produce the internal serialization clock. The internal serialization clock is used to clock out the serial transmit data.

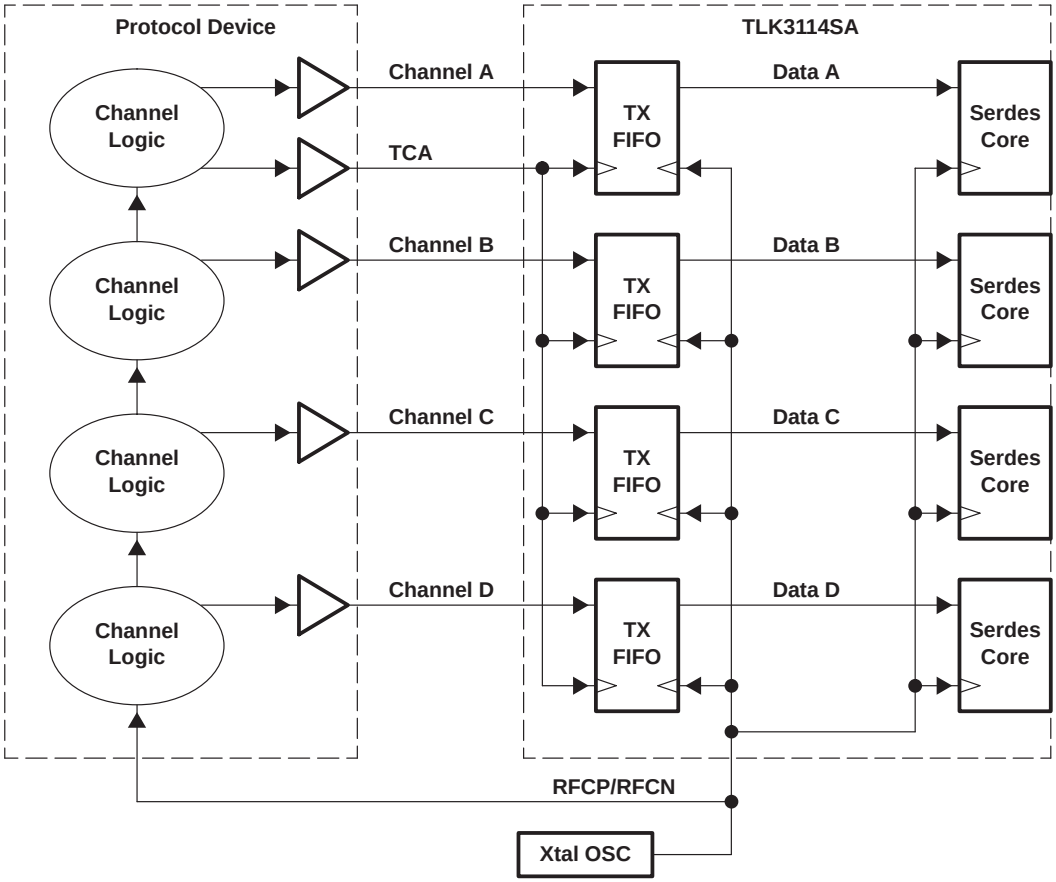


Figure 3−3. Transmit and Reference Clock Relationship (Channel Sync Mode)

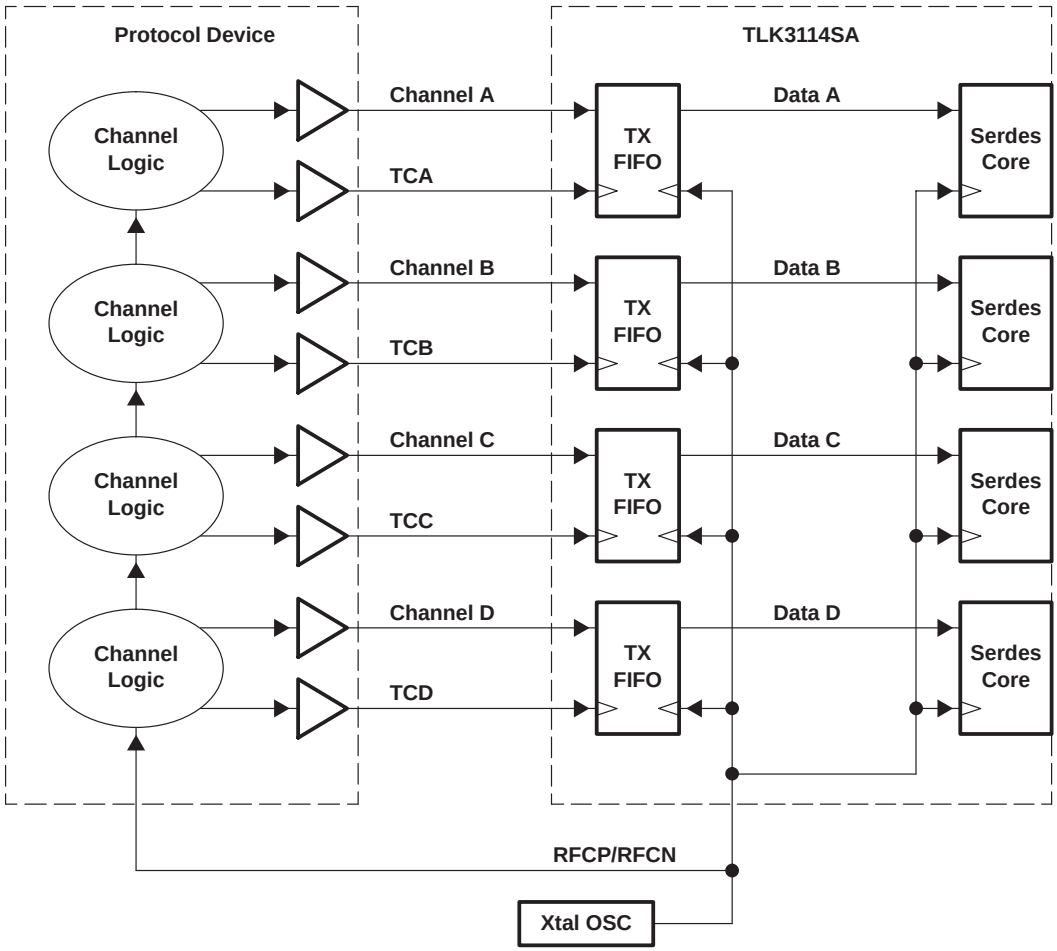


Figure 3−4. Transmit and Reference Clock Relationship (Independent Channel Mode)

3.8 Receive Data Bus Timing

For each channel, the receiver portion of the TLK3114SA device outputs the recovered deserialized data on the receive data bus TDx[0:9] on both the rising and falling edges of the receive data clock, as shown in Figure 3−5. Depending on the state of PSYNC terminal the receive data clock is either RCA (channel sync mode) or the individual receive channel clocks, RCA−RCD (independent channel mode). Terminals RCB, RCC, and RCD are also strobed to match RCA in channel sync mode.

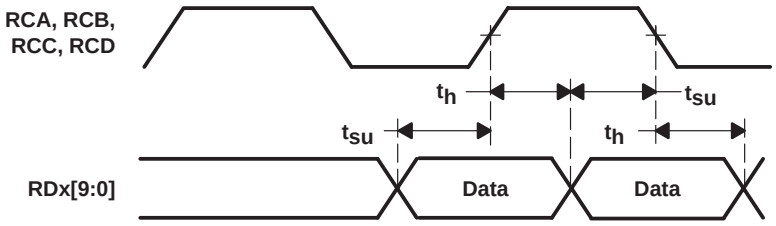


Figure 3−5. Receive Interface Timing

3.9 Data Reception Latency

For each channel, the serial-to-parallel data latency is the time from when the first bit arrives at the receiver input until it is output in the aligned parallel word with RDx0 received as first bit, as shown in Figure 3−6. The minimum latency ($R_{LATENCY}$) is 84 bit times; the maximum is 225 bit times. The 8-b/10-b encoder, channel de-skew, and CTC all contribute to the maximum latency.

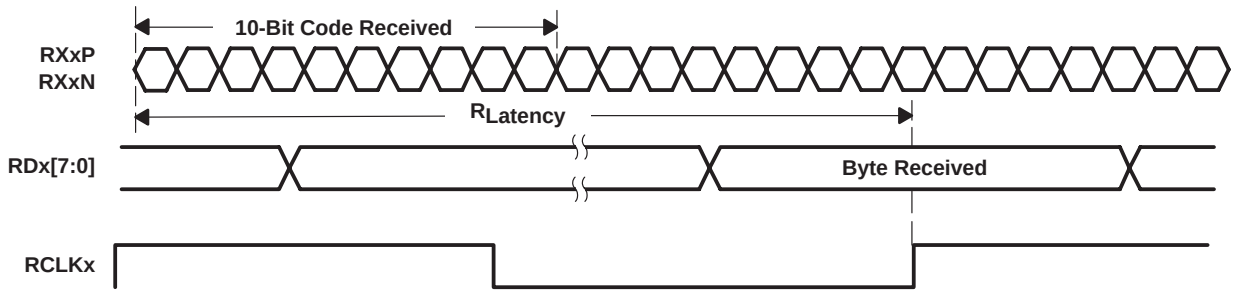


Figure 3−6. Receiver Latency

3.10 Auto Detectable HSTL/SSTL_2 Class 1 I/O

The transmit and receive data buses of the TLK3114SA device are compatible with both high-speed transfer logic (HSTL) supply and stub series terminated logic 2 (SSTL_2) Class 1 buffers. The TLK3114SA device determines which buffer technology to use by sensing the voltage level on the V_{DDQ} supply terminals at power up. If the voltage on the V_{DDQ} supply is between 2.3 V and 2.7 V, the TLK3114SA device provides the necessary drive current to meet SSTL_2 Class 1 requirements. If the voltage on the V_{DDQ} supply is between 1.4 V and 2 V, the TLK3114SA device provides HSTL compatible signaling. During normal operation, the voltage level on the V_{DDQ} terminals must not change.

All HSTL/SSTL_2 Class 1 outputs are series terminated to provide direct connection to a 50-Ω transmission line signaling environment (see Figure 4−10 and Figure 4−11).

3.11 8-b/10-b Encoder

All true serial interfaces require a method of encoding to ensure sufficient transition density for the receiving PLL to acquire and maintain lock. The encoding scheme also maintains the signal dc balance by keeping the number of 1s and 0s the same, which allows for ac-coupled data transmission. The TLK3114SA device uses the 8-b/10-b encoding algorithm that is used by fibre channel and gigabit ethernet. This provides good transition density for clock recovery and improves error checking. The 8-b/10-b encoder/decoder function is enabled for all four channels by the assertion of the CODE terminal. When enabled, the TLK3114SA device internally encodes and decodes the data such that the user reads and writes actual 8-bit data on each channel.

When enabled, the 8-b/10-b encoder converts 8-bit wide data to a 10-bit wide encoded data character to improve its transition density. This transmission code includes D-characters, used for transmitting data, and K-characters, used for transmitting protocol information. Each K- or D-character code word can also have both a positive and a negative disparity version. The disparity of a code word is selected by the encoder to balance the running disparity of the serialized data stream.

The generation of K-characters to be transmitted on each channel is controlled by TDx8 (KGEN). When KGEN is asserted along with the 8 bits of data TDx[0:7], an 8-b/10-b K-character is transmitted. Similarly, reception of K-characters is reported by RDx8 (KFLAG). When KFLAG is asserted, the 8 bits of data on RDx[0:7] must be interpreted as a K-character. The TLK3114SA device transmits and receives all 12 valid K-characters defined in Table 3−4. Table 3−5 provides additional transmit data control coding and descriptions that have been proposed for 10 gigabits per second ethernet. Data patterns put on TDx[0:7], other than those defined in Table 3−4 when TDx8 is asserted, result in an invalid K-character being transmitted, which results in a code error at the receiver.

Table 3−4. Valid K-Codes

K-CODE	TDX8 OR RDX8	DATA BUS (RDX[7:0] OR TDX[7:0])	ENCODED K-CODE		K-CODE DESCRIPTION
			NEGATIVE RUNNING DISPARITY	POSITIVE RUNNING DISPARITY	
00 through FF	0	dddddddd	dddddddddd	dddddddddd	Normal data
K28.0	1	000 11100	001111 0100	110000 1011	IdleO/busy
K28.1†	1	001 11100	001111 1001	110000 0110	IdleE/busy
K28.2	1	010 11100	001111 0101	110000 1010	
K28.3	1	011 11100	001111 0011	110000 1100	Channel alignment precursor
K28.4	1	100 11100	001111 0010	110000 1101	
K28.5†	1	101 11100	001111 1010	110000 0101	IdleE/not busy
K28.6	1	110 11100	001111 0110	110000 1001	
K28.7†	1	111 11100	001111 1000	110000 0111	Code violation or parity error
K23.7	1	111 10111	111010 1000	000101 0111	IdleO/not busy
K27.7	1	111 11011	110110 1000	001001 0111	SOP(S)
K29.7	1	111 11101	101110 1000	010001 0111	EOP(T)
K30.7	1	111 11110	011110 1000	100001 0111	

† A comma is contained within this K-code.

Table 3−5. Valid XGMII Channel Encodings

DATA BUS (TDX[7:0]† OR RDX[7:0]‡)	TDX8§ OR RDX8¶	DESCRIPTION
00 through FF	0	Normal data transmission
00 through 06	1	Reserved
07	1	Idle
08 through 9B	1	Reserved
9C	1	Sequence (only valid in channel A)
9D through FA	1	Reserved
FB	1	Start (only valid in channel A)
FC	1	Reserved
FD	1	Terminate
FE	1	Transmit error propagation
FF	1	Reserved

† XGMII names: TDA[7:0] = TXD[7:0], TDB[7:0] = TXD[15:8], TDC[7:0] = TXD[23:16], and TDD[7:0] = TXD[31:24]
‡ XGMII names: RDA[7:0] = RXD[7:0], RDB[7:0] = RXD[15:8], RDC[7:0] = RXD[23:16], and RDD[7:0] = RXD[31:24]
§ XGMII names: TDA8 = TXC0, TDB8 = TXC1, TDC8 = TXC2, and TDD8 = TXC3
¶ XGMII names: RDA8 = RXC0, RDB8 = RXC1, RDC8 = RXC2, and RDD8 = RXC3

3.12 Comma Detect and 8-b/10-b Decoding

When parallel data is clocked into a parallel-to-serial converter, the byte boundary that was associated with the parallel data is lost in the serialization of the data. When the serial data is received and converted to parallel format again, a method is needed to be able to recognize the byte boundary. Generally, this is accomplished through the use of a synchronization pattern. This is a unique pattern of 1s and 0s that either cannot occur as part of valid data or is a pattern that repeats at defined intervals. 8-b/10-b encoding contains a character called the comma (b'0011111' or b'1100000') which is used by the comma detect circuit to align the received serial data back to its original byte boundary. The decoder detects the K28.5 comma, generating a synchronization signal aligning the data to their 10-bit boundaries for decoding. It then converts the data back into 8-bit data. It is important to note that the comma can be either (b'0011111') or the inverse (b'1100000') depending on the running disparity. The TLK3114SA decoder detects both patterns. Comma detect is not active in PRBS mode.

The reception of K-characters is reported by the assertion of RDx8 (KFLAG) on each channel. When a code word error or running disparity error is detected in the decoded data on a channel, RDx9 (ERROR DETECT) and KFLAG are asserted and an 0xFE is placed on the receive data bus for that channel, as shown in Table 3−6. When a loss of signal (LOS) is detected on the differential receive inputs, a local fault is reported on the receive data bus (see Section 3.15, Fault Detection and Reporting). The LOS signal can be disabled using MDIO (see Table 3−13).

Table 3−6. Receive Data Controls

EVENT	RECEIVE DATA BUS (RDX[7:0])	KFLAG (RDX8)	ERROR DETECT (RDX9)
Normal data	XX	0	0
Normal K-character	Valid K-code (see Table 3−4)	1	0
Loss of signal	See Table 3−7		
Code word error or running disparity error	FE	1	1

3.13 Channel Initialization and Synchronization

The TLK3114SA device has a synchronization state machine, which is responsible for handling link initialization and synchronization for each channel. The initialization and synchronization state diagram is provided in Figure 3−7. The status of any channel can be monitored by reading MDIO registers 4.24 and 5.24, bits 3:0.

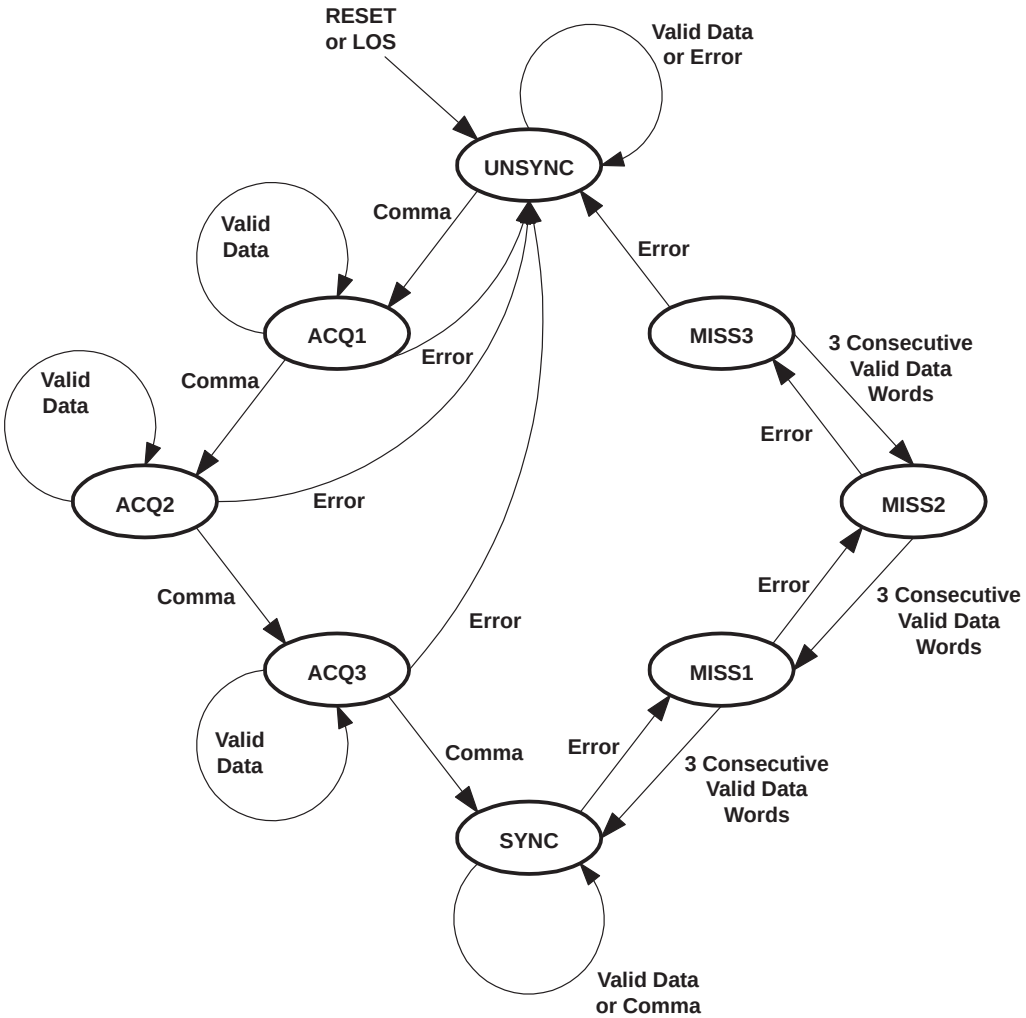


Figure 3−7. Channel Synchronization State Machine

3.13.1 Channel State Descriptions

UNSYNC—This is the initial state for each channel upon device power up or reset. If a LOS condition is detected, the channel state is set to UNSYNC. In this state, the TLK3114SA device has the comma detect circuit active and makes code word alignment adjustments based on the position of a comma in the incoming data stream. While in this state, the TLK3114SA device sets the lane sync bit to 0 for the particular channel in MDIO registers 4.24 and 5.24, bits 3:0, indicating the lane is not synchronized. The channel state transitions to the ACQ1 state upon the detection of a comma.

NOTE: When the lane sync bit equals 0, it causes a local fault to be output on the receive data bus.

ACQ1—During this state the comma detect circuit is active but code word realignment is disabled. The TLK3114SA device remains in this state until either a comma is detected in the same code word alignment position as found in state UNSYNC or a decode error is encountered. While in this state, the lane sync bit for the particular channel remains deasserted indicating the lane is not synchronized. A decode or running disparity error returns the channel state to UNSYNC. A detected comma causes the channel state to transition to ACQ2.

NOTE: When the lane sync bit equals 0, it causes a local fault to be output on the receive data bus.

ACQ2—During this state, the comma detect circuit is active but code word realignment is disabled. The TLK3114SA device remains in this state until either a comma is detected in the same code word alignment position as found in state UNSYNC or a decode error is encountered. While in this state, the lane sync bit for the particular channel remains deasserted indicating the lane is not synchronized. A decode or running disparity error returns the channel state to UNSYNC. A detected comma causes the channel state to transition to ACQ3.

NOTE: When the lane sync bit equals 0, it causes a local fault to be output on the receive data bus.

ACQ3—During this state, the comma detect circuit is active but code word realignment is disabled. The TLK3114SA device remains in this state until either a comma is detected or a decode error encountered. While in this state, the lane sync bit for the particular channel remains deasserted indicating the lane is not synchronized. A decode or running disparity error returns the channel state to UNSYNC. A detected comma causes the channel state to transition to SYNC.

NOTE: When the lane sync bit equals 0, it causes a local fault to be output on the receive data bus.

SYNC—This is the normal state for receiving data. When in this state, the TLK3114SA device sets the lane sync bit to 1 for the particular channel in MDIO registers 4.24 and 5.24, bits 3:0, indicating the lane has been synchronized. During this state the comma detect circuit is active but code word realignment is disabled. A decode or running disparity error causes the channel state to transition to MISS1.

MISS1—When entering this state an internal error counter is cleared. If the next three consecutive codes are decoded without error, the channel state reverts back to SYNC. If a decode or running disparity error is detected, the channel state transitions to MISS2.

MISS2—When entering this state an internal error counter is cleared. If the next three consecutive codes are decoded without error, the channel state reverts back to MISS1. If a decode or running disparity error is detected, the channel state transitions to MISS3.

MISS3—When entering this state an internal error counter is cleared. If the next three consecutive codes are decoded without error, the channel state reverts back to MISS1. If a decode or running disparity error is detected, the channel state transitions to UNSYNC.

3.14 End-of-Packet Error Detection

Because of their unique data patterns, /A/ (K28.3), /K/ (K28.5), and /T/ (K29.7) catch running disparity errors that may have propagated undetected from previous codes in a packet. Running disparity errors detected by these control codes at the end of the packets cause the previous data codes to be reported as errors (0xFE) to allow the protocol device to reject the packet (see Figure 3−8).

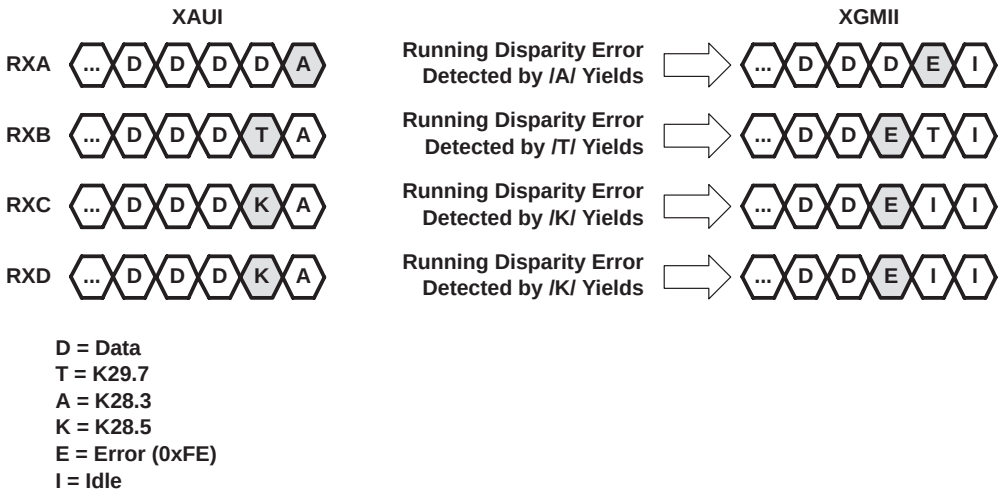


Figure 3−8. End-of-Packet Error Detection

3.15 Fault Detection and Reporting

The TLK3114SA device detects and reports local faults as well as forwards both local and remote faults as defined in the IEEE P802.3ae to aid in fault diagnosis. All faults detected by the TLK3114SA device, such as LOS detect, are reported as local faults to the upper layer protocols, as shown in Table 3−7. Once a local fault is detected in the TLK3114SA device, bit 7 in MDIO registers 4.1 and 5.1 is set. Fault sequences received by the TLK3114SA device, either on the transmit data bus or on the high-speed receiver terminals, are forwarded without change to the MDIO registers in the TLK3114SA device.

The TLK3114SA device reports a fault by outputting a K28.4 (0x9C) on channel A, 0x00 on channels B and C, and either 0x01 for local faults or 0x02 for remote faults on the receive data terminals for channel D. Forwarding of remote faults is handled as a normal transmission.

Table 3−7. Local and Remote Fault Sequences

CHANNEL DESCRIPTION		LOCAL FAULT	REMOTE FAULT
Channel A†	RDA[7:0]	Sequence‡	Sequence‡
	RDA8	1	1
	RDA9	1	1
Channel B	RDB[7:0]	00	00
	RDB8	0	0
	RDB9	0	0
Channel C	RDC[7:0]	00	00
	RDC8	0	0
	RDC9	0	0
Channel D	RDD[7:0]	01	02
	RDD8	0	0
	RDD9	0	0

† Channels A, B, C, and D are equal to the XGMII lanes 0, 1, 2, and 3, respectively.
‡ The sequence character is equal to 0x9C.

3.16 Receive Synchronization and Skew Compensation

When the TLK3114SA device is configured in channel sync mode, a FIFO is enabled in the parallel receive data path on each channel to compensate for channel skew and clock phase tolerance differences between the recovered clocks for each channel and the receive output clock, RCA, as is shown in Figure 3−9. This FIFO has a depth of 11 bytes.

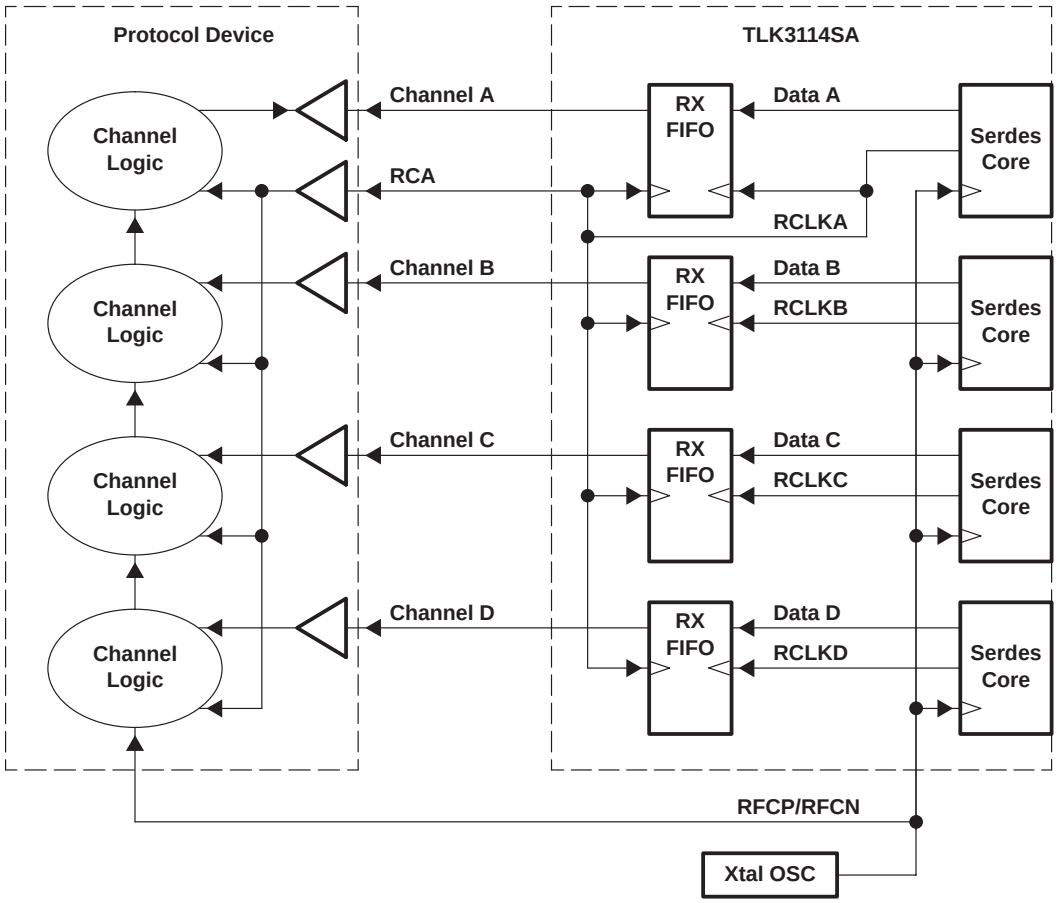


Figure 3−9. Receive and Reference Clock Relationship (Synchronized Channel Modes)

The de-skew of the four channels into a single column of data is accomplished by alignment of the receive FIFOs on each channel to a K28.3 K-character sent during the inter-packet gap (IPG) between data packets or during initial link synchronization. The K28.3 code (referred to as the A or alignment code) is transmitted on the first column following the end of the data packet as shown in Figure 3−12.

The column deskew state machine is provided in Figure 3−10. The status of column alignment can be monitored by reading bit 12 of MDIO registers 4.24 or 5.24 for global alignment, or bits 3:0 of MDIO registers 4.24 or 5.24 for particular channels. Bit 4 of MDIO registers 23, 4.32775, and 5.32775 indicates when a realignment has occurred.

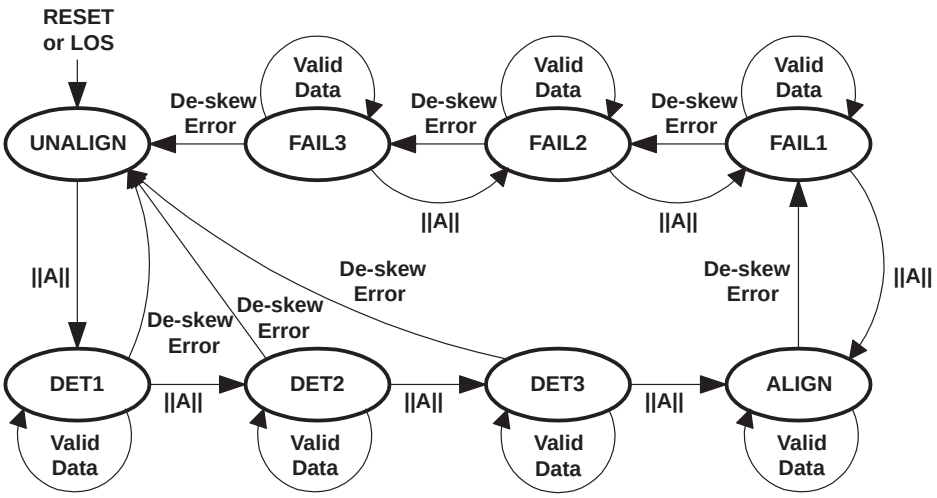


Figure 3−10. Column De-Skew State Machine

3.16.1 Column State Descriptions

UNALIGN—This is the initial state for the column state machine upon device power up or reset. If any of the channel state machines are set to UNSYNC, the column state is set to UNALIGN. In this state, the column state machine searches for alignment character codes (K28.3 or /A/) on each channel and aligns the FIFO pointers on each channel to the /A/ character code. While in this state, the column alignment sync bit is set to 0 in MDIO registers 4.24 and 5.24, bit 12, indicating the column is not aligned. The column state transitions to the DET1 state upon the detection and alignment of /A/ character codes in all four channels.

> **NOTE:** When the XGXS lane alignment bit equals 0, it causes a local fault to be output on the receive data bus.

DET1—During this state, the alignment character code detect circuit is active on each channel but the column realignment is disabled. The column state machine remains in this state looking for a column of alignment character codes. If an incomplete alignment column is detected (alignment character codes not found on all channels), the column state machine transitions to state UNALIGN. While in this state, the column alignment sync bit is set to 0 in MDIO registers 4.24 and 5.24, bit 12, indicating the column is not aligned. Detection of a complete alignment column causes the column state machine to transition to state DET2.

> **NOTE:** When the XGXS lane alignment bit equals 0, it causes a local fault to be output on the receive data bus.

DET2—During this state, the alignment character code detect circuit is active on each channel but the column realignment is disabled. The column state machine remains in this state looking for a column of alignment character codes. If an incomplete alignment column is detected (alignment character codes not found on all channels), the column state machine transitions to state UNALIGN. While in this state, the column alignment sync bit is set to 0 in MDIO registers 4.24 and 5.24, bit 12, indicating the column is not aligned. Detection of a complete alignment column causes the column state machine to transition to state DET3.

> **NOTE:** When the XGXS lane alignment bit equals 0, it causes a local fault to be output on the receive data bus.

DET3—During this state, the alignment character code detect circuit is active on each channel but the column realignment is disabled. The column state machine remains in this state looking for a column of alignment character codes. If an incomplete alignment column is detected (alignment character codes not found on all channels), the column state machine transitions to state UNALIGN. While in this state, the column alignment sync bit is set to 0 in MDIO registers 4.24 and 5.24, bit 12, indicating the column is not aligned. Detection of a complete alignment column causes the column state machine to transition to state ALIGN.

> **NOTE:** When the XGXS lane alignment bit equals 0, it causes a local fault to be output on the receive data bus.

ALIGN—This is the normal state for receiving data. When in this state, the column state machine sets the column alignment sync bit to 1 in MDIO registers 4.24 and 5.24, bit 12, indicating all channels are aligned. During this state, the alignment character code detect circuit is active on each channel but the column realignment is disabled. If a complete alignment column is not detected in the correct position within the IPG, the column state machine transitions to state FAIL1.

FAIL1—When in this state, the column alignment sync bit is 1 in MDIO registers 4.24 and 5.24, bit 12. During this state, the alignment character code detect circuit is active on each channel but the column realignment is disabled. If a complete alignment column is not detected in the correct position within the IPG, the column state machine transitions to state FAIL2.

FAIL2—When in this state, the column alignment sync bit is 1 in MDIO registers 4.24 and 5.24, bit 12. During this state, the alignment character code detect circuit is active on each channel but the column realignment is disabled. If a complete alignment column is not detected in the correct position within the IPG, the column state machine transitions to state FAIL3.

FAIL3—When in this state, the column alignment sync bit is 1 in MDIO registers 4.24 and 5.24, bit 12. During this state, the alignment character code detect circuit is active on each channel but the column realignment is disabled. If complete alignment column is not detected in the correct position within the IPG, the column state machine transitions to state UNALIGN.

3.17 Independent Channel Mode

When the TLK3114SA device is configured in independent channel mode, the recovered clocks for each channel are used to output the received data on the parallel interface. Thus, as is shown in Figure 3−11, in the independent channel modes, no FIFO is enabled.

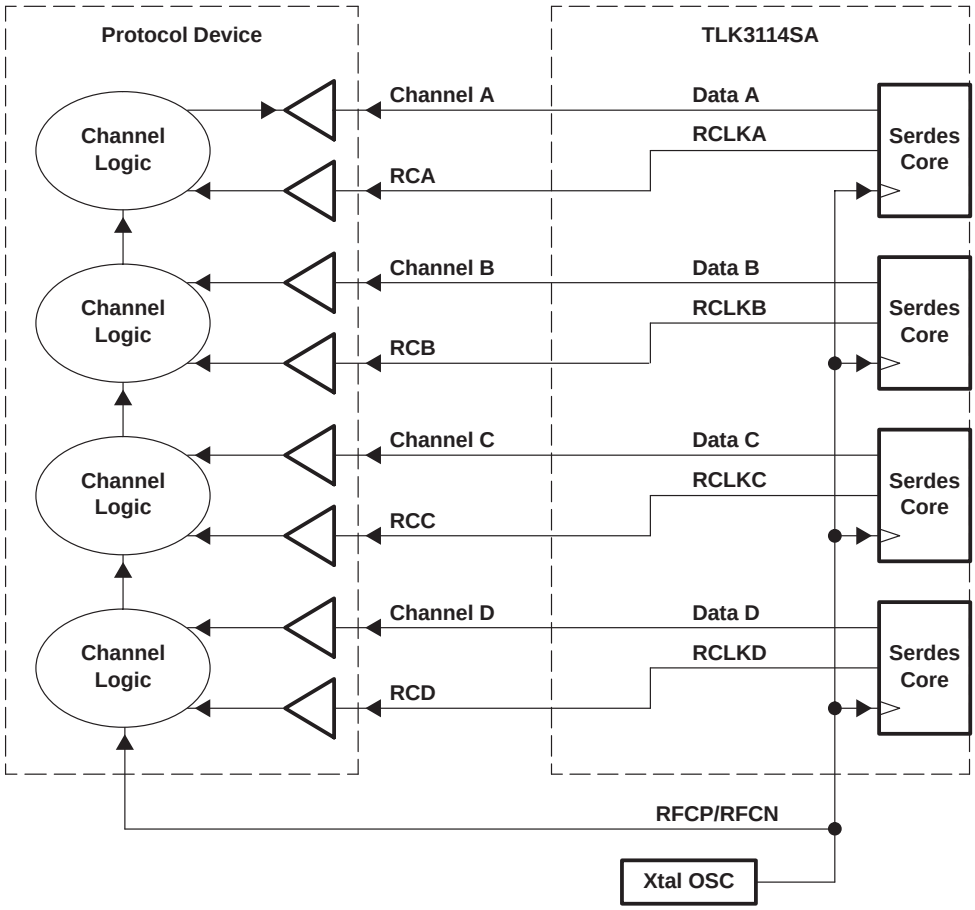


Figure 3−11. Receive and Reference Clock Relationship (Independent Channel Modes)

3.18 Inter-Packet Gap Management

When in the 10-Gbps ethernet XGXS operational mode, the TLK3114SA device replaces the idle codes (see Table 3−5) during the IPG with the necessary codes to perform all channel alignment, byte alignment, and clock tolerance compensation as defined in IEEE 802.3ae, subclause 48.2.4.2. According to clause 46, a valid packet must begin on channel A. However, due to variable packet sizes, the IPG can begin on any channel. The TLK3114SA device replaces idle codes latched on the same TCA (TX_CLK) clock edge as the end of packet code with /K/ codes (as shown in Figure 3−12).

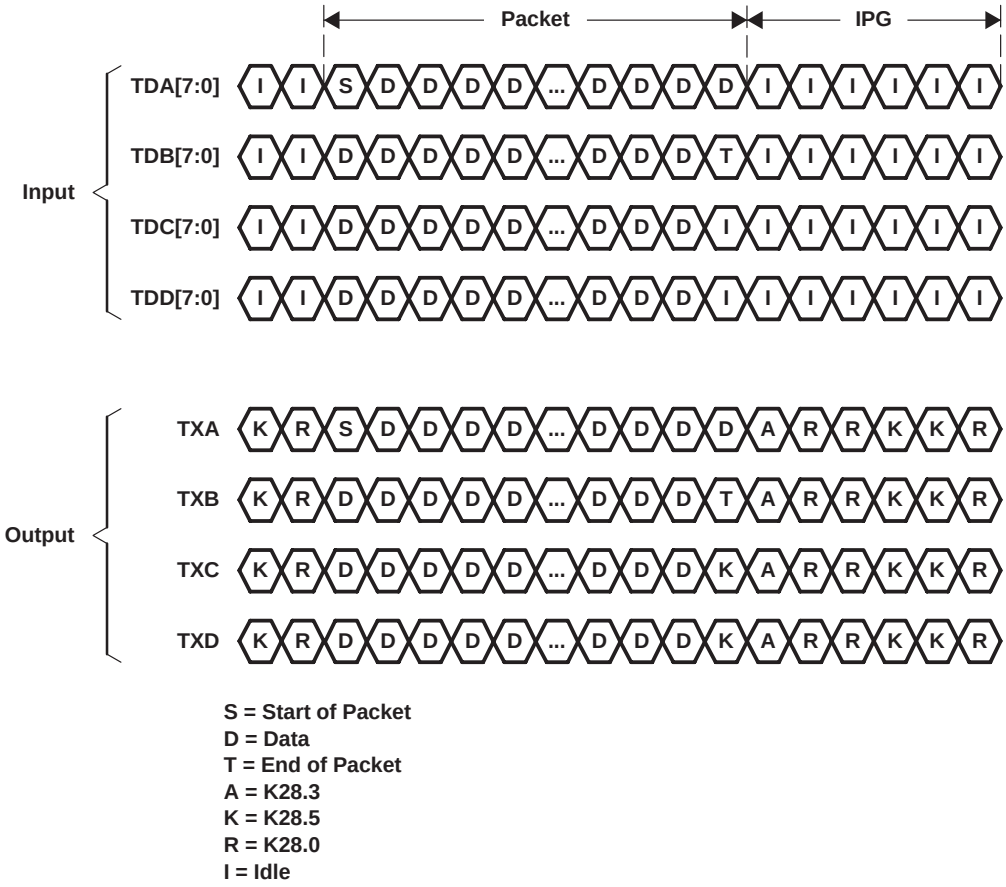


Figure 3−12. Inter-Packet Gap Management

The subsequent idles in the IPG are replaced by columns of channel alignment codes (K28.3), byte alignment codes (K28.5), or clock tolerance compensation codes (K28.0). The state machine, which governs the IPG replacement procedure, is illustrated in Figure 3−13, with notation defined in Table 3−8. Note that any IPG management state transitions to send data if the IPG is terminated.

The repetition of the A pattern on each serial channel allows the FIFOs to remove or add the required phase delay to align the data from all four channels for output on a single edge of the receive clock for channel A, RCA, as shown in Figure 3−14.

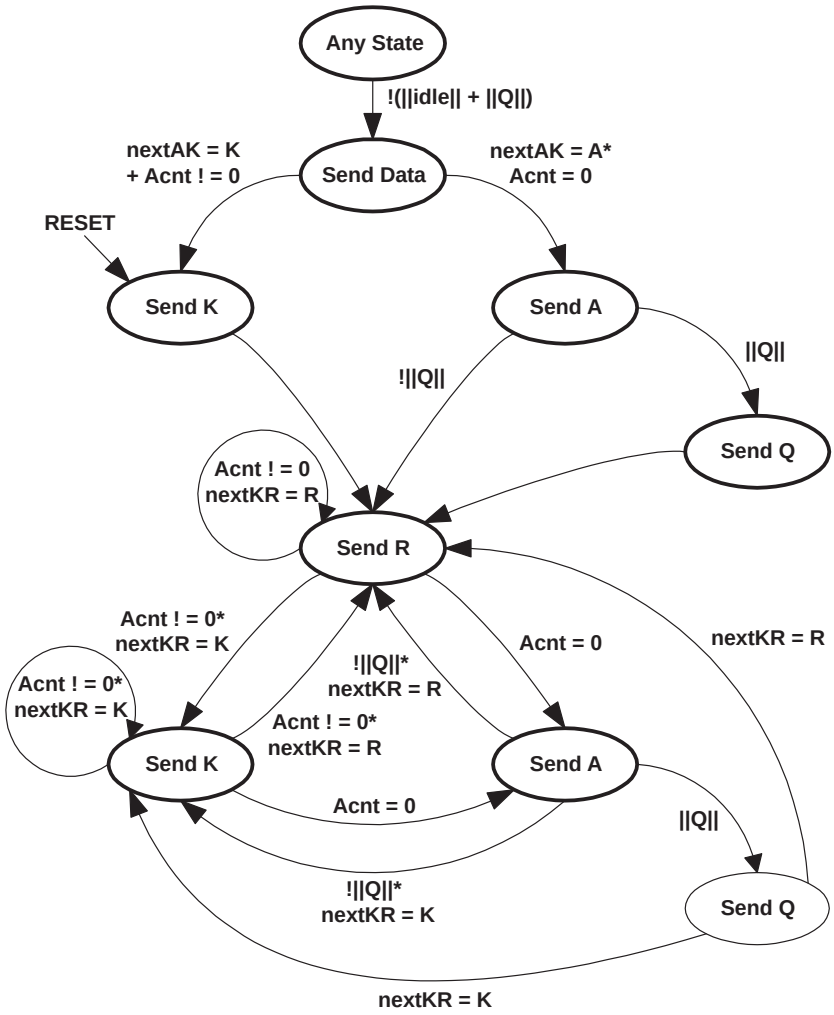


Figure 3−13. IPG Management State Machine

Table 3−8. IPG Management State Machine Notation

SYMBOL	DEFINITION
||idle||	XGMII idle. 0x07 on TD[A:D].
||Q||	Link status message: K28.4, Dx.y, Dx.y, Dx.y
nextAK	A Boolean variable. It takes the value K when an A is sent at the beginning of the IPG and the value A when a K is sent at the beginning of the IPG. Its initial value is K.
Acnt	When an A character is sent, variable Acnt is loaded with a random number such that 16 ≤ Acnt ≤ 31. Acnt is decremented each time a column of non-A characters is generated.
nextKR	A randomly-generated Boolean that can assume the value K or R.

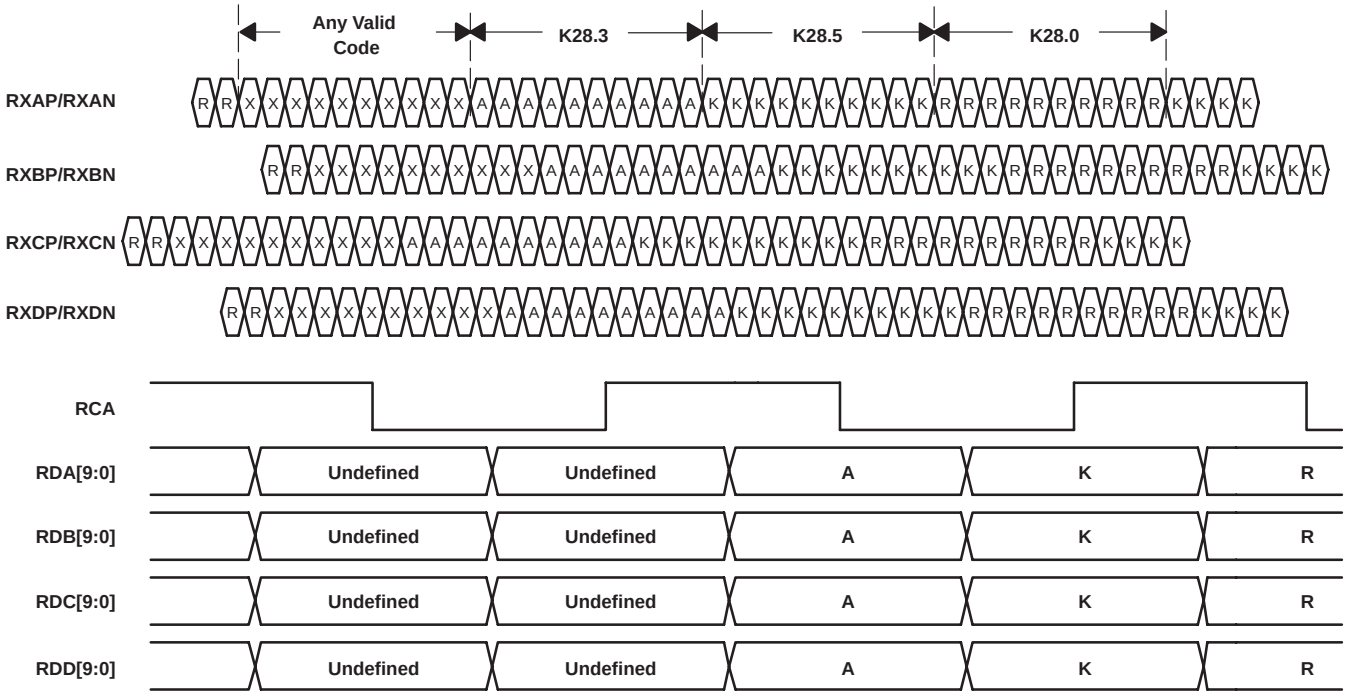


Figure 3−14. Channel Synchronization Using Alignment Code

3.19 Clock Tolerance Compensation (CTC)

The XAUI interface is defined to allow for separate clock domains on each side of the link. Though the reference clocks for two devices on a XAUI link have the same specified frequencies, there are slight differences within those limits that, if not compensated for, lead to over- or underruns of the FIFOs on the receive data path. The TLK3114SA device provides compensation for these differences in reference clock frequencies via the insertion or the removal of /R/ characters on all channels, as shown in Figure 3−15 and Figure 3−16. Bit 11 of MDIO register 16 allows enabling of the CTC, as noted in Table 3−18.

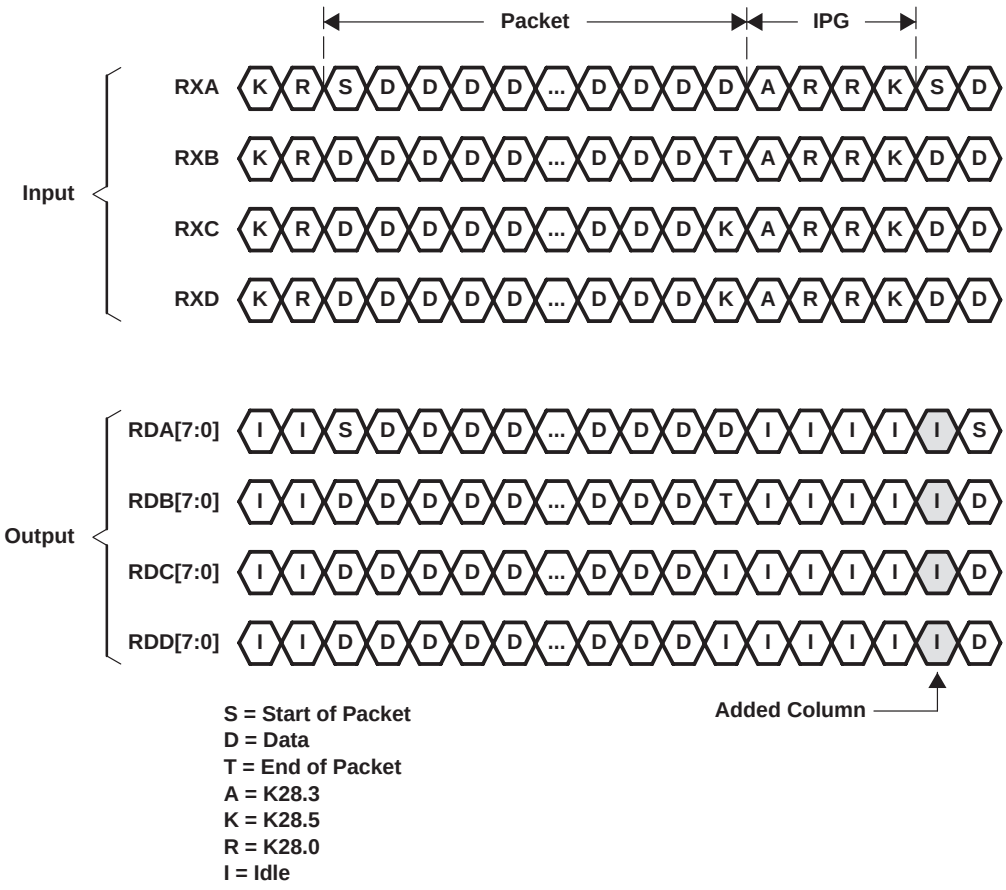


Figure 3−15. Clock Tolerance Compensation: Add

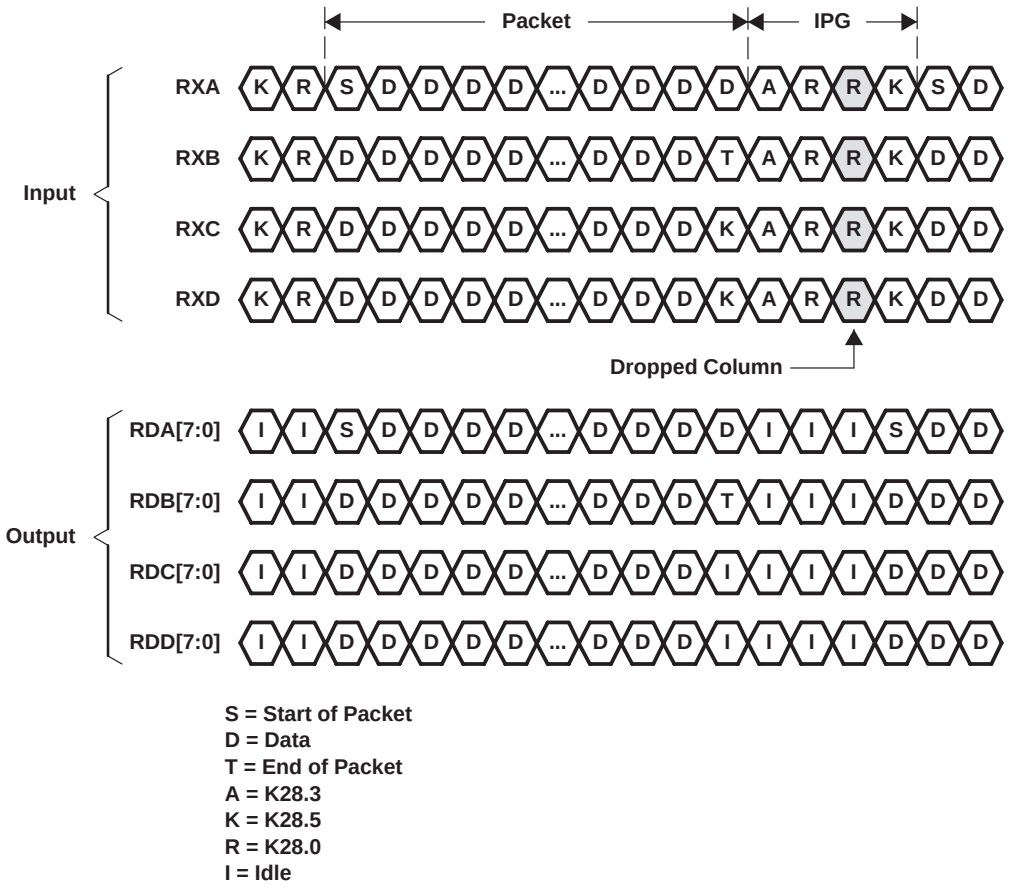


Figure 3−16. Clock Tolerance Compensation: Drop

The /R/ code is disparity neutral, allowing its removal or insertion without affecting the current running disparity of each channel's serial stream.

The clock tolerance compensation circuit also converts XAUI A, K, and R characters to XGMII idles, as illustrated in Figure 3−16.

3.20 Parallel-to-Serial Shift Register

The parallel-to-serial shift register on each channel takes in 10-bit wide data from either the 8-b/10-b encoders, if enabled, or directly from the transmit data bus and converts it to a serial stream. The shift register is clocked by the internally generated bit clock, which is 10 times the reference clock (RFCP/RFCN) frequency. The least significant bit (LSB) for each channel is transmitted first.

3.21 Serial-to-Parallel Shift Register

For each channel, serial data is received on the RXxP/RXxN terminals. The interpolator and clock recovery circuit locks to the data stream if the clock to be recovered is within ±100 PPM of the internally generated bit rate clock. The recovered clock retimes the input data stream. The serial data is then clocked into the serial-to-parallel shift registers. If enabled, the 10-bit wide parallel data is then fed into 8-b/10-b decoders. If the TLK3114SA device is configured in one of the synchronized channel modes, the parallel data for each channel is fed into a FIFO buffer where the output is synchronized to RCA. If the TLK3114SA device is configured in one of the independent channel modes, the parallel data for each channel is output synchronized to each channel's recovered clock.

Transmitting data across PCB or cables attenuates the high frequency content of the signal. This reduces the timing margin for the receiver and clock recovery circuits. The TLK3114SA device applies a filter at the receiver to invert the effects of the interconnect, or equalize and recover some of the lost margin. This maximizes the receiver's ability to recover transmitted data.

3.22 High-Speed VML Output Driver

The high-speed data output driver is implemented using voltage mode logic that offers PECL-compatible differential pair for a 100-Ω differential impedance environment with no external components. The line can be directly coupled or ac coupled. Refer to Figure 4−8 and Figure 4−9 for termination details.

Both current mode logic (CML) and PECL drivers require external components to provide a rising edge (CML) or a falling edge (PECL). The disadvantage of the external edge control is a limited edge rate due to package and line parasitics. In contrast, a VML driver drives and controls both the rising and falling edges inside the package and therefore provides optimum performance for increased speed requirements. Furthermore, the VML driver controls the output voltage swing and adjusts automatically for varying load conditions. The PECL-compatible output provides a nominal 850 mV (singled-ended) swing centered at $V_{DDA}/2$. The receiver input contains internal biasing for ac-coupling. The receiver internal circuitry sets the common mode voltage to $2xV_{DDA}/3$.

When transmitting data across long lengths of PCB trace or cable, the high frequency content of the signal is attenuated due to the skin effect of the media. This causes a smearing of the data eye when viewed on an oscilloscope. The net result is reduced timing margins for the receiver and clock recovery circuits. In order to provide equalization for the high frequency loss, the differential swing is increased or preemphasized for the bit immediately following a transition and subsequently reduced or deemphasized for run lengths greater than one, as shown in Figure 3−17. This provides additional high frequency energy to compensate for PCB or cable loss. The level of the preemphasis is programmable via bits 4 and 5 of MDIO registers 16−20. Users can control the strength of the preemphasis to optimize for a specific system requirement. There are two control bits in the user-defined registers of MDIO to set the preemphasis level, as shown in Table 3−9. See also Table 3−18 for MDIO settings.

Table 3−9. Programmable Preemphasis

PRE1 (Bit 4) REGISTERS 16−20	PRE2 (Bit 5) REGISTERS 16−20	PREEMPHASIS LEVEL ($V_{OD}(p)/ V_{OD}(d)-1$)†
0	0	30%
1	0	20%
0	1	10%
1	1	Preemphasis disabled

† $V_{OD}(p)$: Magnitude of the voltage swing when there is a transition in the data stream.
$V_{OD}(d)$: Magnitude of the voltage swing when there is no transition in the data stream.

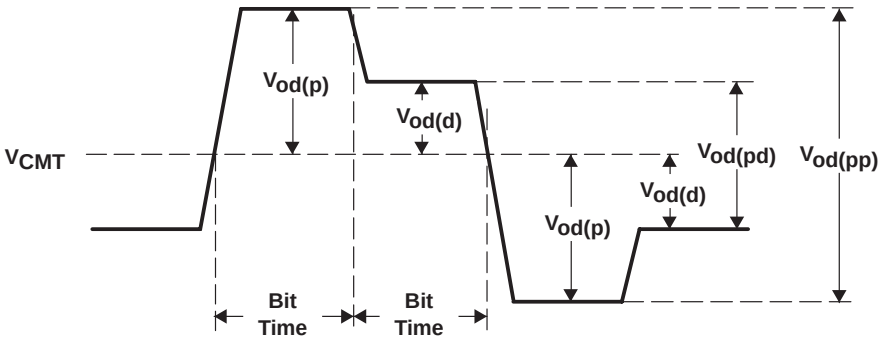


Figure 3−17. Output Differential Voltage Under Preemphasis

3.23 Device Configuration

The TLK3114SA device has four operational configurations controlled by two configuration terminals, CONFIG0 and CONFIG1. These configurations are listed in Table 3−10 and controlled by the MDIO interface (see Table 3−18). When the device is put in a certain mode, unused circuit blocks are powered down to conserve the system power.

Table 3−10. Device Configuration

CONFIG0	CONFIG1	CONFIGURATION
Low	Low	Full-duplex transceiver mode—normal operation (default after reset).
Low	High	Transmit-only mode—data on high-speed data inputs is ignored. Receive data bus is in a high-impedance state.
High	Low	Receive-only mode—high-speed data outputs are in a high-impedance state. Data on the transmit data bus is ignored.
High	High	Repeater mode—recovered serial data and clock are sent back out the transmit serial output.

While transceiver, transmit-only, and receive-only modes are straightforward, the repeater mode of operation is shown in Figure 3−18. The received serial data is recovered by the extracted clock and is then sent back out on the transmit serial output. The data eye opens both vertically and horizontally.

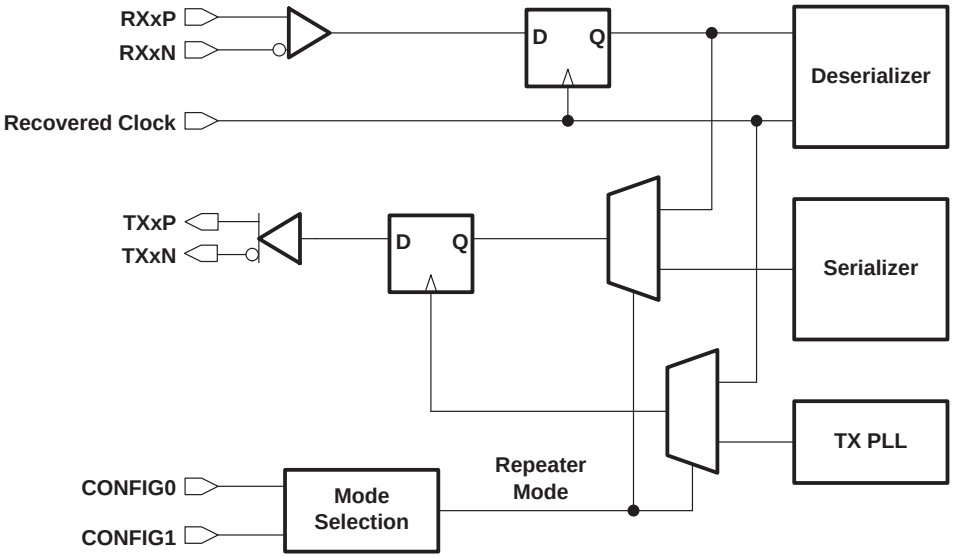


Figure 3−18. Repeater-Mode Block Diagram

3.24 PRBS Generator

The TLK3114SA device has a built-in 2^7-1 PRBS self-test function available on each channel. The PRBS data pattern represents a worst case data recovery task compared to any 8-b/10-b data pattern combination and is, therefore, a sufficient test for the link and jitter tolerance. The self-test function is enabled by asserting the PRBSEN terminal or setting bit 2 (PRBS enable) of MDIO channel configuration registers 16−20, 4.32768−4.32772, or 5.32768−5.32772. When the self-test function is enabled, PRBS is generated and fed into the 10-bit parallel-to-serial converter input register. Data on the transmit data bus is ignored during the PRBS test mode. The PRBS pattern is then fed through the transmit circuitry as if it were normal data and sent out to the transmitter. The output can be sent to a BERT (bit error rate tester), the receiver of another TLK3114SA channel, or can be looped back to the receive input of the same channel. Since the PRBS is not really random but a predetermined sequence of 1s and 0s, the data can be captured and checked for errors by a BERT.

Result reporting of the PRBS test (PRBS_PASS) is available on each receive channel multifunction (MF[A−D]) terminal. To enable the report of the PRBS tests, please refer to bits 10 and 9 of MDIO register 16, 4.32768, or 5.32768. If SYNCEN is high, then PRBS_PASS latches low on the first occurrence of a bit error. SYNCEN low releases the latch function on PRBS_PASS. MDIO comma detect settings do not affect the latching function.

3.25 MDIO Management Interface

The TLK3114SA device supports the MDIO interface as defined in clauses 22 and 45 of the IEEE 802.3ae Ethernet specification. The MDIO allows register-based management and control of the serial links. Normal operation of the TLK3114SA device is possible without use of this interface since all of the essential signals necessary for operations are accessible via the device terminals. However, some additional features are accessible only through the MDIO.

The MDIO management interface consists of a bidirectional data path (MDIO) and a clock reference (MDC). The timing required to read from the internal registers 0−31 is shown in Figure 3−19. The timing required to write to the internal registers 0−31 is shown in Figure 3−20. The port address is defined by the external inputs PADR(0−4).

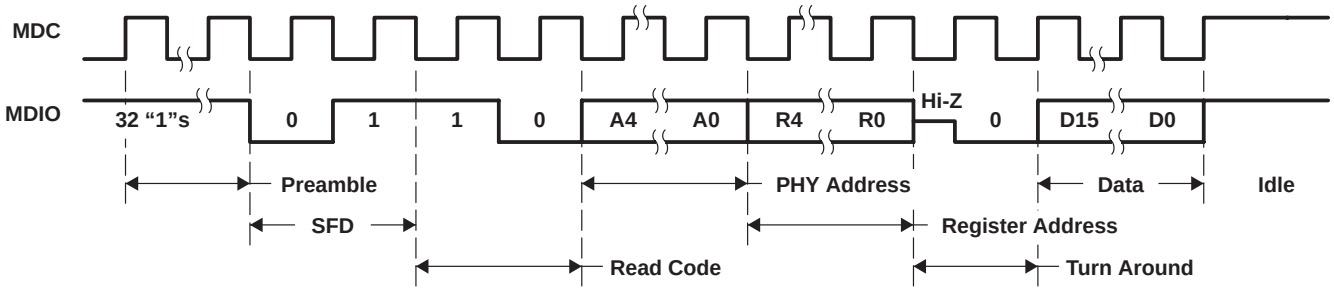


Figure 3−19. Management Interface Read Timing

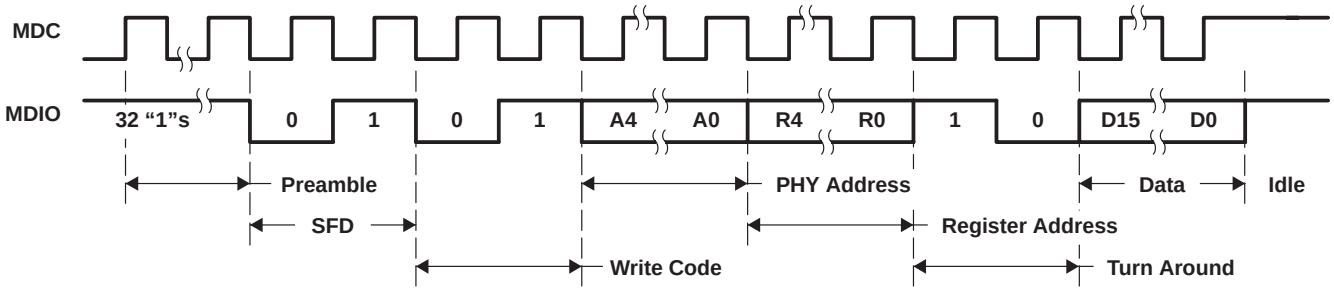


Figure 3−20. Management Interface Write Timing

The extended register address space transactions are orthogonal to register 0−31 transactions, distinguished by the ST bytes. Extended address space registers are denoted X.Y, where X designates the device address and Y designates the register number. The permitted device addresses are shown in Table 3−11. The DADR0 bit is defined by an external input, while the DADR[4:1] bits are predetermined. Write transactions that address an invalid register or device or a read-only register are ignored. Read transactions that address an invalid register return a 0. Read transactions that address an invalid device are ignored.

Timing for an address transaction is shown in Figure 3−21. The timing required to write to the internal registers is shown in Figure 3−22. The timing required to read from the internal registers is shown in Figure 3−23. The timing required to read from the internal registers and then increment the active address for the next transaction is shown in Figure 3−24.

Table 3−11. MDIO Device Address

DADR(4:1)	DADR0	DEVICE MODE
0010	0	PHY XS
0010	1	DTE XS

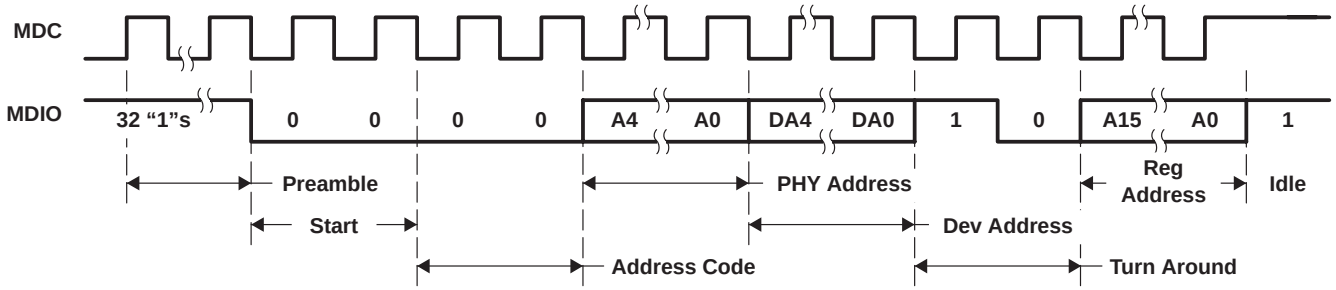


Figure 3−21. Management Interface Extended Space Address Timing

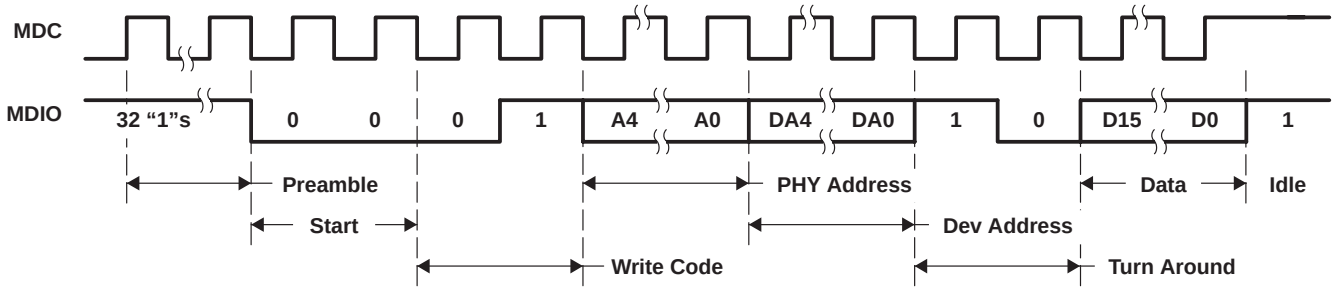


Figure 3−22. Management Interface Extended Space Write Timing

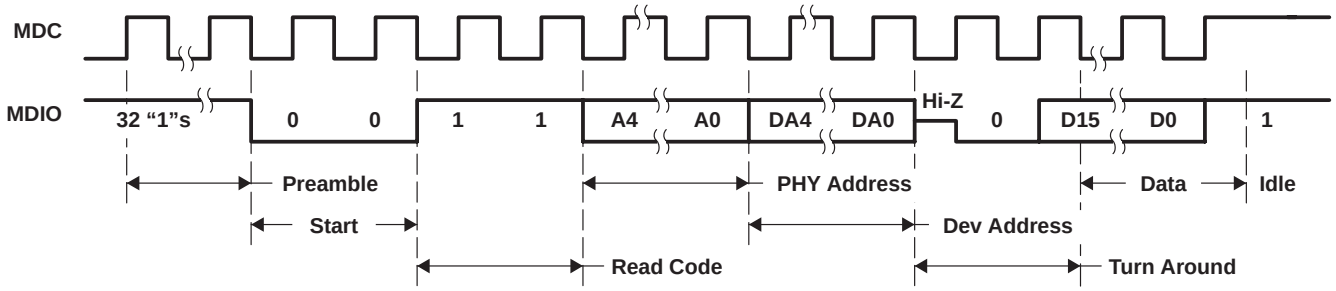


Figure 3−23. Management Interface Extended Space Read Timing

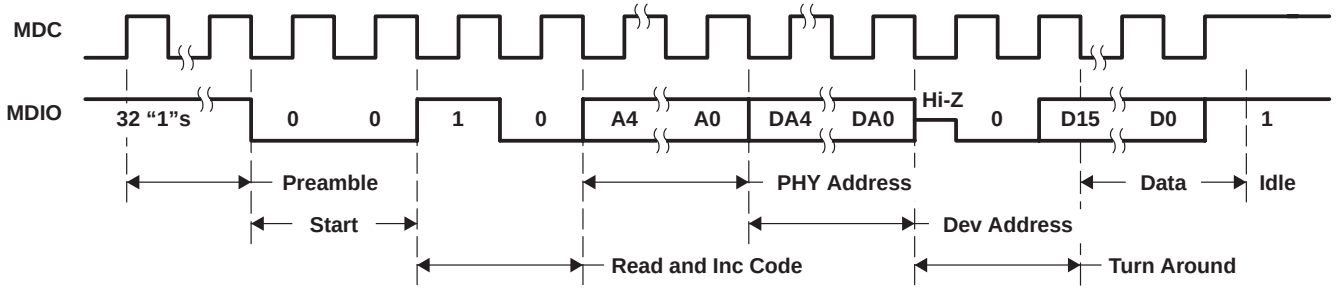


Figure 3−24. Management Interface Extended Space Read and Increment Timing

The IEEE 802.3 Clause 22 and Clause 45 specifications define many of the registers and additional registers have been implemented for expanded functionality. The IEEE-defined registers and the expanded functionality registers are outlined in Table 3−12.

Table 3−12. MDIO Registers

REGISTER ADDRESS	REGISTER NAME	DEFINITION
0	Control	IEEE 802.3 defined. See Table 3−13
1	Status	IEEE 802.3 defined. See Table 3−14
2, 3	PHY identifier	IEEE 802.3 defined. See Table 3−15 and Table 3−16
4−14	Not applicable	−
15	Extended status	IEEE 802.3 defined. See Table 3−17
16	Global configuration	See Table 3−18
17−20	Channel A−D configuration	See Table 3−19, Table 3−20, Table 3−21, and Table 3−22
21	Reserved	Reserved
22	Channel status	See Table 3−23
23	Channel sync status	See Table 3−24
24	CTC status	See Table 3−25
25	Error counter control	See Table 3−26
26−29	Channel A−D error count	See Table 3−27, Table 3−28, Table 3−29, and Table 3−30
4.0	PHY XS control 1	IEEE 802.3 defined. See Table 3−31
4.1	PHY XS status 1	IEEE 802.3 defined. See Table 3−32
4.2, 4.3	PHY XS identifier	IEEE 802.3 defined. Same as registers 2, 3
4.4	PHY XS speed ability	IEEE 802.3 defined. See Table 3−33
4.5	Devices in package	IEEE 802.3 defined. See Table 3−34
4.6, 4.7	Not applicable	−
4.8	PHY XS status 2	IEEE 802.3 defined. See Table 3−35
4.9−4.23	Not applicable	−
4.24	10G PHY XGXS lane status	See Table 3−36
4.25−4.32767	Not applicable	−
4.32768	PHY XS global configuration	See Table 3−37
4.32769−4.32772	PHY XS channel A−D configuration	See Table 3−37
4.32773	Reserved	Reserved
4.32774	PHY XS channel status	See Table 3−37
4.32775	PHY XS channel sync status	See Table 3−37
4.32776	PHY XS CTC status	See Table 3−37
4.32777	Error counter control	See Table 3−37
4.32778−4.32781	Channel A−D error count	See Table 3−37
4.32782−4.65535	Not applicable	−
5.0	DTE XS control 1	IEEE 802.3 defined. See Table 3−38
5.1	DTE XS status 1	IEEE 802.3 defined. See Table 3−39
5.2, 5.3	DTE XS identifier	IEEE 802.3 defined. Same as registers 2, 3
5.4	DTE XS speed ability	IEEE 802.3 defined. See Table 3−40
5.5	Devices in package	IEEE 802.3 defined. See Table 3−41
5.6, 5.7	Not applicable	−
5.8	DTE XS status 2	IEEE 802.3 defined. See Table 3−42
5.9−5.23	Not applicable	−
5.24	10G DTE XGXS lane status	See Table 3−43
5.25−5.32767	Not applicable	−
5.32768	DTE XS global configuration	See Table 3−44
5.32769−5.32772	DTE XS channel A−D configuration	See Table 3−44

Table 3−12. MDIO Registers (Continued)

REGISTER ADDRESS	REGISTER NAME	DEFINITION
5.32773	Reserved	Reserved
5.32774	DTE XS channel status	See Table 3−44
5.32775	DTE XS channel sync status	See Table 3−44
5.32776	DTE XS CTC status	See Table 3−44
5.32777	Error counter control	See Table 3−44
5.32778−5.32781	Channel A−D error count	See Table 3−44
5.32782−5.65535	Not applicable	–

Several MDIO register bits may be affected by Boolean functions. When a bit value is overridden through a Boolean function, writes to that bit are ignored. The bit returns to its prior value once the override is removed.

Table 3−13. Control Register Bit Definitions (Register 0)

BIT(S)	NAME	DESCRIPTION	READ/WRITE
15	Reset	Logically ORed with the inverse of the RSTN terminal. 1 = Global resets including FIFO clear 0 = Normal operation	Read/Write Self Clearing†
14	Loopback	1 = Enable loopback mode on all channels. 0 = Disable loopback mode on all channels (default).	Read/Write
13	Speed selection (LSB)	Not applicable. Read returns a 1.	Read-only
12	Auto-negotiation enable	Not applicable. Read returns a 0.	Read-only
11	Power down	Logically ORed with the inversion of the ENABLE terminal. 1 = Power-down mode is enabled. 0 = Normal operation (default).	Read/Write
10	Isolate	Not applicable. Read returns a 0.	Read-only
9	Restart auto-negotiation	Not applicable. Read returns a 0.	Read-only
8	Duplex mode	Only full duplex is supported. Writes are ignored. Read returns a 1.	Read-only
7	Collision test	Not applicable. Read returns a 0.	Read-only
6	Speed selection (MSB)	Not applicable. Read returns a 1.	Read-only
5:0	Reserved	Write as 0. Ignore on read.	–

† After reset, this bit is set to 1; it automatically sets itself back to 0 on the next MDC clock cycle.

Table 3−14. Status Register Bit Definitions (Register 1)

BIT(S)	NAME	DESCRIPTION	READ/WRITE
15:9		Read returns all 0s.	Read-only
8	Extended status	Read returns a 1, indicating extended status information is held in register 15.	Read-only
7	Reserved	Read is ignored.	Read-only
6:3	Various configurations	Read returns all 0s.	Read-only
2	Link status	1 = Link is up 0 = Link is down Latches low until read.	Read-only
1	Jabber detect	Read returns a 0.	Read-only
0	Extended capability	Read returns a 1, indicating extended register capability.	Read-only

Registers 2 and 3 contain the identifier for the 10-Gbps ethernet XGXS device.

The identifier code is composed of bits 3−24 of the 25-bit organizationally unique identifier (OUI) assigned to Texas Instruments by the IEEE. The 6-bit manufacturer model number is unique to the TLK3114SA device. The manufacturer revision number denotes the current revision of the TLK3114SA device.

Table 3−15. PHY Identifier Bit Definitions (Register 2)

OUI ADDRESS BITS 3−18															
2.15	**2.14**	**2.13**	**2.12**	**2.11**	**2.10**	**2.9**	**2.8**	**2.7**	**2.6**	**2.5**	**2.4**	**2.3**	**2.2**	**2.1**	**2.0**
0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 3−16. PHY Identifier Bit Definitions (Register 3)

OUI ADDRESS BITS 19−24						MANUFACTURER MODEL NUMBER						MANUFACTURER REVISION NUMBER			
3.15	**3.14**	**3.13**	**3.12**	**3.11**	**3.10**	**3.9**	**3.8**	**3.7**	**3.6**	**3.5**	**3.4**	**3.3**	**3.2**	**3.1**	**3.0**
0	1	0	1	0	0	0	0	0	1	0	1	0	0	0	0

Table 3−17. Extended Status Register Bit Definitions (Register 15)

BIT(S)	NAME	DESCRIPTION	READ/WRITE
15:12	Various configurations	Read returns all 0s.	Read-only
11:0	Reserved	Read returns all 0s.	Read-only

See also registers 17−20 for individual channel configurations.

Writing to register 16 overwrites any previous settings to registers 17−20.

Table 3−18. Global Configuration Register Bit Definitions (Register 16)

BIT(S)	NAME	DESCRIPTION	READ/WRITE
15	Reserved	Read returns 0, writes are ignored.	Read-only
14	De-skew state machine	1 = Enable deskew state machine described in Figure 3−10. 0 = Disable deskew state machine (default).	Read/Write
13	Channel synchronization state machine	1 = Enable channel synchronization state machine described in Figure 3−7. 0 = Disable channel synchronization state machine (default).	Read/Write
12	IPG management state machine	1 = Enable IPG management state machine described in Figure 3−13. 0 = Disable IPG management state machine (default).	Read/Write
11	Clock tolerance compensation	1 = Enable clock tolerance compensation. 0 = Disable clock tolerance compensation (default).	Read/Write
10:9	Multifunction pin output	Multifunction (MF[A−D]) terminal configuration. Bit 10 / Bit 9 / Output 0 / 0 / HSTL = 1, SSTL_2 = 0 (default) 0 / 1 / 1 = Comma detected, 0 = data 1 / 0 / Register 22, bits 3−0 (LOS) 1 / 1 / Register 22, bits 7−4 (PRBS pass)	Read/Write
8	Loss of signal detection	1 = Enable LOS condition described in Table 3−6 for all channels (default). 0 = Disable this function.	Read/Write
7	Configuration: Config1	Configuration bits (see Table 3−10), default value = 0. When CONFIG1 = low, this bit can be set to 1. When CONFIG1 = high, this bit is read-only. Logically ORed with external input CONFIG1.	Read/Write
6	Configuration: Config0	Configuration bits (see Table 3−10), default value = 0 When CONFIG0 = low, this bit can be set to 1. When CONFIG0 = high, this bit is read-only. Logically ORed with external input CONFIG0.	Read/Write
5	Preemphasis: Pre2	Programmable preemphasis control (see Table 3−9), default value = 0.	Read/Write
4	Preemphasis: Pre1	Programmable preemphasis control (see Table 3−9), default value = 0.	Read/Write
3	Reserved	Read returns a 0, writes are ignored.	Read-only
2	PRBS enable	1 = Enable PRBS internal generation and verification on all channels 0 = Normal operation (default). When PRBSEN = low, this bit can be set to 1. When PRBSEN = high, this bit is read-only. Logically ORed with PRBSEN.	Read/Write
1	Comma detect enable	1 = Enable K28.5 code detection and bit alignment on all channels (default). 0 = Disable K28.5 code detection on all channels. Logically AND'ed with SYNCEN.	Read/Write
0	Reserved	Read returns a 0, writes are ignored.	Read/Write

Table 3−19. Channel A Configuration Registers Bit Definitions (Register 17)

BIT(S)	NAME	DESCRIPTION	READ/WRITE
15:12	Reserved	Read returns all 0s, writes are ignored.	Read-only
11	Clock tolerance compensation	1 = Enable clock tolerance compensation. 0 = Disable clock tolerance compensation (default). Logically ORed with register 16, bit 11.	Read/Write
10:9	Multifunction pin output	Multifunction (MFA) pin configuration for channel A. Bit 10 / Bit 9 / MFA Output 0 / 0 / HSTL = 1, SSTL_2 = 0 (default) 0 / 1 / 1 = Comma detected, 0 = data 1 / 0 / Register 22, bit 0 (LOS) 1 / 1 / Register 22, bit 4 (PRBS pass) Logically ORed with register 16, bits 10 and 9.	Read/Write
8	Loss of Signal Detection	1 = Enable LOS condition described in Table 3−7 for channel A (default). 0 = Disable this function. Logically AND'ed with register 16, bit 8.	Read/Write
7	Configuration: Config1	Configuration bits (see Table 3−10), default value = 0 When CONFIG1 = low, this bit can be set to 1. When CONFIG1 = high, this bit is read-only. Logically ORed with register 16, bit 7.	Read/Write
6	Configuration: Config0	Configuration bits (see Table 3−10), default value = 0 When CONFIG0 = low, this bit can be set to 1. When CONFIG0 = high, this bit is read-only. Logically ORed with register 16, bit 6.	Read/Write
5	Preemphasis: Pre2	Programmable preemphasis control (see Table 3−9), default value = 0. Logically ORed with register 16, bit 5.	Read/Write
4	Preemphasis: Pre1	Programmable preemphasis control (see Table 3−9), default value = 0. Logically ORed with register 16, bit 4.	Read/Write
3	Loopback	1 = Enable loopback mode on channel A. 0 = Disable loopback mode on channel A (default). Logically ORed with register 0, bit 14. When LPENA = low, this bit can be set to 1. When LPENA = high, this bit is read-only.	Read/Write
2	PRBS enable	1 = Enable PRBS internal generation and verification on channel A 0 = Normal operation (default). Logically ORed with register 16, bit 2. When PRBSEN = low, this bit can be set to 1. When PRBSEN = high, this bit is read-only.	Read/Write
1	Comma detect enable	1 = Enable K28.5 code detection and bit alignment on channel A (default). 0 = Disable K28.5 code detection on channel A. Logically AND'ed with SYNCEN and register 16, bit 1.	Read/Write
0	Power down	1 = Power-down mode is enabled for channel A. 0 = Normal operation (default). Logically ORed with register 0, bit 11.	Read/Write

Table 3−20. Channel B Configuration Registers Bit Definitions (Register 18)

BIT(S)	NAME	DESCRIPTION	READ/WRITE
15:12	Reserved	Read returns all 0s, writes are ignored.	Read-only
11	Clock tolerance compensation	1 = Enable clock tolerance compensation. 0 = Disable clock tolerance compensation (default). Logically ORed with register 16, bit 11.	Read/Write
10:9	Multifunction pin output	Multifunction (MFB) pin configuration for channel B. Bit 10 / Bit 9 / MFB Output 0 / 0 / HSTL = 1, SSTL_2 = 0 (default) 0 / 1 / 1 = Comma detected, 0 = data 1 / 0 / Register 22, bit 1 (LOS) 1 / 1 / Register 22, bit 5 (PRBS Pass) Logically ORed with register 16, bits 10 and 9.	Read/Write
8	Loss of signal detection	1 = Enable LOS condition described in Table 3−7 for channel B (default). 0 = Disable this function. Logically AND'ed with register 16, bit 8.	Read/Write
7	Configuration: Config1	Configuration bits (see Table 3−10), default value = 0. When CONFIG1 = low, this bit can be set to 1. When CONFIG1 = high, this bit is read-only. Logically ORed with register 16, bit 7.	Read/Write
6	Configuration: Config0	Configuration bits (see Table 3−10), default value = 0 When CONFIG0 = low, this bit can be set to 1. When CONFIG0 = high, this bit is read-only. Logically ORed with register 16, bit 6.	Read/Write
5	Preemphasis: Pre2	Programmable preemphasis control (see Table 3−9), default value = 0. Logically ORed with register 16, bit 5.	Read/Write
4	Preemphasis: Pre1	Programmable preemphasis control (see Table 3−9), default value = 0. Logically ORed with register 16, bit 4.	Read/Write
3	Loopback	1 = Enable loopback mode on channel B. 0 = Disable loopback mode on channel B (default). Logically ORed with register 0, bit 14.	Read/Write
2	PRBS enable	1 = Enable PRBS internal generation and verification on channel B. 0 = Normal operation (default). Logically ORed with register 16, bit 2. When PRBSEN = low, this bit can be set to 1. When PRBSEN = high, this bit is read-only.	Read/Write
1	Comma detect enable	1 = Enable K28.5 code detection and bit alignment on channel B (default). 0 = Disable K28.5 code detection on channel B. Logically AND'ed with SYNCEN and register 16, bit 1.	Read/Write
0	Power down	1 = Power-down mode is enabled for channel B. 0 = Normal operation (default). Logically ORed with register 0, bit 11.	Read/Write

Table 3−21. Channel C Configuration Registers Bit Definitions (Register 19)

BIT(S)	NAME	DESCRIPTION	READ/WRITE
15:12	Reserved	Read returns all 0s, writes are ignored.	Read-only
11	Clock tolerance compensation	1 = Enable clock tolerance compensation. 0 = Disable clock tolerance compensation (default). Logically ORed with register 16, bit 11.	Read/Write
10:9	Multifunction pin output	Multifunction (MFC) pin configuration for channel C. Bit 10 / Bit 9 / MFC Output 0 / 0 / HSTL = 1, SSTL_2 = 0 (default) 0 / 1 / 1 = Comma detected, 0 = data 1 / 0 / Register 22, bit 2 (LOS) 1 / 1 / Register 22, bit 6 (PRBS Pass) Logically ORed with register 16, bits 10 and 9.	Read/Write
8	Loss of signal detection	1 = Enable LOS condition described in Table 3−7 for channel C (default). 0 = Disable this function. Logically AND'ed with register 16, bit 8.	Read/Write
7	Configuration: Config1	Configuration bits (see Table 3−10), default value = 0 When CONFIG1 = low, this bit can be set to 1. When CONFIG1 = high, this bit is read-only. Logically ORed with register 16, bit 7.	Read/Write
6	Configuration: Config0	Configuration bits (see Table 3−10), default value = 0 When CONFIG0 = low, this bit can be set to 1. When CONFIG0 = high, this bit is read-only. Logically ORed with register 16, bit 6.	Read/Write
5	Preemphasis: Pre2	Programmable preemphasis control (see Table 3−9), default value = 0. Logically ORed with register 16, bit 5.	Read/Write
4	Preemphasis: Pre1	Programmable preemphasis control (see Table 3−9), default value = 0. Logically ORed with register 16, bit 4.	Read/Write
3	Loopback	1 = Enable loopback mode on channel C. 0 = Disable loopback mode on channel C (default). Logically ORed with register 0, bit 14.	Read/Write
2	PRBS enable	1 = Enable PRBS internal generation and verification on channel C. 0 = Normal operation (default). Logically ORed with register 16, bit 2 When PRBSEN = low, this bit can be set to 1. When PRBSEN = high, this bit is read-only.	Read/Write
1	Comma detect enable	1 = Enable K28.5 code detection and bit alignment on channel C (default). 0 = Disable K28.5 code detection on channel C. Logically AND'ed with SYNCEN and register 16, bit 1.	Read/Write
0	Power down	1 = Power-down mode is enabled for channel C. 0 = Normal operation (default). Logically ORed with register 0, bit 11.	Read/Write

Table 3−22. Channel D Configuration Registers Bit Definitions (Register 20)

BIT(S)	NAME	DESCRIPTION	READ/WRITE
15:12	Reserved	Read returns all 0s, writes are ignored.	Read-only
11	Clock tolerance compensation	1 = Enable clock tolerance compensation. 0 = Disable clock tolerance compensation (default). Logically ORed with register 16, bit 11	Read/Write
10:9	Multifunction pin output	Multifunction (MFD) pin configuration for channel D. Bit 10 / Bit 9 / MFD Output 0 / 0 / HSTL = 1, SSTL_2 = 0 (default) 0 / 1 / 1 = Comma detected, 0 = data 1 / 0 / Register 22, bit 3 (LOS) 1 / 1 / Register 22, bit 7 (PRBS Pass) Logically ORed with register 16, bits 10 and 9.	Read/Write
8	Loss of signal detection	1 = Enable LOS condition described in Table 3−7 for channel D (default). 0 = Disable this function. Logically AND'ed with register 16, bit 8.	Read/Write
7	Configuration: Config1	Configuration bits (see Table 3−10), default value = 0 When CONFIG1 = low, this bit can be set to 1. When CONFIG1 = high, this bit is read-only. Logically ORed with register 16, bit 7.	Read/Write
6	Configuration: Config0	Configuration bits (see Table 3−10), default value = 0 When CONFIG0 = low, this bit can be set to 1. When CONFIG0 = high, this bit is read-only. Logically ORed with register 16, bit 6.	Read/Write
5	Preemphasis: Pre2	Programmable preemphasis control (see Table 3−9), default value = 0. Logically ORed with register 16, bit 5.	Read/Write
4	Preemphasis: Pre1	Programmable preemphasis control (see Table 3−9), default value = 0. Logically ORed with register 16, bit 4.	Read/Write
3	Loopback	1 = Enable loopback mode on channel D. 0 = Disable loopback mode on channel D (default). Logically ORed with register 0, bit 14	Read/Write
2	PRBS enable	1 = Enable PRBS internal generation and verification on channel D 0 = Normal operation (default) Logically ORed with register 16, bit 2 When PRBSEN = low, this bit can be set to 1. When PRBSEN = high, this bit is read-only.	Read/Write
1	Comma detect enable	1 = Enable K28.5 code detection and bit alignment on channel D (default). 0 = Disable K28.5 code detection on channel D. Logically AND'ed with SYNCEN and register 16, bit 1	Read/Write
0	Power down	1 = Power-down mode is enabled for channel D. 0 = Normal operation (default) Logically ORed with register 0, bit 11	Read/Write

Table 3−23. Channel Status Register (Register 22)

BIT(S)	NAME	DESCRIPTION	READ/WRITE
15	Channel D transmit FIFO collision error	1 = Collision error is detected to cause the transmit FIFO self reset. 0 = No error (default) After being read, this bit is reset to 0.	Read-only
14	Channel C transmit FIFO collision error	1 = Collision error is detected to cause the transmit FIFO self reset. 0 = No error (default) After being read, this bit is reset to 0.	Read-only
13	Channel B transmit FIFO collision error	1 = Collision error is detected to cause the transmit FIFO self reset. 0 = No error (default) After being read, this bit is reset to 0.	Read-only
12	Channel A transmit FIFO collision error	1 = Collision error is detected to cause the transmit FIFO self reset. 0 = No error (default) After being read, this bit is reset to 0.	Read-only
11	Channel D decode error	1 = Code word or running disparity error detected. 0 = No error (default) After being read, this bit is reset to 0.	Read-only
10	Channel C decode error	1 = Code word or running disparity error detected. 0 = No error (default) After being read, this bit is reset to 0.	Read-only
9	Channel B decode error	1 = Code word or running disparity error detected. 0 = No error (default) After being read, this bit is reset to 0.	Read-only
8	Channel A decode error	1 = Code word or running disparity error detected. 0 = No error (default) After being read, this bit is reset to 0.	Read-only
7	Channel D PRBS pass	1 = PRBS testing passes without error (default). 0 = Error is detected during PRBS test. After PRBS_PASS has been cleared, reading this bit sets it to 1.	Read-only
6	Channel C PRBS pass	1 = PRBS testing passes without error (default). 0 = Error is detected during PRBS test. After PRBS_PASS has been cleared, reading this bit sets it to 1.	Read-only
5	Channel B PRBS pass	1 = PRBS testing passes without error (default). 0 = Error is detected during PRBS test. After PRBS_PASS has been cleared, reading this bit sets it to 1.	Read-only
4	Channel A PRBS pass	1 = PRBS testing passes without error (default). 0 = Error is detected during PRBS test After PRBS_PASS has been cleared, reading this bit sets it to 1.	Read-only
3	Channel D LOS output	1 = LOS condition is reported. 0 = No LOS (default) After being read, this bit is reset to 0.	Read-only
2	Channel C LOS output	1 = LOS condition is reported. 0 = No LOS (default) After being read, this bit is reset to 0.	Read-only
1	Channel B LOS output	1 = LOS condition is reported. 0 = No LOS (default) After being read, this bit is reset to 0.	Read-only
0	Channel A LOS output	1 = LOS condition is reported. 0 = No LOS (default) After being read, this bit is reset to 0.	Read-only

Table 3−24. Channel Synchronization Status Register (Register 23)

BIT(S)	NAME	DESCRIPTION	READ/WRITE
15:5	Reserved	Read returns all 0s.	Read-only
4	Channel allign flag	1 = Channel deskew circuit has realigned to a K28.3 /A/ code word on all channels. 0 = No /A/ has been detected. After being read, this bit is reset to 0.	Read-only
3	Channel D receive FIFO collision error	1 = Collision error is detected to cause the receive FIFO self reset. 0 = No error. After being read, this bit is reset to 0.	Read-only
2	Channel C receive FIFO collision error	1 = Collision error is detected to cause the receive FIFO self reset. 0 = No error. After being read, this bit is reset to 0.	Read-only
1	Channel B receive FIFO collision error	1 = Collision error is detected to cause the receive FIFO self reset. 0 = No error. After being read, this bit is reset to 0.	Read-only
0	Channel A receive FIFO collision error	1 = Collision error is detected to cause the receive FIFO self reset. 0 = No error. After being read, this bit is reset to 0.	Read-only

Table 3−25. Clock Tolerance Compensation Status (Register 24)

BIT(S)	NAME	DESCRIPTION	READ/WRITE
15	Channel D drop idle column	1 = IDLE column has been dropped. 0 = No IDLE column dropped. After being read, this bit is reset to 0.	Read-only
14	Channel C drop idle column	1 = IDLE column has been dropped. 0 = No IDLE column dropped. After being read, this bit is reset to 0.	Read-only
13	Channel B drop idle column	1 = IDLE column has been dropped. 0 = No IDLE column dropped. After being read, this bit is reset to 0.	Read-only
12	Channel A drop idle column	1 = IDLE column has been dropped. 0 = No IDLE column dropped. After being read, this bit is reset to 0.	Read-only
11	Channel D insert idle column	1 = IDLE column has been inserted. 0 = No IDLE column inserted. After being read, this bit is reset to 0.	Read-only
10	Channel C insert idle column	1 = IDLE column has been inserted. 0 = No IDLE column inserted. After being read, this bit is reset to 0.	Read-only
9	Channel B insert idle column	1 = IDLE column has been inserted. 0 = No IDLE column inserted. After being read, this bit is reset to 0.	Read-only
8	Channel A insert idle column	1 = IDLE column has been inserted. 0 = No IDLE column inserted. After being read, this bit is reset to 0.	Read-only
7	Channel D FIFO overflow	1 = FIFO overflow condition 0 = No error After being read, this bit is reset to 0.	Read-only
6	Channel C FIFO overflow	1 = FIFO overflow condition 0 = No error After being read, this bit is reset to 0.	Read-only
5	Channel B FIFO overflow	1 = FIFO overflow condition 0 = No error After being read, this bit is reset to 0.	Read-only
4	Channel A FIFO overflow	1 = FIFO overflow condition 0 = No error After being read, this bit is reset to 0.	Read-only
3	Channel D FIFO underflow	1 = FIFO underflow condition 0 = No error After being read, this bit is reset to 0.	Read-only
2	Channel C FIFO underflow	1 = FIFO underflow condition 0 = No error After being read, this bit is reset to 0.	Read-only
1	Channel B FIFO underflow	1 = FIFO underflow condition 0 = No error After being read, this bit is reset to 0.	Read-only
0	Channel A FIFO underflow	1 = FIFO underflow condition 0 = No error After being read, this bit is reset to 0.	Read-only

Table 3−26. Error Counter Control Register (Register 25)

BIT(S)	NAME	DESCRIPTION	READ/WRITE
15:4	Reserved	Read returns all 0s.	Read-only
3	Channel D counter select	0 = Running disparity error counter (default). 1 = Decode error counter	Read/Write
2	Channel C counter select	0 = Running disparity error counter (default). 1 = Decode error counter	Read/Write
1	Channel B counter select	0 = Running disparity error counter (default). 1 = Decode error counter	Read/Write
0	Channel A counter select	0 = Running disparity error counter (default). 1 = Decode error counter	Read/Write

Table 3−27. Channel A Error Count (Register 26)

BIT(S)	NAME	DESCRIPTION	READ/WRITE
15:0	Error count	Channel A running disparity or decode error count value selected by register 25, bit 0. After being read, this counter is reset to 0.	Read-only

Table 3−28. Channel B Error Count (Register 27)

BIT(S)	NAME	DESCRIPTION	READ/WRITE
15:0	Error count	Channel B running disparity or decode error count value selected by register 25, bit 1. After being read, this counter is reset to 0.	Read-only

Table 3−29. Channel C Error Count (Register 28)

BIT(S)	NAME	DESCRIPTION	READ/WRITE
15:0	Error count	Channel C running disparity or decode error count value selected by register 25, bit 2. After being read, this counter is reset to 0.	Read-only

Table 3−30. Channel D Error Count (Register 29)

BIT(S)	NAME	DESCRIPTION	READ/WRITE
15:0	Error count	Channel D running disparity or decode error count value selected by register 25, bit 3. After being read, this counter is reset to 0.	Read-only

Table 3−31. PHY XS Control 1 Register (Register 4.0)

BIT(S)	NAME	DESCRIPTION	READ/WRITE
15	Reset	Logically ORed with the inverse of RSTN terminal. 1 = Global resets including FIFO clear. 0 = Normal operation (default)	Read/Write Self Clearing†
14	Loopback	1 = Enable loopback mode on all channels. 0 = Disable loopback mode on all channels (default).	Read/Write
13	Speed selection (LSB)	Not applicable. Read returns 1.	Read-only
12:7	Reserved	Not applicable. Read returns all 0s.	Read-only
6	Speed selection (MSB)	Not applicable. Read returns 1.	Read-only
5:2	Speed selection	Not applicable. Read returns all 0s.	Read-only
1:0	Reserved	Not applicable. Read returns all 0s.	Read-only

† After reset, this bit is set to 1; it automatically sets itself back to 0 on the next MDC clock cycle.

Table 3−32. PHY XS Status 1 Register (Register 4.1)

BIT(S)	NAME	DESCRIPTION	READ/WRITE
15:8	Reserved	Read is ignored.	Read-only
7	Local fault	Logical OR of register 4.8, bits 10 and 11.	Read-only
6:3	Reserved	Read is ignored.	Read-only
2	TX link status	1 = Link is up 0 = Link is down Latches low until read.	Read-only
1:0	Reserved	Read is ignored.	Read-only

Table 3−33. PHY XS Speed Ability Register (Register 4.4)

BIT(S)	NAME	DESCRIPTION	READ/WRITE
15:1	Reserved	Read returns all 0s.	Read-only
0	10G capable	Read returns 1.	Read-only

Table 3−34. Devices in Package Register (Register 4.5)

BIT(S)	NAME	DESCRIPTION	READ/WRITE
15:6	Reserved	Read is ignored.	Read-only
5	DTE XS present	1 = Device is configured as a DTE XS. 0 = Device is configured as a PHY XS.	Read-only
4	PHY XS present	1 = Device is configured as a PHY XS. 0 = Device is configured as a DTE XS.	Read-only
3:1	Not applicable	Read returns all 0s.	Read-only
0	Clause 22 registers present	Read returns 1.	Read-only

Table 3−35. 10G PHY XS Status 2 Register (Register 4.8)

BIT(S)	NAME	DESCRIPTION	READ/WRITE
15	Device present	Read returns 1.	Read-only
14	Device present	Read returns 0.	Read-only
13:12	Reserved	Read is ignored.	Read-only
11	Transmit local fault	1 = Transmit fault detected 0 = No transmit fault detected Latches high until read.	Read-only
10	Receive local fault	1 = Receive fault detected 0 = No receive fault detected Latches high until read.	Read-only
9:0	Reserved	Read is ignored.	Read-only

Table 3−36. 10G PHY XGXS Lane Status Register (Register 4.24)

BIT(S)	NAME	DESCRIPTION	READ/WRITE
15:13	Reserved	Read is ignored.	Read-only
12	Lane alignment	1 = PHY XGXS transmit lanes aligned 0 = PHY XGXS transmit lanes not aligned	Read-only
11:4	Reserved	Read is ignored.	Read-only
3	Lane D sync	Lane D is synchronized.	Read-only
2	Lane C sync	Lane C is synchronized.	Read-only
1	Lane B sync	Lane B is synchronized.	Read-only
0	Lane A sync	Lane A is synchronized.	Read-only

MDIO registers 4.32768−4.32781 are analogous to registers 16−29. The following table cross references the appropriate register definition.

Table 3−37. PHY XS Register Cross Reference (Registers 4.32768−4.32776)

REGISTER ADDRESS	NAME	EQUIVALENT REGISTER ADDRESS	EQUIVALENT REGISTER NAME	DEFINITION
4.32768	PHY XS global configuration	16	Global Configuration	See Table 3−18
4.32769−4.32772	PHY XS channels A−D configuration	17−20	Channels A−D Configuration	See Table 3−19, Table 3−20, Table 3−21, and Table 3−22
4.32774	PHY XS channel status	22	Channel Status	See Table 3−23
4.32775	PHY XS channel sync status	23	Channel Sync Status	See Table 3−24
4.32776	PHY XS CTC status	24	CTC Status	See Table 3−25
4.32777	Error counter control	25	Error Counter Control	See Table 3−26
4.32778−4.32781	Channels A−D error count	26−29	Channels A−D Error Count	See Table 3−27, Table 3−28, Table 3−29, and Table 3−30

Table 3−38. DTE XS Control 1 Register (Register 5.0)

BIT(S)	NAME	DESCRIPTION	READ/WRITE
15	Reset	Logically ORed with the inverse of RSTN terminal. 1 = Global resets including FIFO clear. 0 = Normal operation (default).	Read/Write Self Clearing†
14	Loopback	1 = Enable loopback mode on all channels. 0 = Disable loopback mode on all channels (default).	Read/Write
13	Speed selection (LSB)	Not applicable. Read returns 1.	Read-only
12:7	Reserved	Not applicable. Read returns all 0s.	Read-only
6	Speed selection (MSB)	Not applicable. Read returns 1.	Read-only
5:2	Speed selection	Not applicable. Read returns all 0s.	Read-only
1:0	Reserved	Not applicable. Read returns all 0s.	Read-only

† After reset, this bit is set to 1; it automatically sets itself back to 0 on the next MDC clock cycle.

Table 3−39. DTE XS Status 1 Register (Register 5.1)

BIT(S)	NAME	DESCRIPTION	READ/WRITE
15:8	Reserved	Read is ignored.	Read-only
7	Local fault	Logical OR of register 5.8, bits 10 and 11.	Read-only
6:3	Reserved	Read is ignored.	Read-only
2	RX link status	1 = Link is up 0 = Link is down Latches low until read.	Read-only
1:0	Reserved	Read is ignored.	Read-only

Table 3−40. DTE XS Speed Ability Register (Register 5.4)

BIT(S)	NAME	DESCRIPTION	READ/WRITE
15:1	Reserved	Read returns all 0s.	Read-only
0	10G capable	Read returns a 1.	Read-only

Table 3−41. Devices in Package Register (Register 5.5)

BIT(S)	NAME	DESCRIPTION	READ/WRITE
15:6	Reserved	Read is ignored.	Read-only
5	DTE XS present	1 = Device is configured as a DTE XS. 0 = Device is configured as a PHY XS.	Read-only
4	PHY XS present	1 = Device is configured as a PHY XS. 0 = Device is configured as a DTE XS.	Read-only
3:1	Not applicable	Read returns all 0s.	Read-only
0	Clause 22 registers present	Read returns 1.	Read-only

Table 3−42. 10G DTE XS Status 2 Register (Register 5.8)

BIT(S)	NAME	DESCRIPTION	READ/WRITE
15	Device present	Read returns 1.	Read-only
14	Device present	Read returns 0.	Read-only
13:12	Reserved	Read is ignored.	Read-only
11	Transmit local fault	1 = Transmit fault detected 0 = No transmit fault detected Latches high until read.	Read-only
10	Receive local fault	1 = Receive fault detected 0 = No receive fault detected Latches high until read.	Read-only
9:0	Reserved	Read is ignored.	Read-only

Table 3−43. 10G DTE XGXS Lane Status Register (Register 5.24)

BIT(S)	NAME	DESCRIPTION	READ/WRITE
15:13	Reserved	Read is ignored.	Read-only
12	Lane alignment	1 = DTE XGXS transmit lanes aligned 0 = DTE XGXS transmit lanes not aligned	Read-only
11:4	Reserved	Read is ignored.	Read-only
3	Lane D sync	Lane D is synchronized	Read-only
2	Lane C sync	Lane C is synchronized	Read-only
1	Lane B sync	Lane B is synchronized	Read-only
0	Lane A sync	Lane A is synchronized	Read-only

MDIO registers 5.32768−5.32781 are analogous to registers 16−29. The following table cross references the appropriate register definition.

Table 3−44. DTE XS Register Cross Reference (Registers 5.32768−5.32776)

REGISTER ADDRESS	NAME	EQUIVALENT REGISTER ADDRESS	EQUIVALENT REGISTER NAME	DEFINITION
5.32768	DTE XS global configuration	16	Global configuration	See Table 3−18
5.32769−5.32772	DTE XS channel A−D configuration	17−20	Channel A−D configuration	See Table 3−19, Table 3−20, Table 3−21, and Table 3−22
5.32774	DTE XS channel status	22	Channel status	See Table 3−23
5.32775	DTE XS channel sync status	23	Channel sync status	See Table 3−24
5.32776	DTE XS CTC status	24	CTC status	See Table 3−25
5.32777	Error counter control	25	Error counter control	See Table 3−26
5.32778−5.32781	Channel A−D error count	26−29	Channel A−D error count	See Table 3−27, Table 3−28, Table 3−29, and Table 3−30

3.26 Operating Frequency Range

The TLK3114SA device is optimized for operation at a serial data rate of 3.125 Gbps. The TLK3114SA device may operate at a serial data rate between 2.5 Gbps to 3.125 Gbps. The external differential reference clock has an operating frequency from 125 MHz to 156.25 MHz. The reference clock frequency must be within ±100 PPM and have less than 40 ps of jitter.

3.27 Power-Down Mode

When the ENABLE terminal is held low, the TLK3114SA device enters a low power quiescent state. In this state, all analog and digital circuitry is disabled. In the power-down mode, the serial transmit and the receive data bus terminals for all channels are in a high-impedance state.

3.28 Loop Back Testing

The TLK3114SA device can provide a self-test function by enabling the internal loop-back path with the assertion of LPENx for each channel, setting bit 14 (Loopback) of register 4.0 or 5.0, or by setting bit 3 (Loopback) of MDIO channel configuration registers 17−20, 4.32769−4.32772, or 5.32769−5.32772. Enabling this terminal or bit causes serial transmitted data to be routed internally to the receiver for that channel (see Figure 1−5). The parallel data output can be compared to the parallel input data for that channel to provide functional verification. The external differential output is held in a high-impedance state during the loop-back testing.

3.29 Power-On Reset

Upon application of minimum valid power, the TLK3114SA device generates an internal power-on reset. During the power-on reset the receive data terminals RDx[0:9] are tri-stated and the recovered receive clock terminals RC[A−D] are held low. The length of the power-on reset cycle is dependent upon the frequency of the reference clock, RFCP/RFCN, but is less than 1 ms in duration.

3.30 Differences From the TLK3104SA Device

The TLK3114SA device contains several functional improvements and extensions beyond those included in the TLK3104SA device. These differences are outlined in Table 3−45.

Table 3−45. Comparison of TLK3104SA and TLK3114SA Devices

PARAMETER/FUNCTION	TLK3104SA	TLK3114SA
HSTL	Supports HSTL scaled to 1.8 V	Buffers optimized for 1.5-V HSTL, although they still support 1.8-V scaled HSTL. See Section 3.10.
Comma detect	Comma detect on positive comma only	Comma detect on both positive and negative commas. See Section 3.12.
Improved error reporting	LOS and decode errors reported as 0xFF	Enhanced reporting. See Table 3−6.
End-of-packet error detection and reporting	Not supported	Supported. See Section 3.14.
Local fault and remote fault detection and reporting	Not supported	Supported. See Section 3.15.
IPG code generation and stripping	Not supported	Supported. See Section 3.18.
Clock tolerance compensation	Not supported	Supported. See Section 3.19.
Repeater mode	Not supported	Supported. See Section 3.23.
Power	Low power	Further reduced power
Serial receive	XAUI compliant	Improved signal tolerance
Terminal A1	TRSTN	ENABLE
Terminal U1	ENABLE	DADR0
Clause 45 MDIO	Not supported	Supported. See Section 3.25.
MDIO PHY/PRT address name	DVAD[0:4]	PADR[0:4]
MDIO DEV address specifier	Not supported	DADR0. See Section 3.25.

The ENABLE terminal on the TLK3104SA device is U1. On the TLK3114SA device the ENABLE terminal is terminal A1. The TLK3114SA device is compatible with a design intended for the TLK3104SA device. The TLK3104SA design would be required to pull U1 high and A1 high. If a TLK3114SA device was substituted then U1 would be ignored, since only clause 22 MDIO transactions would be executed, and A1 would still be required to be high. Also, the JTAG standard, IEEE 1149.1, specifies that TRSTN is optional as long as there is an ENABLE or reset terminal which accomplishes the same task. The TLK3114SA device places ENABLE where the TLK3104SA device had TRSTN so that JTAG function is unaffected.

The MDIO register addresses have been renamed to better reflect terminology in IEEE 802.3ae clause 45. The name changes do not reflect a functional change.

4 Electrical Specifications

4.1 Absolute Maximum Ratings Over Operating Free-Air Temperature Range (unless otherwise noted)†

Supply voltage, V_{DD}, V_{DDQ} , V_{DDA} . . . . . −0.3 to 3 V
Input voltage, VI, (LVTTL) . . . . . −0.5 to 4 V
Input voltage, VI, (HSTL/SSTL_2 Class 1) . . . . . −0.5 to 4 V
DC input voltage (I/O) . . . . . −0.3 to 3 V
Storage temperature. T_{stg} . . . . . −65°C to 150°C
Electrostatic discharge . . . . . HBM: 2 kV, CDM: 750 V
Characterized free-air operating temperature range . . . . . 0°C to 70°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE: All voltage values, except differential I/O bus voltages, are stated with respect to the network ground terminal.

4.2 Recommended Operating Conditions

			MIN	TYP	MAX	UNIT
Core supply voltage, V_{DD}			2.3	2.5	2.7	V
I/O supply voltage, V_{DDQ}	SSTL_2 Class 1		2.3	2.5	2.7	V
	HSTL Class 1		1.4	1.5	1.9	
Analog supply voltage, V_{DDA}			2.3	2.5	2.7	V
Core supply current, I_{DD}	R_ω = 156.25 MHz			500	650	mA
I/O supply current, I_{DDQ}	SSTL_2 Class 1,	R_ω = 156.25 MHz		150	325	mA
	HSTL Class 1,	R_ω = 156.25 MHz		120	200	
Analog supply current, I_{DDA}	R_ω = 156.25 MHz			280	320	mA
Total power consumption, P_D	Transceiver mode,	R_ω = 156.25 MHz		2.25	3.25	W
	Transmit mode,	R_ω = 156.25 MHz		0.9	1.5	
	Receive mode,	R_ω = 156.25 MHz		2	2.8	
	Repeater mode,	R_ω = 156.25 MHz		1.8	2.2	
Input reference voltage, V_{REF}	SSTL_2 Class 1		1.15	1.25	1.35	V
	HSTL Class 1		0.68	0.75	0.9	
Analog shutdown current, I_{SDA}	ENABLE = Low			300		µA
Core shutdown current, I_{SDD}	ENABLE = Low			500		µA

† The value of V_{REF} may be selected to provide optimum noise margin in the system. Typically, the value of V_{REF} is expected to be $0.5V_{DDQ}$ of the transmitting device and V_{REF} is expected to track variations in V_{DDQ}. Peak-to-peak ac noise on V_{REF} may not exceed ±2% of V_{REF} (dc).

4.3 Reference Clock Timing Requirements (RFCP/N)

These characteristics are over recommended operating conditions unless otherwise noted.

PARAMETER		CONDITION	MIN	NOM	MAX	UNIT
R_ω	Frequency	Minimum data rate	TYP−0.01%	125	TYP+0.01%	MHz
		Maximum data rate	TYP−0.01%	156.25	TYP+0.01%	
	Accuracy		−100		100	ppm
	Duty cycle		40%	50%	60%	
	Jitter	Random and deterministic			40	ps

This clock must be crystal referenced to meet the requirements of the above table. Contact TI for specific clocking recommendations.

4.4 Reference Clock Electrical Characteristics (RFCP/N)

These characteristics are over recommended operating conditions unless otherwise noted.

PARAMETER		MIN	TYP	MAX	UNIT
V_I	Input voltage	825		1675	mV
V_{idth}	Differential input voltage	200			mV_{P-P}
C_{IN}	Input capacitance			3	pF
R_{IN}	Input differential impedance	80	100	120	Ω

4.5 LVTTL Electrical Characteristics

These characteristics are over recommended operating conditions unless otherwise noted.

See Chapter 2, *Terminal Descriptions*, for a list of LVTTL signals.

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	I_{OH} = −400 µA, V_{DD} = MIN	V_{DD}−0.2		V_{DD}	V
V_{OL}	Low-level output voltage	I_{OL} = 1 mA, V_{DD} = MIN	0	0.25	0.6	V
V_{IH}	High-level input voltage		2		3.5	V
V_{IL}	Low-level input voltage				0.8	V
I_H	High input current	V_{DD} = MAX, V_{IN} = 2 V			40	µA
I_L	Low input current	V_{DD} = MAX, V_{IN} = 0.4 V			−600	µA
C_{IN}	Input capacitance				4	pF

4.6 SSTL_2 Class 1 Signals

See Chapter 2, *Terminal Descriptions*, for a list of SSTL_2 Class 1 signals.

NOTE: For more information on SSTL_2 Class 1 specifications and test conditions, see the EIA/JEDEC, Stub Series Terminated Logic For 2.5 V (SSTL_2), EIA/JESD8-9A, Dec 2000.

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
$V_{OH(dc)}$	High-level output voltage		1.76			V
$V_{OL(dc)}$	Low-level output voltage				0.74	V
$V_{IH(dc)}$	High-level dc input voltage	DC input, logic high	V_{ref}+0.18		V_{DDQ}+0.3	V
$V_{IL(dc)}$	Low-level dc input voltage	DC input, logic low	−0.3		V_{ref}–0.18	V
$V_{IH(ac)}$	High-level ac input voltage	AC input, logic high	V_{ref}+0.35			V
$V_{IL(ac)}$	Low-level ac input voltage	AC input, logic low			V_{ref}–0.35	V
$I_{OH(dc)}$	High-output current	V_{DDQ} = 2.3 V, V_{OUT} = V_{DDQ}–0.62 V	−7.6			mA
$I_{OL(dc)}$	Low-output current	V_{DDQ} = 2.3 V, V_{OUT} = 0.54 V	7.6			mA
C_{IN}	Input capacitance				4	pF

4.7 HSTL Signals

See Chapter 2, *Terminal Descriptions*, for a list of HSTL signals.

NOTE: For more information on HSTL specifications and test conditions, see the EIA/JEDEC, High-Speed Transceiver Logic (HSTL): A 1.5-V Output Buffer Supply Voltage Based Interface Standard for Digital Integrated Circuits, EIA/JESD8-6, Aug 1995.

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
$V_{OH(dc)}$	High-level output voltage		V_{DDQ}−0.4		V_{DDQ}	V
$V_{OL(dc)}$	Low-level output voltage				0.4	V
$V_{IH(dc)}$	High-level dc input voltage	DC input, logic high	V_{ref}+0.1		V_{DDQ}+0.3	V
$V_{IL(dc)}$	Low-level dc input voltage	DC input, logic low	−0.3		V_{ref}–0.1	V
$V_{IH(ac)}$	High-level ac input voltage	AC input, logic high	V_{ref}+0.2			V
$V_{IL(ac)}$	Low-level ac input voltage	AC input, logic low			V_{ref}–0.2	V
$I_{OH(dc)}$	High-output current	V_{DDQ} = 1.5 V	−8			mA
$I_{OL(dc)}$	Low-output current	V_{DDQ} = 1.5 V	8			mA
C_{IN}	Input capacitance				4	pF

4.8 Serial Transmitter/Receiver Characteristics

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
$V_{OD(p)}$	TX output voltage magnitude away from common mode	Maximum preemphasis enabled, See Figure 4−1	650	850	1000	mV
$V_{OD(d)}$		Preemphasis disabled, See Figure 4−1	600		800	mV
$V_{OD(pp)}$	TX output differential peak-to-peak voltage swing	Maximum preemphasis enabled, See Figure 4−1	1300	1700	2000	mV_{P-P}
$V_{OD(pd)}$		Preemphasis disabled, See Figure 4−1	1200	1450	1600	mV_{P-P}
V_{CMT}	TX output common-mode voltage range	See Figure 4−1	1000	1250	1400	mV
V_{ID}	RX input voltage magnitude away from common mode	See Figure 4−3	100		1150	mV
$V_{ID(p)}$	RX input differential peak-to-peak voltage swing	See Figure 4−3	200		2300	mV_{P-P}
V_{CMR}	RX input common-mode voltage range	See Figure 4−3	1000		2000	mV
I_{LKG}	RX input leakage current		−10		10	µA
C_I	RX input capacitance				2	pF
t_r, t_f	Differential output signal rise, fall time (20% to 80%)	R_L = 50 Ω, C_L = 5 pF, See Figure 4−1	80	90	130	ps
J_{TOL}	Jitter tolerance, total jitter at serial input	Zero crossing, See Figure 4−4			0.65	UI†
J_{DR}	Serial input deterministic jitter	Zero crossing, See Figure 4−4			0.37	UI
J_S	Serial input sinusoidal jitter <20 MHz				0.1	UI
J_T	Serial output total jitter	PRBS at 3.125 GHz, See Figure 4−2		0.2	0.35	UI
J_D	Serial output deterministic jitter	PRBS at 3.125 GHz			0.17	UI
$R_{(LATENCY)}$	Total delay from RX input to RD output	See Figure 3−6	89		225	Bits
$T_{(LATENCY)}$	Total delay from TD input to TX output	See Figure 3−2	71		120	Bits

† Unit interval (UI) is one serial bit time (320 ps minimum).

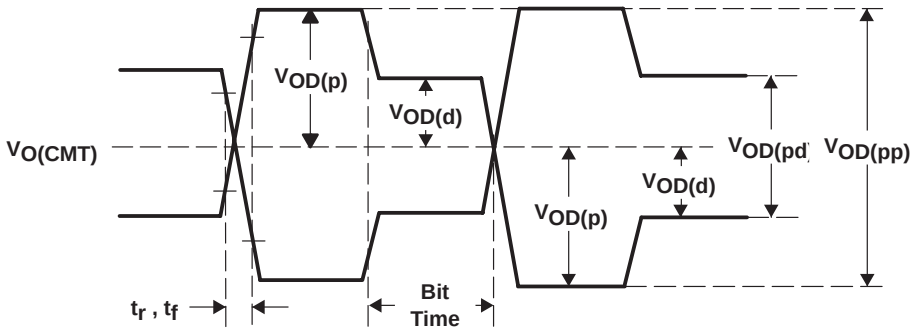


Figure 4−1. Differential and Common-Mode Output Voltage Definitions

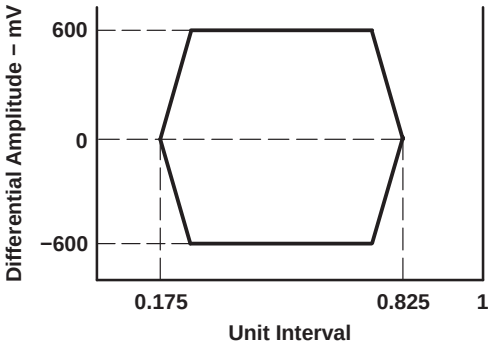


Figure 4−2. Transmit Template

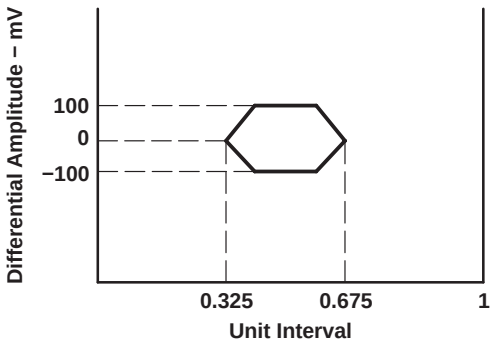
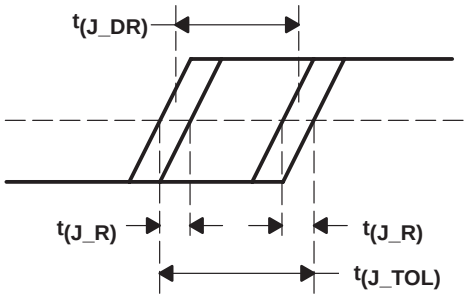


Figure 4−3. Receive Template



NOTE: $t_{(J\_TOL)} = t_{(J\_R)} + t_{(J\_DR)}$, where $t_{(J\_TOL)}$ is the receive jitter tolerance, $t_{(J\_DR)}$ is the received deterministic jitter, and $t_{(J\_R)}$ is the Gaussian random edge jitter distribution at a maximum BER = 10^{-12}.

Figure 4−4. Input Jitter

4.9 SSTL_2 Class 1/HSTL Output Switching Characteristics

These characteristics are over recommended operating conditions unless otherwise noted.

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
t_{su}	RDx[0:9] setup prior to RCx transition high or low	Figure 4−5, timing relative to 0.5xV_{DDQ}	960			ps
t_h	RDx[0:9] hold after RCx transition high or low	Figure 4−5, timing relative to 0.5xV_{DDQ}	960			ps
slew	RDx[0:9] slew rate	C_L = 10 pF	1			mV/ps

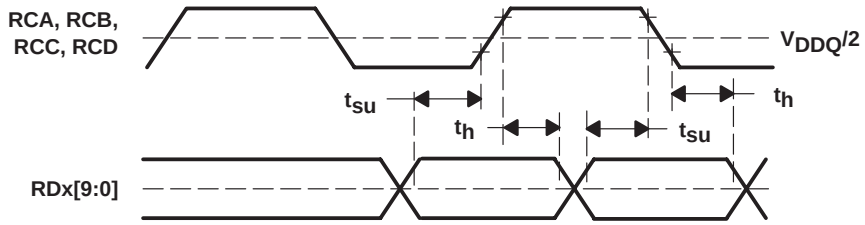


Figure 4−5. SSTL_2 Class 1/HSTL Output Timing Requirements

4.10 SSTL_2 Class 1/HSTL Input Timing Requirements

These characteristics are over recommended operating conditions unless otherwise noted.

PARAMETER		TEST CONDITION	MIN	TYP†	MAX	UNIT
t_{su}	TDx[0:9] setup prior to TCx transition high or low	Figure 4−6, timing relative to V_{REF}	480			ps
t_h	TDx[0:9] hold after TCx transition high or low	Figure 4−6, timing relative to V_{REF}	480			ps

† All typical values are at 25°C with a nominal supply.

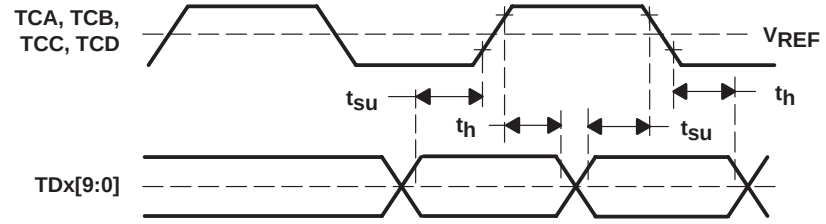


Figure 4−6. SSTL_2 Class 1/HSTL Data Input Timing Requirements

4.11 MDIO Timing Requirements

These characteristics are over recommended operating conditions unless otherwise noted.

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
t_{period}	MDC period	See Figure 4−7	50	400		ns
t_{su}	MDIO setup to ↑ MDC	See Figure 4−7	10			ns
t_h	MDIO hold to ↑ MDC	See Figure 4−7	10			ns

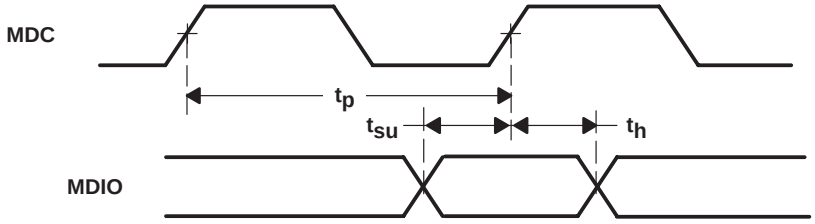


Figure 4−7. MDIO Read/Write Timing

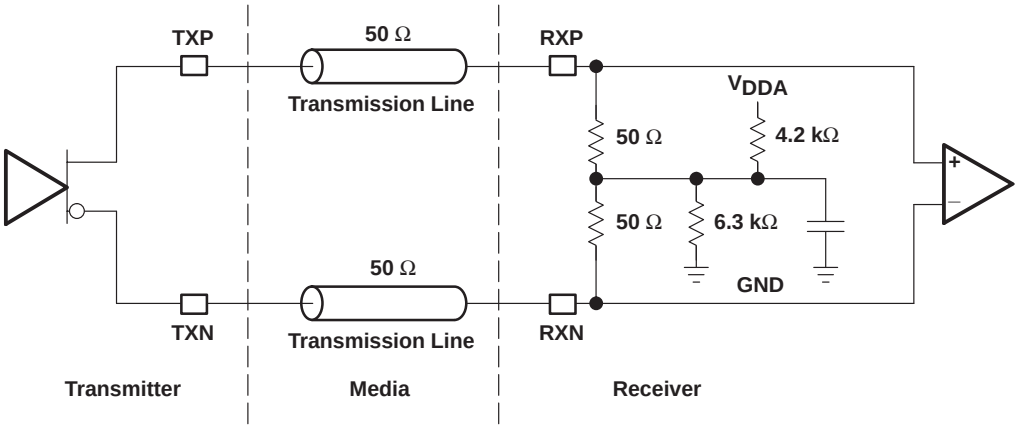


Figure 4−8. High-Speed I/O Direct-Coupled Mode

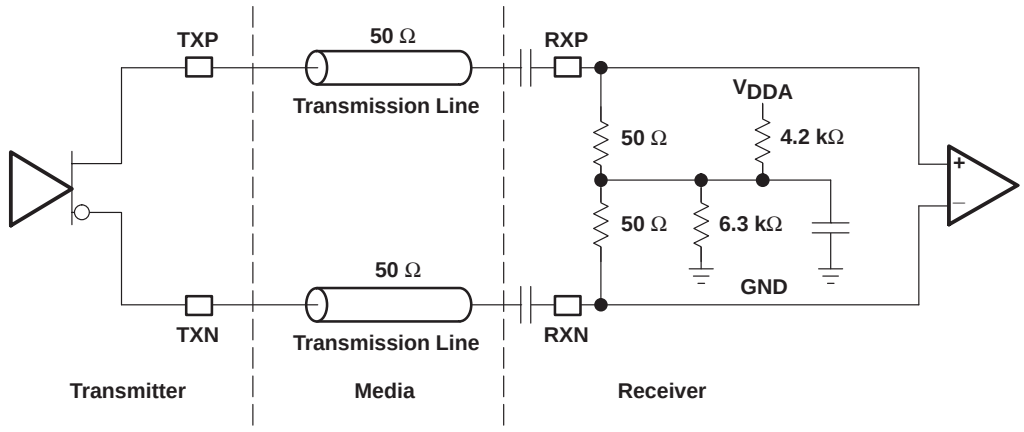
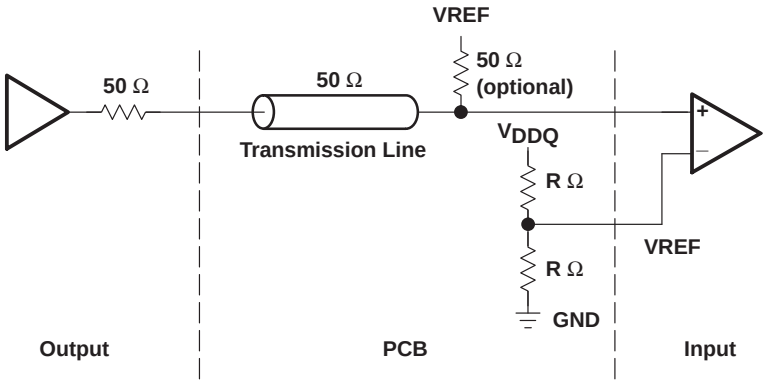
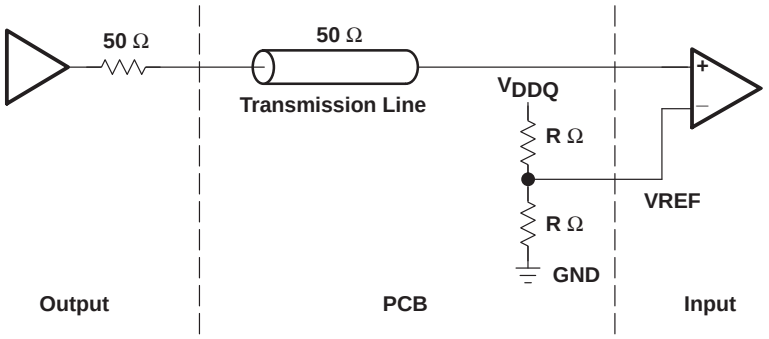


Figure 4−9. Example High-Speed I/O AC-Coupled Mode



NOTE: The output buffer of the TLK3114SA has on-chip termination of 50 Ω. The output signal is compliant with the JEDEC SSTL_2 Class 1 specification. Line termination on the receive end is optional and not recommended for low-power applications.

Figure 4−10. SSTL_2 Class 1 I/O



NOTE: The TLK3114SA provides a push-pull effect on the output buffer for externally sourced series terminated loads. In HSTL mode, the signal swing is small, allowing for minimal power consumption and low electromagnetic emission (EME). To assure sufficient signal levels on the receive side, no termination resistor is used.

Figure 4−11. HSTL I/O

4.12 Package Dissipation Rating

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
θ_{JA}	Junction-to-free air thermal resistance	Airflow = 0 M/S		21.6		°C/W
		Airflow = 1 M/S		17.8		°C/W
		Airflow = 2 M/S		16.7		°C/W

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TLK3114SAGNT	OBSOLETE	BGA	GNT	289		TBD	Call TI	Call TI	0 to 70	TLK3114SAQ 2G	

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
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Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
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(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

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