

NC7SP74 TinyLogic® ULP D-Type Flip-Flop with Preset and Clear

General Description

The NC7SP74 is a single D-type CMOS Flip-Flop with preset and clear from Fairchild's Ultra Low Power (ULP) Series of TinyLogic®. Ideal for applications where battery life is critical, this product is designed for ultra low power consumption within the V_{CC} operating range of 0.9V to 3.6V.

The internal circuit is composed of a minimum of inverter stages including the output buffer, to enable ultra low static and dynamic power.

The NC7SP74, for lower drive requirements, is uniquely designed for optimized power and speed, and is fabricated with an advanced CMOS technology to achieve best in class speed operation while maintaining extremely low CMOS power dissipation.

The signal level applied to the D input is transferred to the Q output during the positive going transition of the CLK pulse.

Features

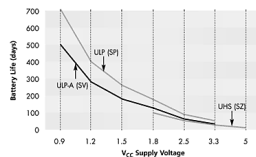
- Space saving US8 surface mount package
- MicroPak™ Pb-Free leadless package
- 0.9V to 3.6V V_{CC} supply operation
- 3.6V overvoltage tolerant I/Os at V_{CC} from 0.9V to 3.6V
- t_{PD}
 - 3.0 ns typ for 3.0V to 3.6V V_{CC}
 - 4.0 ns typ for 2.3V to 2.7V V_{CC}
 - 5.0 ns typ for 1.65V to 1.95V V_{CC}
 - 6.0 ns typ for 1.40V to 1.60V V_{CC}
 - 9.0 ns typ for 1.10V to 1.30V V_{CC}
 - 24.0 ns typ for 0.90V V_{CC}
- Power-Off high impedance inputs and outputs
- Static Drive (I_{OH}/I_{OL})
 - ±2.6 mA @ 3.00V V_{CC}
 - ±2.1 mA @ 2.30V V_{CC}
 - ±1.5 mA @ 1.65V V_{CC}
 - ±1.0 mA @ 1.40V V_{CC}
 - ±0.5 mA @ 1.10V V_{CC}
 - ±20 μ A @ 0.9V V_{CC}
- Uses patented Quiet Series™ noise/EMI reduction circuitry
- Ultra low dynamic power

Ordering Code:

Order Number	Package Number	Product Code Top Mark	Package Description	Supplied As
NC7SP74K8X	MAB08A	P74	8-Lead US8, JEDEC MO-187, Variation CA 3.1mm Wide	3k Units on Tape and Reel
NC7SP74L8X	MAC08A	X9	Pb-Free 8-Lead MicroPak, 1.6 mm Wide	5k Units on Tape and Reel

Pb-Free package per JEDEC J-STD-020B.

Battery Life vs. V_{CC} Supply Voltage



TinyLogic ULP and ULP-A with up to 50% less power consumption can extend your battery life significantly.

$$\text{Battery Life} = (V_{\text{battery}} \cdot I_{\text{battery}} \cdot 9) / (P_{\text{device}}) / 24 \text{hrs/day}$$

$$\text{Where, } P_{\text{device}} = (I_{CC} \cdot V_{CC}) + (C_{PD} + C_L) \cdot V_{CC}^2 \cdot f$$

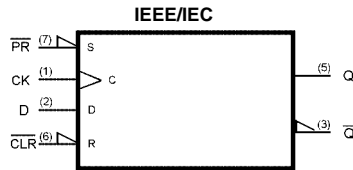
Assumes ideal 3.6V Lithium Ion battery with current rating of 900mAh and derated 90% and device frequency at 10MHz, with $C_L = 15$ pF load

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MicroPak™ and Quiet Series™ are trademarks of Fairchild Semiconductor Corporation.

Pin Descriptions

Pin Names	Description
D	Data Input
CK	Clock Pulse Input
$\overline{\text{CLR}}$	Direct Clear Input
Q, $\overline{\text{Q}}$	Flip-Flop Output
$\overline{\text{PR}}$	Direct Preset Input

Logic Symbol



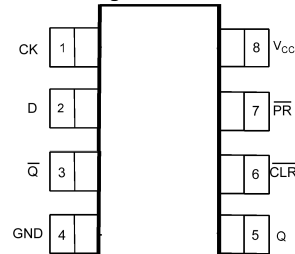
Truth Table

Inputs				Outputs		Function
$\overline{\text{CLR}}$	$\overline{\text{PR}}$	D	CK	Q	$\overline{\text{Q}}$	
L	H	X	X	L	H	Clear
H	L	X	X	H	L	Preset
L	L	X	X	H	H	—
H	H	L	↑	L	H	—
H	H	H	↑	H	L	—
H	H	X	↓	Q_n	\overline{Q}_n	No Change

H = HIGH Logic Level
 L = LOW Logic Level
 Q_n = No change in data
 X = Immaterial
 Z = High Impedance
 ↑ = Rising Edge
 ↓ = Falling edge

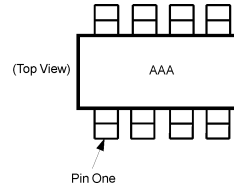
Connection Diagrams

Pin Assignments for US8



(Top View)

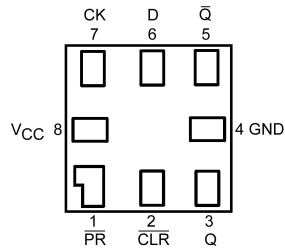
Pin One Orientation Diagram



AAA represents Product Code Top Mark - see ordering code

Note: Orientation of Top Mark determines Pin One location. Read the top product code mark left to right, Pin One is the lower left pin (see diagram).

Pad Assignments for MicroPak



(Top Thru View)

Absolute Maximum Ratings (Note 1)		Recommended Operating Conditions (Note 3)	
Supply Voltage (V_{CC})	-0.5V to +4.6V	Power Supply	0.9V to 3.6V
DC Input Voltage (V_{IN})	-0.5V to +4.6V	Input Voltage (V_{IN})	0V to 3.6V
DC Output Voltage (V_{OUT})	-0.5V to +7.0V	Output Voltage (V_{OUT})	HIGH or LOW State
HIGH or LOW State (Note 2)	-0.5V to $V_{CC} + 0.5V$	HIGH or LOW State	0V to V_{CC}
$V_{CC} = 0V$	-0.5V to 4.6V	$V_{CC} = 0V$	0V to 3.6V
DC Input Diode Current (I_{IK}) $V_{IN} < 0V$	± 50 mA	Output Current in (I_{OH}/I_{OL})	
DC Output Diode Current (I_{OK})		$V_{CC} = 3.0V$ to 3.6V	± 2.6 mA
$V_{OUT} < 0V$	-50 mA	$V_{CC} = 2.3V$ to 2.7V	± 2.1 mA
$V_{OUT} > V_{CC}$	+50 mA	$V_{CC} = 1.65V$ to 1.95V	± 1.5 mA
DC Output Source/Sink Current (I_{OH}/I_{OL})	± 50 mA	$V_{CC} = 1.40V$ to 1.60V	± 1.0 mA
DC V_{CC} or Ground Current per		$V_{CC} = 1.10V$ to 1.30V	± 0.5 mA
Supply Pin (I_{CC} or Ground)	± 50 mA	$V_{CC} = 0.9V$	± 20 μA
Storage Temperature Range (T_{STG})	-65°C to +150°C	Free Air Operating Temperature (T_A)	-40°C to +85°C
		Minimum Input Edge Rate ($\Delta t/\Delta V$)	
		$V_{IN} = 0.8V$ to 2.0V, $V_{CC} = 3.0V$	10 ns/V

Note 1: Absolute Maximum Ratings: are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the Electrical Characteristics tables are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Note 2: I_O Absolute Maximum rating must be observed.

Note 3: Unused inputs must be held HIGH or LOW. They may not float.

DC Electrical Characteristics

Symbol	Parameter	V_{CC} (V)	$T_A = +25^\circ C$		$T_A = -40^\circ C$ to $+85^\circ C$		Units	Conditions
			Min	Max	Min	Max		
V_{IH}	HIGH Level Input Voltage	0.90	0.65 x V_{CC}		0.65 x V_{CC}		V	
		$1.10 \leq V_{CC} \leq 1.30$	0.65 x V_{CC}		0.65 x V_{CC}			
		$1.40 \leq V_{CC} \leq 1.60$	0.65 x V_{CC}		0.65 x V_{CC}			
		$1.65 \leq V_{CC} \leq 1.95$	0.65 x V_{CC}		0.65 x V_{CC}			
		$2.30 \leq V_{CC} \leq 2.70$	1.6		1.6			
		$3.00 \leq V_{CC} \leq 3.60$	2.1		2.1			
V_{IL}	LOW Level Input Voltage	0.90		0.35 x V_{CC}		0.35 x V_{CC}	V	
		$1.10 \leq V_{CC} \leq 1.30$		0.35 x V_{CC}		0.35 x V_{CC}		
		$1.40 \leq V_{CC} \leq 1.60$		0.35 x V_{CC}		0.35 x V_{CC}		
		$1.65 \leq V_{CC} \leq 1.95$		0.35 x V_{CC}		0.35 x V_{CC}		
		$2.30 \leq V_{CC} \leq 2.70$		0.7		0.7		
		$3.00 \leq V_{CC} \leq 3.60$		0.9	0.9			
V_{OH}	HIGH Level Output Voltage	0.90	$V_{CC} - 0.1$		$V_{CC} - 0.1$		V	$I_{OH} = -20 \mu A$
		$1.10 \leq V_{CC} \leq 1.30$	$V_{CC} - 0.1$		$V_{CC} - 0.1$			
		$1.40 \leq V_{CC} \leq 1.60$	$V_{CC} - 0.1$		$V_{CC} - 0.1$			
		$1.65 \leq V_{CC} \leq 1.95$	$V_{CC} - 0.1$		$V_{CC} - 0.1$			
		$2.30 \leq V_{CC} \leq 2.70$	$V_{CC} - 0.1$		$V_{CC} - 0.1$			
		$3.00 \leq V_{CC} \leq 3.60$	$V_{CC} - 0.1$		$V_{CC} - 0.1$			
		$1.10 \leq V_{CC} \leq 1.30$	0.75 x V_{CC}		0.70 x V_{CC}			
		$1.40 \leq V_{CC} \leq 1.60$	1.07		0.99			
		$1.65 \leq V_{CC} \leq 1.95$	1.24		1.22			
$2.30 \leq V_{CC} \leq 2.70$	1.95		1.87					
		$3.00 \leq V_{CC} \leq 3.60$	2.61		2.55			

DC Electrical Characteristics (Continued)

Symbol	Parameter	V _{CC} (V)	T _A = +25°C		T _A = -40°C to +85°C		Units	Conditions
			Min	Max	Min	Max		
V _{OL}	LOW Level Output Voltage	0.90		0.1		0.1	V	I _{OL} = 20 μA
		1.10 ≤ V _{CC} ≤ 1.30		0.1		0.1		
		1.40 ≤ V _{CC} ≤ 1.60		0.1		0.1		
		1.65 ≤ V _{CC} ≤ 1.95		0.1		0.1		
		2.30 ≤ V _{CC} ≤ 2.70		0.1		0.1		
		3.00 ≤ V _{CC} ≤ 3.60		0.1		0.1		
		1.10 ≤ V _{CC} ≤ 1.30		0.30 × V _{CC}		0.30 × V _{CC}		
		1.40 ≤ V _{CC} ≤ 1.60		0.31		0.37		
		1.65 ≤ V _{CC} ≤ 1.95		0.31		0.35		
2.30 ≤ V _{CC} ≤ 2.70		0.31		0.33				
3.00 ≤ V _{CC} ≤ 3.60		0.31		0.33				
I _{IN}	Input Leakage Current	0.90 to 3.60		±0.1		±0.5	μA	0 ≤ V _I ≤ 3.6V
I _{OFF}	Power Off Leakage Current	0		0.5		0.5	μA	0 ≤ (V _I , V _O) ≤ 3.6V
I _{CC}	Quiescent Supply Current	0.90 to 3.60		0.9		0.9	μA	V _I = V _{CC} or GND

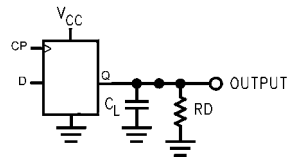
AC Electrical Characteristics (10pF, 1MΩ)										
Symbol	Parameter	V _{CC} (V)	T _A = +25°C			T _A = -40°C to +85°C		Units	Conditions	Figure Number
			Min	Typ	Max	Min	Max			
f _{MAX}	Maximum Clock Frequency	0.90		40.0				MHz	C _L = 10 pF R _D = 1 MΩ	Figures 1, 5
		1.10 ≤ V _{CC} ≤ 1.30	50			50				
		1.40 ≤ V _{CC} ≤ 1.60	75			75				
		1.65 ≤ V _{CC} ≤ 1.95	100			100				
		2.30 ≤ V _{CC} ≤ 2.70	125			125				
3.00 ≤ V _{CC} ≤ 3.60	150			150						
t _{PLH} t _{PHL}	Propagation Delay CK to Q, \bar{Q}	0.90		24.0				ns	C _L = 10 pF R _D = 1 MΩ	Figures 1, 3
		1.10 ≤ V _{CC} ≤ 1.30	4.0	15.0	22.0	3.5	31.0			
		1.40 ≤ V _{CC} ≤ 1.60	2.0	9.0	13.0	1.5	14.0			
		1.65 ≤ V _{CC} ≤ 1.95	1.5	7.0	11.0	1.0	13.0			
		2.30 ≤ V _{CC} ≤ 2.70	1.0	5.0	8.0	0.8	9.0			
3.00 ≤ V _{CC} ≤ 3.60	1.0	4.0	7.0	0.5	8.0					
t _{PLH} t _{PHL}	Propagation Delay $\overline{\text{CLR}}$, $\overline{\text{PR}}$, to Q, \bar{Q}	0.90		6.5				ns	C _L = 10 pF R _D = 1 MΩ	Figures 1, 3
		1.10 ≤ V _{CC} ≤ 1.30	4.0	12.0	23.0	4.0	34.0			
		1.40 ≤ V _{CC} ≤ 1.60	2.0	9.0	12.0	2.0	14.0			
		1.65 ≤ V _{CC} ≤ 1.95	1.5	7.0	11.0	1.5	13.0			
		2.30 ≤ V _{CC} ≤ 2.70	1.0	5.0	9.0	1.0	9.0			
3.00 ≤ V _{CC} ≤ 3.60	1.0	4.0	7.0	1.0	8.0					
t _S	Setup Time, CK to D	0.90		10.0				ns	C _L = 10 pF R _D = 1 MΩ	Figures 1, 4
		1.10 ≤ V _{CC} ≤ 1.30	7.0			7.0				
		1.40 ≤ V _{CC} ≤ 1.60	3.0			3.0				
		1.65 ≤ V _{CC} ≤ 1.95	2.0			2.0				
		2.30 ≤ V _{CC} ≤ 2.70	1.5			1.5				
3.00 ≤ V _{CC} ≤ 3.60	1.0			1.0						
t _H	Hold Time, CK to D	0.90		1.0				ns	C _L = 10 pF R _D = 1 MΩ	Figures 1, 4
		1.10 ≤ V _{CC} ≤ 1.30	0.5			0.5				
		1.40 ≤ V _{CC} ≤ 1.60	0.5			0.5				
		1.65 ≤ V _{CC} ≤ 1.95	0.5			0.5				
		2.30 ≤ V _{CC} ≤ 2.70	0.5			0.5				
3.00 ≤ V _{CC} ≤ 3.60	0.5			0.5						
t _W	Pulse Width, CK, $\overline{\text{PR}}$, $\overline{\text{CLR}}$	0.90		5.0				ns	C _L = 10 pF R _D = 1 MΩ	Figures 1, 5
		1.10 ≤ V _{CC} ≤ 1.30	5.0			5.0				
		1.40 ≤ V _{CC} ≤ 1.60	3.0			3.0				
		1.65 ≤ V _{CC} ≤ 1.95	2.5			2.5				
		2.30 ≤ V _{CC} ≤ 2.70	2.5			2.5				
3.00 ≤ V _{CC} ≤ 3.60	2.0			2.0						
t _{REC}	Recover Time $\overline{\text{CLR}}$, $\overline{\text{PR}}$ to CK	0.90		12.0				ns	C _L = 10 pF R _D = 1 MΩ	Figures 1, 4
		1.10 ≤ V _{CC} ≤ 1.30	8.5			8.5				
		1.40 ≤ V _{CC} ≤ 1.60	3.5			3.5				
		1.65 ≤ V _{CC} ≤ 1.95	3.0			3.0				
		2.30 ≤ V _{CC} ≤ 2.70	2.5			2.5				
3.00 ≤ V _{CC} ≤ 3.60	2.0			2.0						

AC Electrical Characteristics (15pF, 1MΩ)										
Symbol	Parameter	V _{CC} (V)	T _A = +25°C			T _A = -40°C to +85°C		Units	Conditions	Figure Number
			Min	Typ	Max	Min	Max			
f _{MAX}	Maximum Clock Frequency	0.90		40.0				MHz	C _L = 15 pF R _D = 1 MΩ	Figures 1, 5
		1.10 ≤ V _{CC} ≤ 1.30	50			150				
		1.40 ≤ V _{CC} ≤ 1.60	75			200				
		1.65 ≤ V _{CC} ≤ 1.95	100			250				
		2.30 ≤ V _{CC} ≤ 2.70	125			175				
3.00 ≤ V _{CC} ≤ 3.60	150			200						
t _{PLH} t _{PHL}	Propagation Delay CK to Q, \bar{Q}	0.90		27.0			ns	C _L = 15 pF R _D = 1 MΩ	Figures 1, 3	
		1.10 ≤ V _{CC} ≤ 1.30	5.0	16.0	23.0	4.5				34.0
		1.40 ≤ V _{CC} ≤ 1.60	3.0	10.0	14.0	2.5				16.0
		1.65 ≤ V _{CC} ≤ 1.95	2.0	7.0	11.0	2.0				13.0
		2.30 ≤ V _{CC} ≤ 2.70	1.5	5.0	8.0	1.0				9.0
3.00 ≤ V _{CC} ≤ 3.60	1.0	4.0	7.0	0.5	8.0					
t _{PLH} t _{PHL}	Propagation Delay \overline{CLR} , \overline{PR} , to Q, \bar{Q}	0.90		27.0			ns	C _L = 15 pF R _D = 1 MΩ	Figures 1, 3	
		1.10 ≤ V _{CC} ≤ 1.30	5.0	15.0	24.0	5.0				37.0
		1.40 ≤ V _{CC} ≤ 1.60	3.0	10.0	13.0	3.0				16.0
		1.65 ≤ V _{CC} ≤ 1.95	2.0	7.0	11.0	2.0				13.0
		2.30 ≤ V _{CC} ≤ 2.70	1.5	5.0	9.0	1.5				9.0
3.00 ≤ V _{CC} ≤ 3.60	1.0	4.0	7.0	1.0	8.0					
t _S	Setup Time, CK to D	0.90		10.0			ns	C _L = 15 pF R _D = 1 MΩ	Figures 1, 4	
		1.10 ≤ V _{CC} ≤ 1.30	7.0			7.0				
		1.40 ≤ V _{CC} ≤ 1.60	3.0			3.0				
		1.65 ≤ V _{CC} ≤ 1.95	2.0			2.0				
		2.30 ≤ V _{CC} ≤ 2.70	1.5			1.5				
3.00 ≤ V _{CC} ≤ 3.60	1.0			1.0						
t _H	Hold Time, CK to D	0.90		1.0			ns	C _L = 15 pF R _D = 1 MΩ	Figures 1, 4	
		1.10 ≤ V _{CC} ≤ 1.30	0.5			0.5				
		1.40 ≤ V _{CC} ≤ 1.60	0.5			0.5				
		1.65 ≤ V _{CC} ≤ 1.95	0.5			0.5				
		2.30 ≤ V _{CC} ≤ 2.70	0.5			0.5				
3.00 ≤ V _{CC} ≤ 3.60	0.5			0.5						
t _W	Pulse Width, CK, \overline{PR} , \overline{CLR}	0.90		5.0			ns	C _L = 15 pF R _D = 1 MΩ	Figures 1, 5	
		1.10 ≤ V _{CC} ≤ 1.30	5.0			5.0				
		1.40 ≤ V _{CC} ≤ 1.60	3.0			3.0				
		1.65 ≤ V _{CC} ≤ 1.95	2.5			2.5				
		2.30 ≤ V _{CC} ≤ 2.70	2.5			2.5				
3.00 ≤ V _{CC} ≤ 3.60	2.0			2.0						
t _{REC}	Recover Time \overline{CLR} , \overline{PR} to CK	0.90		12.0			ns	C _L = 15 pF R _D = 1 MΩ	Figures 1, 4	
		1.10 ≤ V _{CC} ≤ 1.30	8.5			8.5				
		1.40 ≤ V _{CC} ≤ 1.60	3.5			3.5				
		1.65 ≤ V _{CC} ≤ 1.95	3.0			3.0				
		2.30 ≤ V _{CC} ≤ 2.70	2.5			2.5				
3.00 ≤ V _{CC} ≤ 3.60	2.0			2.0						

AC Electrical Characteristics (30pF, 1MΩ)										
Symbol	Parameter	V _{CC} (V)	T _A = +25°C			T _A = -40°C to +85°C		Units	Conditions	Figure Number
			Min	Typ	Max	Min	Max			
f _{MAX}	Maximum Clock Frequency	0.90		40.0				MHz	C _L = 30 pF R _D = 1 MΩ	Figures 1, 5
		1.10 ≤ V _{CC} ≤ 1.30	50			150				
		1.40 ≤ V _{CC} ≤ 1.60	75			200				
		1.65 ≤ V _{CC} ≤ 1.95	100			250				
		2.30 ≤ V _{CC} ≤ 2.70	125			175				
3.00 ≤ V _{CC} ≤ 3.60	150			200						
t _{PLH} t _{PHL}	Propagation Delay CK to Q, \bar{Q}	0.90		34.0				ns	C _L = 30 pF R _D = 1 MΩ	Figures 1, 3
		1.10 ≤ V _{CC} ≤ 1.30	6.0	18.0	27.0	5.0	43.0			
		1.40 ≤ V _{CC} ≤ 1.60	4.0	11.0	17.0	3.0	18.0			
		1.65 ≤ V _{CC} ≤ 1.95	2.0	8.0	13.0	2.0	15.0			
		2.30 ≤ V _{CC} ≤ 2.70	1.0	6.0	10.0	1.0	11.0			
3.00 ≤ V _{CC} ≤ 3.60	0.8	5.0	8.0	0.5	10.0					
t _{PLH} t _{PHL}	Propagation Delay $\overline{\text{CLR}}$, $\overline{\text{PR}}$, to Q, \bar{Q}	0.90		34.0				ns	C _L = 30 pF R _D = 1 MΩ	Figures 1, 3
		1.10 ≤ V _{CC} ≤ 1.30	6.0	17.0	28.0	5.5	46.0			
		1.40 ≤ V _{CC} ≤ 1.60	4.0	11.0	16.0	3.5	18.0			
		1.65 ≤ V _{CC} ≤ 1.95	2.0	8.0	13.0	2.5	15.0			
		2.30 ≤ V _{CC} ≤ 2.70	1.0	6.0	9.0	1.5	11.0			
3.00 ≤ V _{CC} ≤ 3.60	0.8	5.0	8.0	1.0	10.0					
t _S	Setup Time, CK to D	0.90		10.0				ns	C _L = 30 pF R _D = 1 MΩ	Figures 1, 4
		1.10 ≤ V _{CC} ≤ 1.30	7.0			7.0				
		1.40 ≤ V _{CC} ≤ 1.60	3.0			3.0				
		1.65 ≤ V _{CC} ≤ 1.95	2.0			2.0				
		2.30 ≤ V _{CC} ≤ 2.70	1.5			1.5				
3.00 ≤ V _{CC} ≤ 3.60	1.0			1.0						
t _H	Hold Time, CK to D	0.90		1.0				ns	C _L = 30 pF R _D = 1 MΩ	Figures 1, 4
		1.10 ≤ V _{CC} ≤ 1.30	0.5			0.5				
		1.40 ≤ V _{CC} ≤ 1.60	0.5			0.5				
		1.65 ≤ V _{CC} ≤ 1.95	0.5			0.5				
		2.30 ≤ V _{CC} ≤ 2.70	0.5			0.5				
3.00 ≤ V _{CC} ≤ 3.60	0.5			0.5						
t _W	Pulse Width, CK, $\overline{\text{PR}}$, $\overline{\text{CLR}}$	0.90		5.0				ns	C _L = 30 pF R _D = 1 MΩ	Figures 1, 5
		1.10 ≤ V _{CC} ≤ 1.30	5.0			4.0				
		1.40 ≤ V _{CC} ≤ 1.60	3.0			3.0				
		1.65 ≤ V _{CC} ≤ 1.95	2.5			2.0				
		2.30 ≤ V _{CC} ≤ 2.70	2.5			3.0				
3.00 ≤ V _{CC} ≤ 3.60	2.0			2.0						
t _{REC}	Recover Time $\overline{\text{CLR}}$, $\overline{\text{PR}}$ to CK	0.90		12.0				ns	C _L = 30 pF R _D = 1 MΩ	Figures 1, 4
		1.10 ≤ V _{CC} ≤ 1.30	8.5			8.5				
		1.40 ≤ V _{CC} ≤ 1.60	3.5			3.5				
		1.65 ≤ V _{CC} ≤ 1.95	3.0			3.0				
		2.30 ≤ V _{CC} ≤ 2.70	2.5			2.5				
3.00 ≤ V _{CC} ≤ 3.60	2.0			2.0						

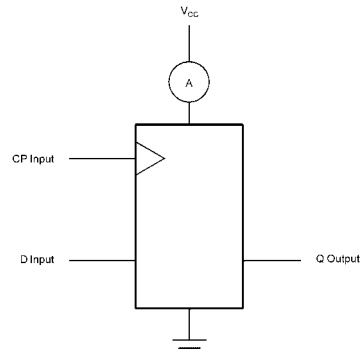
Capacitance						
Symbol	Parameter	Typ	Max	Units	Conditions	Figure Number
C _{IN}	Input Capacitance	2.0		pF	V _{CC} = 0V	
C _{OUT}	Output Capacitance	4.0		pF	V _{CC} = 0V	
C _{PD}	Power Dissipation Capacitance	8.0		pF	V _I = 0V or V _{CC} f = 10 MHz	Figure 2

AC Loading and Waveforms



C_L includes load and stray capacitance
 Input PRR = 1.0 MHz; $t_w = 500$ ns

FIGURE 1. AC Test Circuit



CP Input = AC Waveform; $t_r = t_f = 2.5$ ns;
 CP Input PRR = 10 MHz; Duty Cycle = 50%
 D Input PRR = 5MHz; Duty Cycle = 50%

FIGURE 2. I_{CCD} Test Circuit

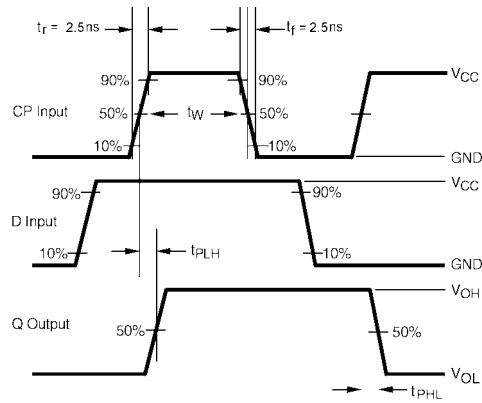


FIGURE 3. AC Waveforms

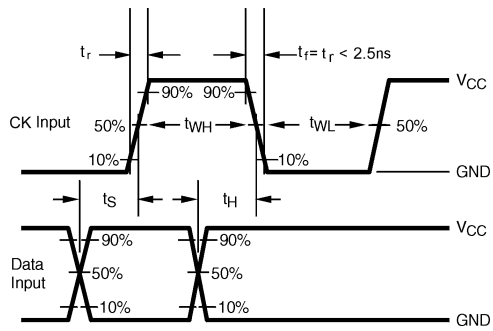


FIGURE 4. AC Waveforms

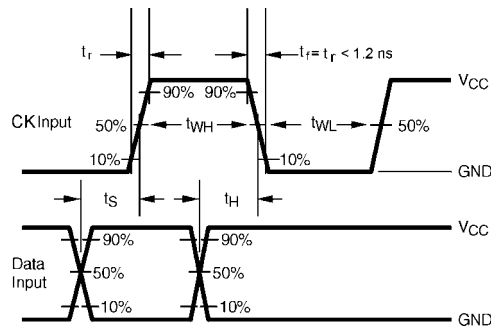


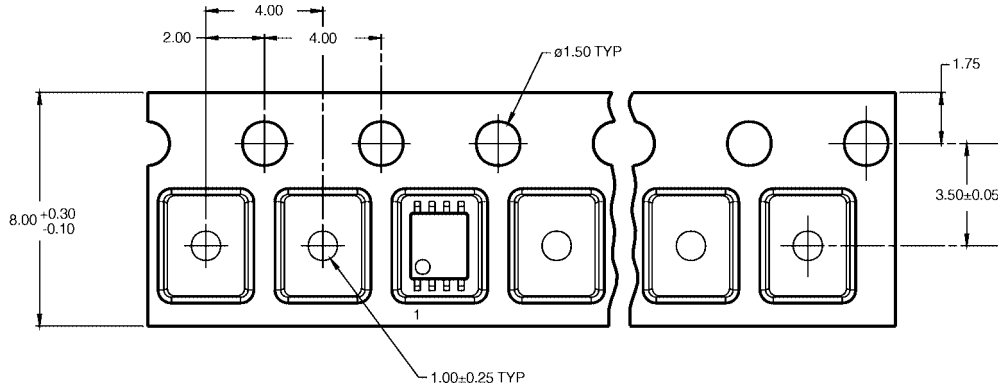
FIGURE 5. AC Waveforms

Tape and Reel Specification

TAPE FORMAT for US8

Package Designator	Tape Section	Number Cavities	Cavity Status	Cover Tape Status
K8X	Leader (Start End)	125 (typ)	Empty	Sealed
	Carrier	3000	Filled	Sealed
	Trailer (Hub End)	75 (typ)	Empty	Sealed

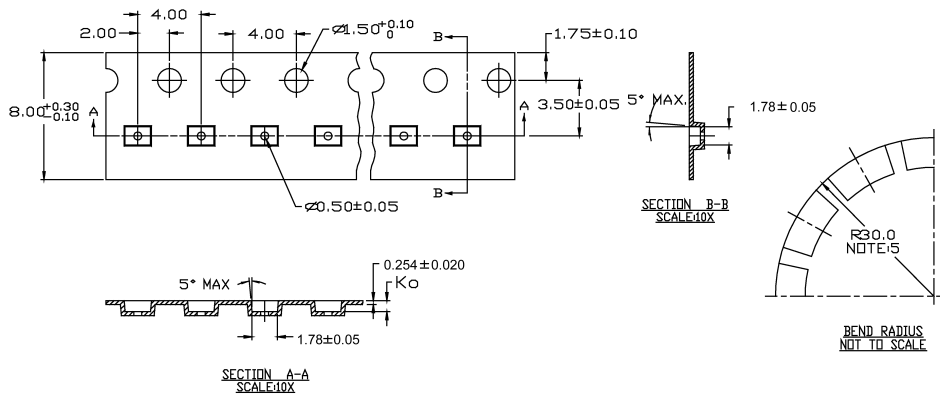
TAPE DIMENSIONS inches (millimeters)



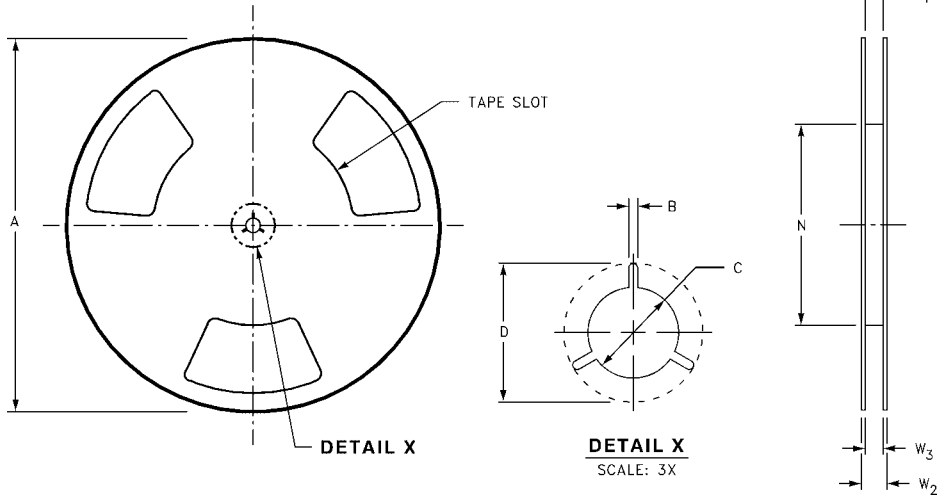
TAPE FORMAT for MicroPak

Package Designator	Tape Section	Number Cavities	Cavity Status	Cover Tape Status
L8X	Leader (Start End)	125 (typ)	Empty	Sealed
	Carrier	3000	Filled	Sealed
	Trailer (Hub End)	75 (typ)	Empty	Sealed

TAPE DIMENSIONS inches (millimeters)

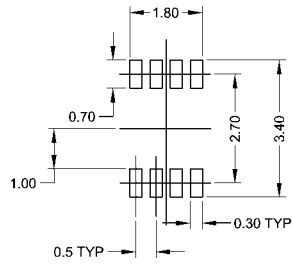
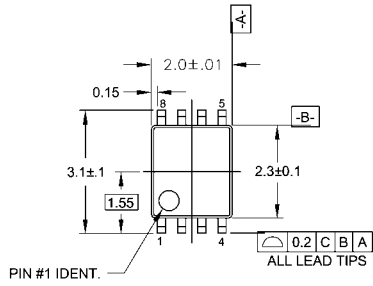


Tape and Reel Specification (Continued)
REEL DIMENSIONS inches (millimeters)

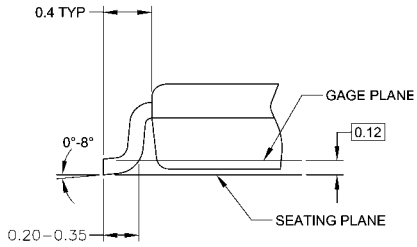
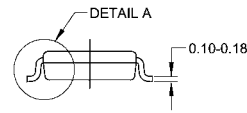
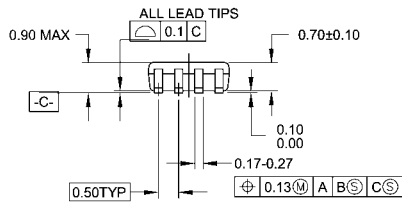


Tape Size	A	B	C	D	N	W1	W2	W3
8 mm	7.0 (177.8)	0.059 (1.50)	0.512 (13.00)	0.795 (20.20)	2.165 (55.00)	$0.331 + 0.059/-0.000$ ($8.40 + 1.50/-0.00$)	0.567 (14.40)	$W1 + 0.078/-0.039$ ($W1 + 2.00/-1.00$)

Physical Dimensions inches (millimeters) unless otherwise noted



LAND PATTERN RECOMMENDATION



DETAIL A

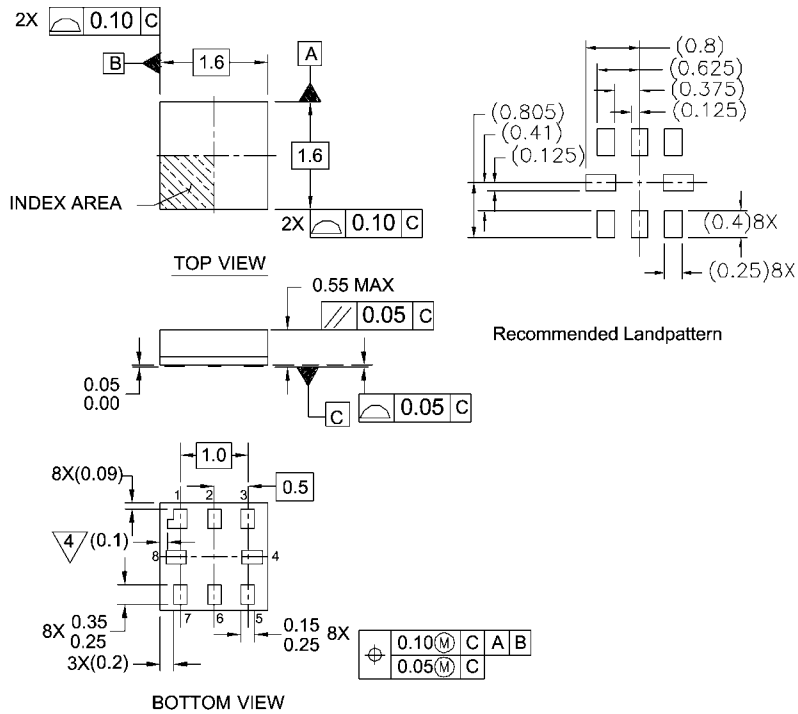
NOTES:

- A. CONFORMS TO JEDEC REGISTRATION MO-187
- B. DIMENSIONS ARE IN MILLIMETERS.
- C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.
- D. DIMENSIONS AND TOLERANCES PER ANSI Y14.5M, 1982.

MAB08AREVC

**8-Lead US8, JEDEC MO-187, Variation CA 3.1mm Wide
Package Number MAB08A**

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



Notes:

1. PACKAGE CONFORMS TO JEDEC MO-255 VARIATION UAAD
2. DIMENSIONS ARE IN MILLIMETERS
3. DRAWING CONFORMS TO ASME Y.14M-1994
4. PIN 1 FLAG, END OF PACKAGE OFFSET.

MAC08AREVC

**Pb-Free 8-Lead MicroPak, 1.6 mm Wide
Package Number MAC08A**

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2. A critical component in any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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