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DS14C89A/DS14C89AT
Quad CMOS Receiver

General Description

The DS14C89A/DS14C89AT, pin-for-pin compatible to the DS1489A/MC1489A, are receivers designed to interface data terminal equipment (DTE) with data circuit-terminating equipment (DCE). These devices translate levels conforming to EIA-232E and CCITT V.28 standards to TTL/CMOS logic levels.

The device is fabricated in low threshold CMOS metal gate technology. The device provides very low power consumption compared to their bipolar equivalents: 900 μA (DS14C89A) versus 26 mA (DS1489A).

The DS14C89A/DS14C89AT provide on chip noise filtering which eliminates the need for external response control filter capacitors. When replacing the DS1489A with the DS14C89A/DS14C89AT, the response control filter pins can be tied high, low, or not connected.

Features

- Meets EIA/TIA-232-E and CCITT V.28 Standards
- Industrial Temperature Range
  −40°C to +85°C–DS14C89AT
- LOW Power consumption
- On chip noise filter
- Available in SOIC Package

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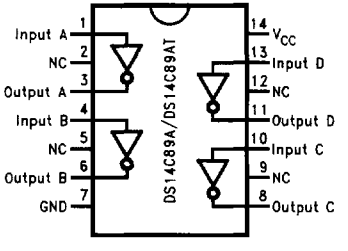
Connection Diagram



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Order Number DS14C89AN, DS14C89AM, DS14C89ATJ, DS14C89ATN, DS14C89ATM
See NS Package Number J14A, M14A, N14A

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

V_{CC}	+6V
Input Voltage	−30V to +30V
Receiver Output Voltage	(V_{CC}) +0.3V to GND−0.3V
Junction Temperature	+150°C
Continuous Power Dissipation @ +25°C (Note 2)	
N Package	1513 mW
J Package	1935 mW
M Package	1063 mW
Lead Temp. (Soldering 4 seconds)	+260°C
Storage Temp. Range	−65°C to +150°C
ESD Rating ≥ 1.8 kV, Typically ≥ 2 kV (HMB, 1.5 kΩ, 100 pF)	

Recommended Operating Conditions

	Min	Max	Units
V_{CC} (GND = 0V)	+4.5	+5.5	V
Operating Free Air Temp. (T_A)			
DS14C89A	0	+75	°C
DS14C89AT	−40	+85	°C

Electrical Characteristics Over recommended operating conditions, unless otherwise specified

Symbol	Parameter	Conditions			Min	Typ	Max	Units
V_{TH}	Input High Threshold				1.3		2.7	V
V_{TL}	Input Low Threshold				0.5		1.9	V
V_{HY}	Typical Input Hysteresis					1.0		V
I_{IN}	Input Current	V_{IN} = +25V	V_{CC} = +4.5V to +5.5V		3.6		8.3	mA
		V_{IN} = −25V			−3.6		−8.3	mA
		V_{IN} = +3V			0.43		1.0	mA
		V_{IN} = −3V			−0.43		−1.0	mA
		V_{IN} = +15V	V_{CC} = 0V (Power-Off) (Note 4)		2.14		5.0	mA
		V_{IN} = −15V			−2.14		−5.0	mA
		V_{IN} = +3V			0.43		1.0	mA
		V_{IN} = −3V			−0.43		−1.0	mA
V_{OH}	Output High Voltage	V_{IN} = V_{TL} (min)	I_{OUT} = −3.2 mA		2.8	4.0		V
			I_{OUT} = −20μA		3.5	4.7		V
V_{OL}	Output Low Voltage	V_{IN} = V_{TH} (max) I_{OUT} = +3.2 mA				0.15	0.4	V
I_{CC}	Supply Current	No Load V_{IN} = 2.7V or 0.5V		DS14C89A		0.5	900	μA
				DS14C89AT		0.5	2.0	mA

AC Electrical Characteristics

Over recommended operating conditions, unless otherwise specified, C_l = 50 pF (Note 3)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{PLH}	Propagation Delay Low to High	Input Pulse Width ≥ 10 μs		3.5	6.5	μs
t_{PHL}	Propagation Delay High to Low	Input Pulse Width ≥ 10 μs		3.2	6.5	μs
t_{SK}	Typical Propagation Delay Skew			400		ns
t_r	Output Rise Time			40	300	ns
t_f	Output Fall Time			40	300	ns
t_{nw}	Pulse Width assumed to be Noise				1.0	μs

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The tables of "Electrical Characteristics" specify conditions for device operation.

Note 2: Derate N Package 12.1 mW/°C, J Package 12.9 mW/°C, and M Package 8.5 mW/°C above +25°C.

Note 3: AC input waveforms for test purposes: t_r = t_f = 200 ns, V_{IH} = +3V, V_L = −3V, f = 20 KHz.

Note 4: Under the power-off supply conditions it is assumed that the power supply potential drops to zero (0V) and is replaced by a low impedance or short circuit to ground.

Parameter Measurement Information

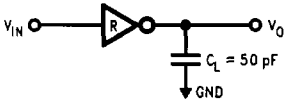

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FIGURE 1. Receiver Load Circuit

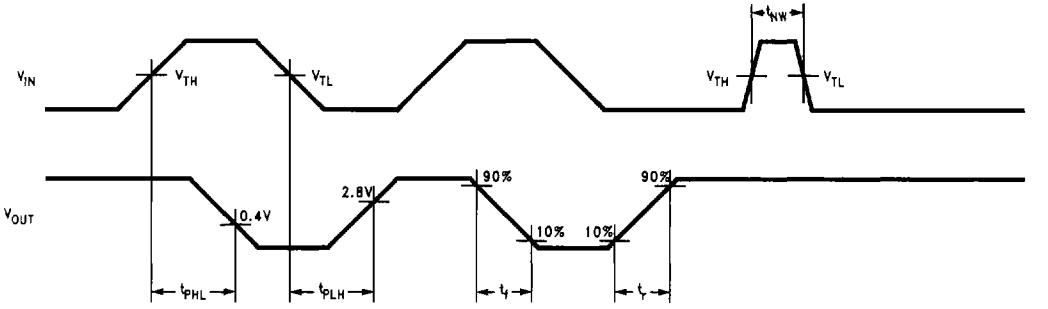

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FIGURE 2. Receiver Switching Waveform (Note 3)

Typical Application Information

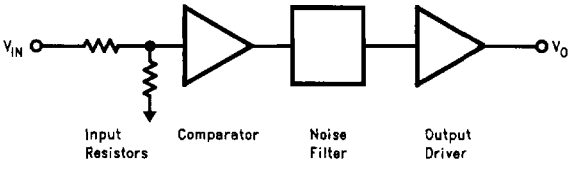

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FIGURE 3. Receiver Block Diagram

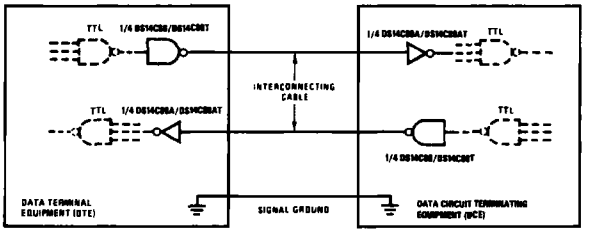

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FIGURE 4. EIA-232D Data Transmission