ICL7182
101 Segment LCD Bargraph A/D Converter

GENERAL DESCRIPTION

The Harris ICL7182 is a complete analog-to-digital converter (ADC) that directly drives a multiplexed liquid crystal display (LCD). Included are a charge-balanced ADC, a 2.56V bandgap reference, display decode and driver, and a 50 kHz oscillator. Only a display and three passive components are required for a complete analog bargraph.

The fully differential analog and reference inputs may be operated anywhere between and including the supply rails. This allows sensing either ground-referenced signals or bridge configurations. Linearity and zero offset errors are guaranteed to be less than 0.5% for a 1V full-scale input. The full-scale differential input range is 200 mV to 1.1V.

The low drift 50 ppm/°C reference is trimmed to 1.5% accuracy and, when used with a simple resistor divider, can set the full-scale input voltage. The reference, when used with an Harris ICL7660, extends the operating supply range from 3V to 40V and allows sensing input signals below ground.

The backplane and segment drivers supply the LCD with the proper waveforms to create a discrete series of segments forming a 101 segment bar which is proportional to the input voltage, with a plus or minus annunciator to indicate the polarity. In addition, three independent TTL controllable annunciators are provided for limit or unit indication. The bargraph multiplexing scheme provides duplex contrast ratio and allows the complete system to be placed in a standard 40 pin DIP. The LCD operating voltage is externally set to adjust contrast for a range of fluid types and temperature.

The internal oscillator requires no external components and establishes the conversion rate and backplane clock frequency. The nominal conversion rate of 25 per second can be easily changed between 15 to 40 conversions per second by adding a single capacitor or overdriving the oscillator.

FEATURES

- **1% Resolution ... 100 Data Segments Plus Zero**
- **No Missing Segments Guaranteed**
- **Single 5V Supply Operation**
- **Only Three Passive Components Required**
- **True Differential Input and Reference**
- **Direct LCD Display Drive Provides Duplex Contrast Ratio**
- **Overrange and Polarity Indication**
- **Three User Defined Annunciators—Easily Expandable**
- **Precision On-Chip Reference ... 50 ppm/°C**
- **Low Average Power Consumption ... 1.8 mW**
- **40 Pin DIP or 44 Pin Surface Mount Package**
- **Extended Temperature Range Operation**

ORDERING INFORMATION

Part Number	Temperature Range	Package Description
ICL7182CPL	0°C to +70°C	40-Pin Plastic DIP
ICL7182CM44	0°C to +70°C	44-Pin Surface Mount

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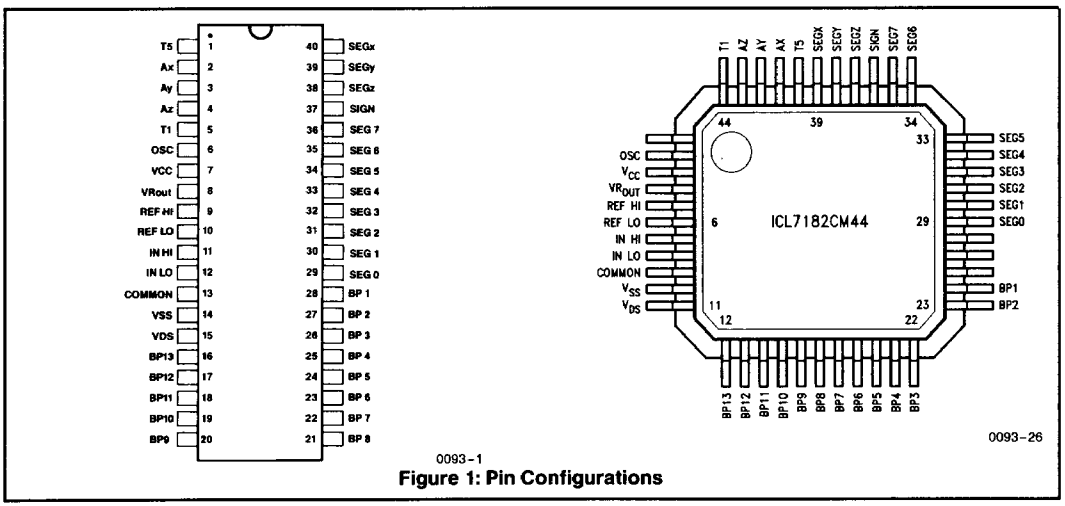


Figure 1: Pin Configurations

310675-002

NOTE: All typical values have been characterized but are not tested.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage (V_{CC} to V_{SS}) 10V
Supply Voltage (V_{CC} to V_{DS}) 11V
Display Drive Pin Voltage ..... (V_{CC} + 0.3V) to (V_{DS} − 0.3V)
Analog or Reference Inputs .... (V_{CC} + 0.3V) to (V_{SS} − 0.3V)
Com, Osc, Ax, Ay,
Az, T1, T5 Pins ..... (V_{CC} + 0.3V) to (V_{SS} − 0.3V)
Reference Output Current ..... 8 mA
Lead Temperature (Soldering, 10 sec) ..... 300°C
Storage Temperature Range ..... −65°C to +150°C
Operating Temperature Range ..... −25°C to +85°C
Continuous Total Power Dissipation (T_A = 25°C)
40 Pin DIP Plastic Package ..... 500 mW
44 Pin CM Plastic Package ..... 375 mW

NOTE: *Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

ELECTRICAL CHARACTERISTICS

Unless otherwise stated: V_{CC} = 5.0V, V_{SS} = V_{DS} = GND, T_A = 25°C, V_{REF} = 1.000V, VIN_{CM} = $VREF_{CM}$ = 2.5V, pin 6 open (Note 1)

Parameter	Test Conditions	Limits			Units
		Min	Typ	Max	
Zero Input Reading	V_{IN} = 0.0V	−0	±0	+0	Segs
Unadjusted Gain Error	V_{IN} = V_{REF}	−1	0	+1	Segs
Linearity Error	(Note 2)	−0.63	±0.2	+0.63	Segs
Rollover Error	V_{IN} = −V_{REF} (Note 3)	−0.5	±0.1	+0.5	Segs
Conversion Time			400		µs
Display Update Rate			25		Hz
Input Referred Noise	(Note 4)		500		µV
DC Power Supply Rejection	V_{CC} = 4.5 to 6.0V		0.02	0.3	Segs/V
ANALOG INPUT					
Common Mode Rejection Ratio	VIN_{CM} = 0V to 5V, V_{IN} ≅ 0V		0.02	0.1	Segs/V
Differential Mode Input			1.0	1.1	V
Average Input Current	V_{IN} = 1.0V (Note 5)		1.3		nA
REFERENCE INPUT					
Common Mode Rejection Ratio	$VREF_{CM}$ = 0.5V to 4.5V		0.01	0.1	Segs/V
Average Input Current	(Note 6)		6		nA
REFERENCE OUTPUT					
Output Voltage	V_{CC} − VRout, Iout = 0 µA	2.520	2.560	2.590	V
Temperature Coefficient	−25°C < T_A < 85°C, Iout = 0 µA		50	200	ppm/°C
Output Impedance	Iout = +10 µA to −2 mA		1.3	5	Ω
Current Into VRout Pin		10	20		µA
Current Out of VRout			8	2	mA
Output Noise	0.1 Hz to 10 Hz (Note 4)		110		µV
POWER SUPPLY					
Supply Current Average	(Note 6)		350	500	µA
Supply Current Peak	(Note 6)		1.5	2.0	mA
Supply Voltage Range	Guaranteed by PSRR	4.5	5.0	6.0	V
OSCILLATOR					
Oscillator Frequency	Osc Pin Open	26	51	72	kHz
Backplane Frequency	Osc Pin Open	25	50	70	Hz
DISPLAY DRIVE					
Display Output Impedance	V_{CC} − V_{DS} = 3V to 7V		70	200	kΩ
DC Component of Display	V_{CC} − V_{DS} = 3V to 7V	−50	±10	50	mV
V_{DS} Supply Current	V_{CC} − V_{DS} = 3V to 7V (Note 7)		60	120	µA

NOTE: All typical values have been characterized but are not tested.

ELECTRICAL CHARACTERISTICS (Continued) Unless otherwise stated: V_{CC} = 5.0V, V_{SS} = V_{DS} = GND, T_A = 25°C, V_{REF} = 1.000V, VIN_{CM} = $VREF_{CM}$ = 2.5V, pin 6 open (Note 1)

Parameter	Test Conditions	Limits			Units
		Min	Typ	Max	
ANNUNCIATOR INPUTS					
Input High Voltage	Operating Temp Range	2.4			V
Input Low Voltage	Operating Temp Range			0.8	V
Input Leakage	Operating Temp Range	−1	0.001	+1	μA

NOTE 1: The differential mode input voltages are defined as: V_{IN} = (IN HI − IN LO) and VREF = (REF HI − REF LO). The common mode input voltage, VIN_{CM} and $VREF_{CM}$, is defined as the average differential input voltage with respect to V_{SS}.

2: The linearity error is the deviation from a straight line which passes through negative full scale and postive full scale readings.

3: The rollover error is defined as the difference in reading for equal positive and negative inputs near full-scale.

4: Peak to peak value not exceeded 95% of the time (±2 standard deviations).

5: Defined as the average current flowing into the input with a 1.0 μF capacitor across V_{IN} or V_{REF} inputs and the common mode voltage at ½ VCC.

6: The average supply current is measured with a supply bypass capacitor and annunciator inputs tied to V_{SS}.

7: The supply current for V_{DS} flows from the V_{CC} pin.

PIN DESCRIPTION AND FUNCTION

Pin No.	Symbol	Description
1	T5	Test pin #5, buffered oscillator frequency divided by two that can typically source and sink 2 mA.
2	Ax	Annunciator Segx select, low turns on Segx, high turns off Segx.
3	Ay	Annunciator Segy select, low turns on Segy, high turns off Segy.
4	Az	Annunciator Segz select, low turns on Segz, high turns off Segz.
5	T1	Test pin #1, normally left open or tied to V_{SS}.
6	Osc	50 kHz free running oscillator control and clock input pin. The internal oscillator may be overdriven by a 30 to 80 kHz external clock driving pin 6, or the free running frequency can be reduced by adding an external capacitor between pin 6 and V_{CC}.
7	V_{CC}	Positive supply voltage.
8	VRout	Bandgap reference buffered output, down 2.56V from V_{CC}.
9	REF HI	Positive Reference Input.
10	REF LO	Negative Reference Input.
11	IN HI	Positive Analog Input.
12	IN LO	Negative Analog Input.
13	Common	Internally generated voltage which is typically within ±50 mV of ½ (V_{CC} − V_{SS}) and has 1.4 kΩ output impedance. This pin is normally left open or bypassed with a 0.1 μF capacitor to signal ground.
14	V_{SS}	Negative supply voltage, normally ground.
15	V_{DS}	Display negative voltage, establishes the pk-pk display drive.
16–28	BP13–BP1	LCD backplane drivers.
29–36	Seg0–Seg7	LCD segment drivers.
37	Sign	Positive sign segment driver.
38	Segz	Annunciator driver selected by Az.
39	Segy	Annunciator driver selected by Ay.
40	Segx	Annunciator driver selected by Ax.

NOTE: All typical values have been characterized but are not tested.

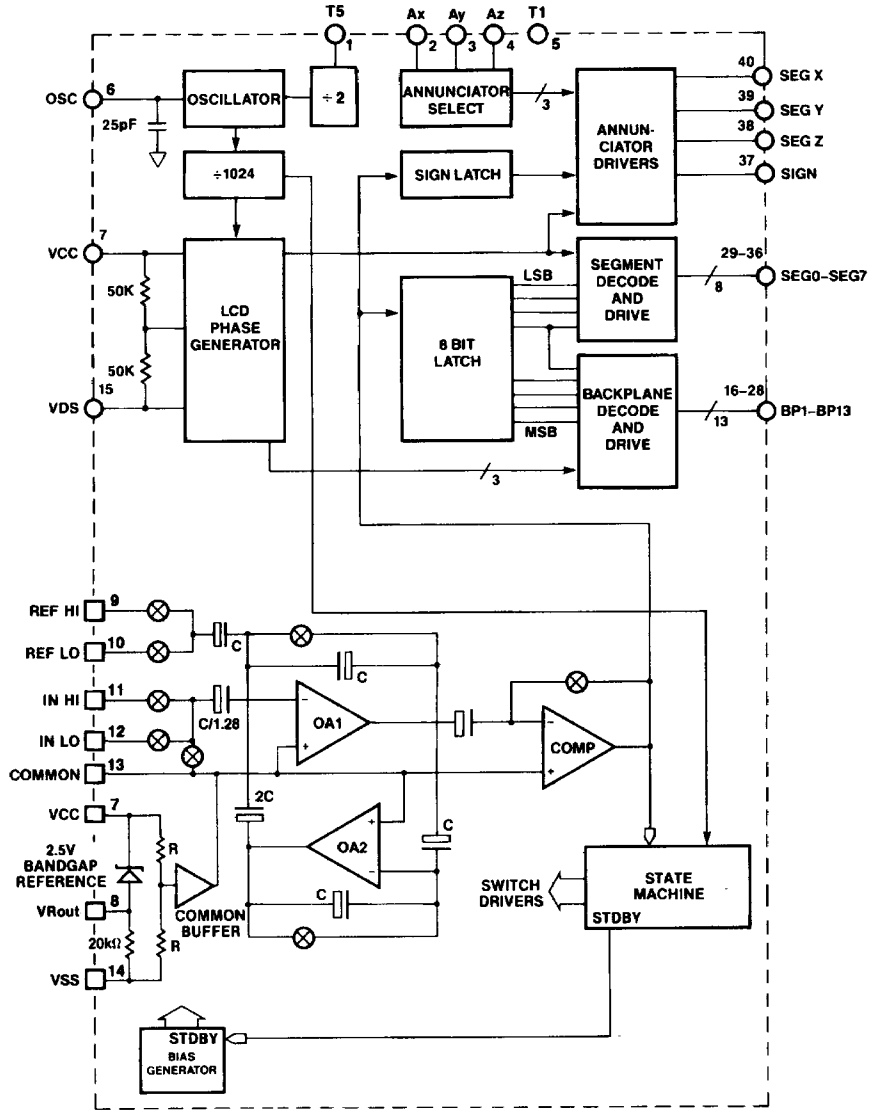


Figure 2: Functional Diagram

NOTE: All typical values have been characterized but are not tested.

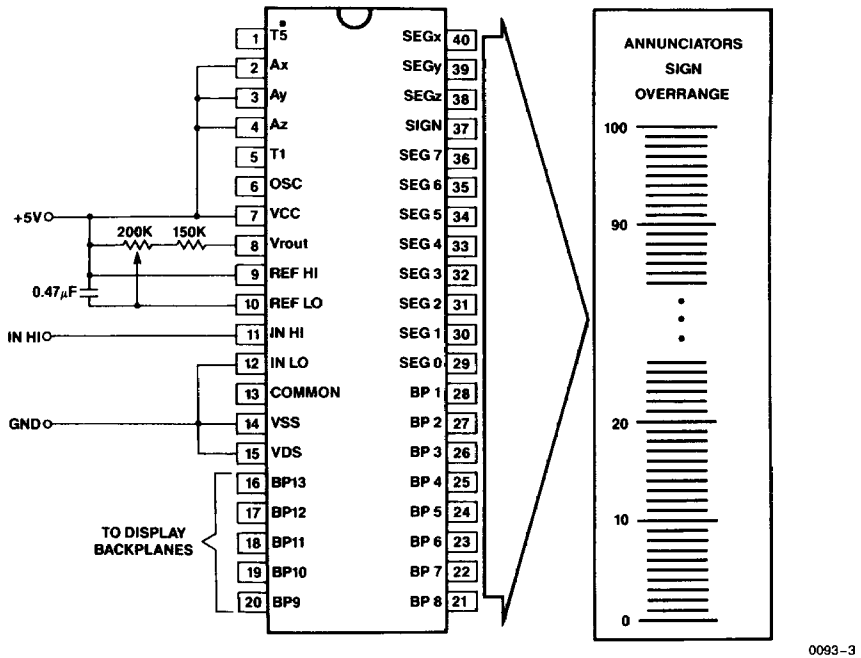
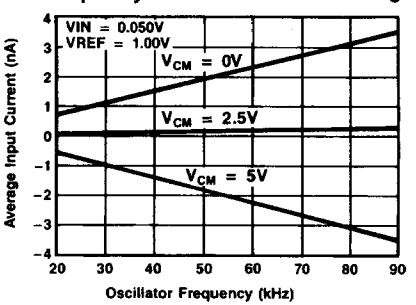


Figure 3: ICL7182 using the internal reference. Values shown are for 1.000V full-scale, 25 readings per second, single 5V supply.

TYPICAL PERFORMANCE CHARACTERISTICS

Average Analog Input Current vs. Frequency and Common Mode Voltage



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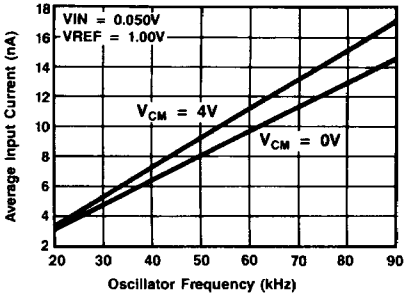
Average Reference Input Current vs. Frequency and Common Mode Voltage



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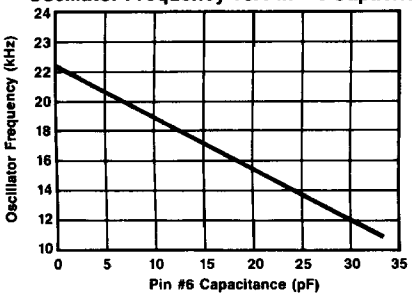
NOTE: All typical values have been characterized but are not tested.

TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

Oscillator Frequency vs. Pin #6 Capacitor



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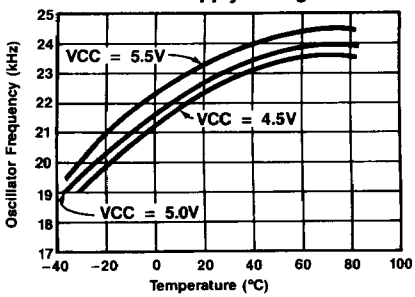
Oscillator Frequency vs. Temperature and Supply Voltage



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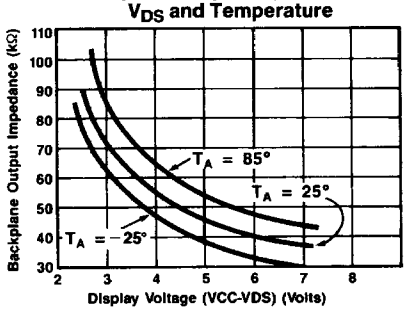
Backplane Output Impedance vs. V_{DS} and Temperature



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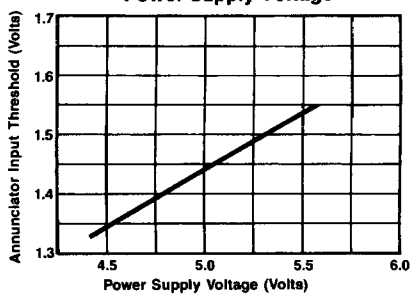
Annunciator Input Threshold vs. Power Supply Voltage



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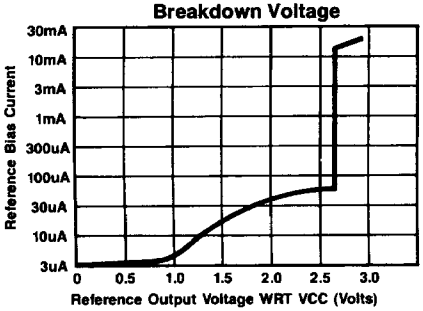
Reference Bias Current vs. Breakdown Voltage



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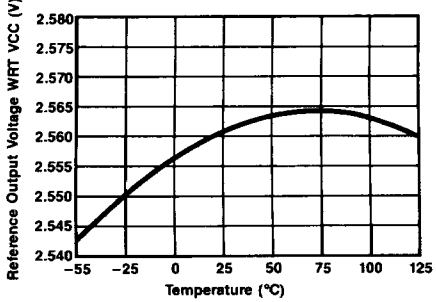
Reference Output vs.Temperature



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NOTE: All typical values have been characterized but are not tested.

FUNCTIONAL DESCRIPTION

A functional diagram of the ICL7182 A/D converter is shown in Figure 2. The device operates on the cyclic converter principle implemented with switched capacitor amplifiers. Analog switches are closed sequentially by state machine control logic to sample the input and perform a multiply-by-two and delay function. The sampled input charge is recirculated and compared to the reference to determine the weight of each bit. The sign is determined first and after 18 cycles a 9-bit binary code is latched and the display is updated.

Under normal operation the conversion requires 32 clock cycles and the display updates once every 2048 clock cycles. Before and during the conversion the supply current for the analog section increases from typically 300 μA to 1.3 mA and remains high for a total of 96 clock cycles. The operation proceeds as follows:

Clock Cycle	Operation
0–96	Supply current increases from 300 μA to 1.3 mA
0–47	Converter autozero begins
48	IN LO is sampled
49	IN HI is sampled
50–70	REF LO and REF HI are sampled once per clock cycle
71–77	Converter output is latched and display is updated
78–2047	Supply current decreases from 1.3 mA to 300 μA
2048	New conversion begins

The changing supply current may result in a noisy reading if the supply dynamic impedance is high. This can be resolved by using a supply bypass capacitor.

Analog Inputs

The analog and reference inputs are guaranteed to correctly operate within the supply voltage. Both inputs will continue to function 200 mV to 400 mV outside of the supplies but the converter specifications degrade as the input protection diodes become forward biased.

As the reference and analog inputs are sampled, transient currents flow from the inputs to charge small internal capacitors.

These transient currents occur at the leading edge of the internal clock and decay at a rate determined by the input capacitance of the converter and the source resistance. Source resistances larger than Rs given in the equation below will cause conversion errors.

$$Rs\ (max) = \frac{1}{6\ (Fosc)\ (Cin)}$$

Where: Fosc = Oscillator frequency
Cin = 40 pF, typical input capacitance
Rs = Source resistance

Input Bypass Capacitor

For source resistances larger than Rs above (typically 80 kΩ) bypass capacitors across the inputs will average these charging currents and cause a small DC current to flow through the output resistance of the analog and reference source signals. The average input current is a function of the common mode voltage and the oscillator frequency (see typical graphs). This current is typically 2 nA for the analog input and 6 nA for the reference input. The effects of the voltage drops across source resistances, due to the average value of input current, can be compensated by full-scale adjustment while the given source resistor and input bypass capacitor are in place.

Reference Output

The internal bandgap reference behaves like a 2.56V zener with the cathode tied to V_{CC} and the anode tied to VRout. The regulator circuitry maintains a low 1.3Ω output impedance for bias currents through the zener between 90 μA and 2 mA. At minimum supply voltage the internal 20 kΩ resistor will provide 10 μA of current sink into VRout. The minimum sink current may be increased by adding an external resistor from VRout to V_{SS}.

The reference is internally trimmed to within 1.5% of 2.56V. The reference output can be externally divided (see Figure 3) to establish the full-scale input. Two fixed value resistors with 1% tolerance will relate to a system accuracy of 2% RMS.

2

NOTE: All typical values have been characterized but are not tested.

Display Drive

The binary output of the A/D converter is encoded to drive 8 segments that serpentine across thirteen backplanes of an LCD display. The backplanes are driven with three level signals and the segment lines are driven with two level signals. The three levels of the backplane are set by the V_{CC} supply, the V_{DS} supply, and the output of a voltage divider which is connected between V_{CC} and V_{DS}. The two levels of the segment drive are set by the V_{CC} and V_{DS} supplies.

The bargraph takes advantage of the fact that above a particular segment all segments will be off and below that segment all segments will be on, also that only one backplane will have segments which are both on and off. The backplanes with all segments off are driven with an "off backplane" waveform, the backplanes with all segments on are driven with an "on backplane" waveform, and the one backplane with both on and off segments is driven with a "unique backplane" waveform. The off segments are driven with an off segment waveform and the on segments are driven with an on segment waveform with respect to the unique backplane. The sign segment and annunciator segment drives are designed for use with respect to BP1. The phasing between display waveforms is shown in Figure 4.

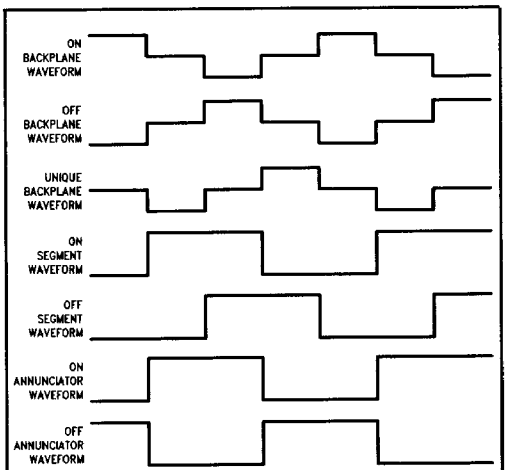


Figure 4: Display Drive Waveforms

The LCD segments appear ON when the RMS voltage between the backplane and segment drives is greater than the 90%-ON voltage of the LCD fluid, and they appear OFF when the RMS voltage is less than 10%-ON voltage of the LCD fluid. For the ½ multiplexed (duplex) waveforms used on the ICL7182 a 2.25:1 contrast ratio is achieved.

Display Set Voltage

The V_{DS} pin sets the peak-to-peak amplitude of the display drive waveforms. This voltage should be selected to give maximum contrast for a particular LCD fluid type and temperature. Good contrast ratio is obtained if V_{DS} is set within the range determined by the equation below.

$$(1.27)(Vth_{90\%}) \leq (V_{CC} - V_{DS}) \leq (2.26)(Vth_{10\%})$$

Where: $Vth_{90\%}$ = 90% ON Visual Threshold

$Vth_{10\%}$ = 10% ON Visual Threshold

For example the Hamlin Inc. type 02 LCD fluid has $Vth_{90\%}$ = 3.05V and $Vth_{10\%}$ = 2.2V, therefore the best contrast is achieved when $V_{CC} - V_{DS}$ is set between 3.9V and 5V. For most applications where V_{CC} is tied to a +5V supply the V_{DS} pin can be tied to ground.

To accommodate a large range of temperatures and fluid types the V_{DS} pin can be driven above or below V_{SS}. The voltage difference between V_{CC} and V_{DS} can vary from from 3V to 7V. For $V_{CC} - V_{DS}$ less than 3V the output impedance of the backplane drivers increase substantially. The dependence of display drive output impedance on V_{DS} and temperature is shown in the typical performance curves.

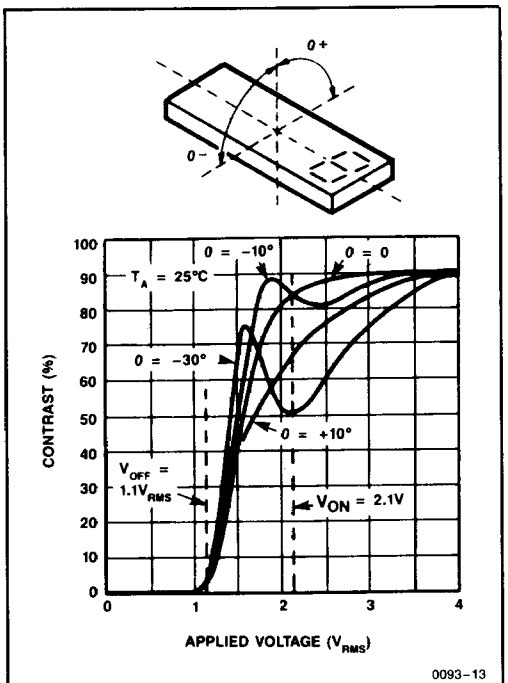


Figure 5: Contrast vs. Applied RMS Voltage

NOTE: All typical values have been characterized but are not tested.

Display Set Voltage (Continued)

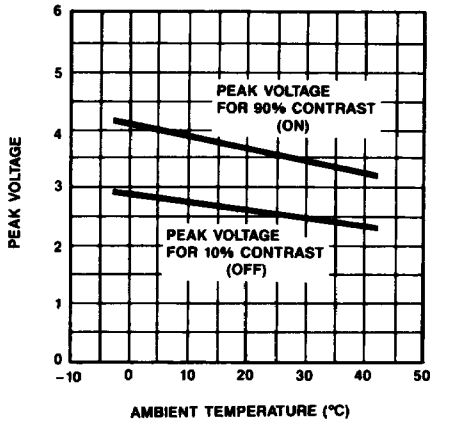


Figure 6: Temperature Dependence of LC Threshold

Temperature Effects and Temperature Compensation

The performance of the IC material is affected by temperature in two ways. The response time of the display to changes in applied RMS voltage gets longer as the display temperature drops. At very low temperatures (−20°C) some displays may take several seconds to change a new character after the new information appears at the outputs. However, for most applications above 0°C this will not be a problem with available multiplexed LCD materials, and for low-temperature applications, high-speed liquid crystal materials are available. One high temperature effect to consider deals with plastic materials used to make the polarizer. Some polarizers become soft at high temperatures and permanently lose their polarizing ability, thereby seriously degrading display contrast. Some displays also use sealing materials unsuitable for high temperature use. Thus, when specifying displays the following must be kept in mind: liquid crystal material, polarizer, and seal materials.

A more important effect of temperature is the variation of threshold voltage. For typical liquid crystal materials suitable for multiplexing, the peak voltage has a temperature coefficient of −7 to −14 mV/°C. This means that as temperature rises, the threshold voltage goes down. Assuming a fixed value for V_P, when the threshold voltage drops below $V_P/3$ OFF segments begin to be visible. Figure 6 shows the temperature dependence of peak voltage for the same liquid crystal material of Figure 5.

For applications where the display temperature does not vary widely, V_P may be set at a fixed voltage chosen to make the RMS OFF voltage, $V_P/3$, just below the threshold voltage at the highest temperature expected. This will prevent OFF segments turning ON at high temperature (this at the cost of reduced contrast for ON segments at low temperatures).

For applications where the display temperature may vary to wider extremes, the display voltage V_{DISP} (and thus V_P) may require temperature compensation to maintain sufficient contrast without OFF segments becoming visible.

Display Voltage and Temperature Compensation

These circuits allow control of the display peak voltage by bringing the bottom of the voltage divider resistor string out at pin 15. The simplest means for generating a display voltage suitable to a particular display is to connect a potentiometer from pin 15 to V_{SS} as shown in Figure 7. A potentiometer with a maximum value of 100 kΩ should give sufficient range of adjustment to suit most displays. This method for generating display voltage should be used only in applications where the temperature of the chip and display won't vary more than ±5°C (±9°F), as the resistors on the chip have a positive temperature coefficient, which will tend to increase the display peak voltage with an increase in temperature. The display voltage also depends on the power supply voltage, leading to tighter tolerances for wider temperature ranges.

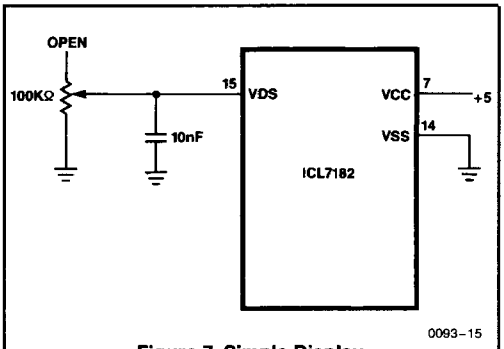


Figure 7: Simple Display Voltage Adjustment

NOTE: All typical values have been characterized but are not tested.

Display Set Voltage (Continued)

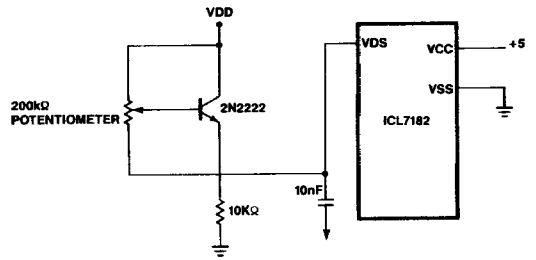


Figure 8A: Temperature compensation and contrast adjustment for LCD fluid types which have visual threshold tempcos of ~ −10 mV/°C and operate with 3V to 4.0V.

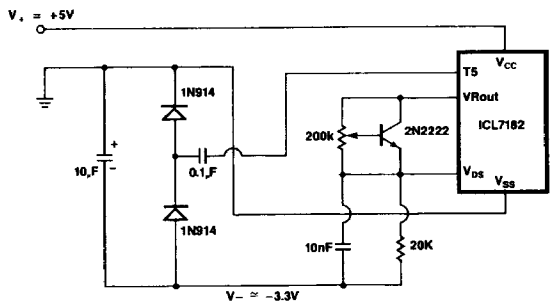


Figure 8B: Generating a negative supply from +5V to drive the display voltage pin below ground. This allows use of wide temperature LCD fluids which require peak-peak display drives of 3.5V to 7V. For LCD fluids which have threshold tempcos of ~ −8 mV/°C the collector of Q1 and 200 kΩ resistor should be tied to V_{ROUT}, for larger threshold tempcos of ~ −16 mV/°C this point should be tied to V_{CC}.

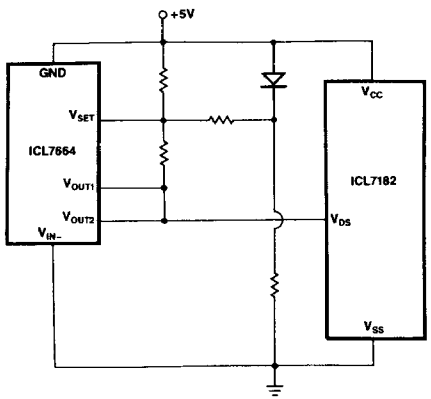


Figure 9: Conceptually a flexible LCD contrast and temperature compensation using an ICL7664 can be designed in this manner. This technique allows adjusting the display voltage and temperature compensation independently.

NOTE: All typical values have been characterized but are not tested.

Display Layout

Custom displays developed for the ICL7182 need to be arranged such that the 8 segment lines serpentine across 13 backplanes. The annunciators and first eight data segments share a common backplane (BP1). An example layout is shown in Figure 10. This 1.3" by 4.5" display is available from Hamlin Inc. (part # 4464-363-921) for prototyping and evaluation.

Custom Display

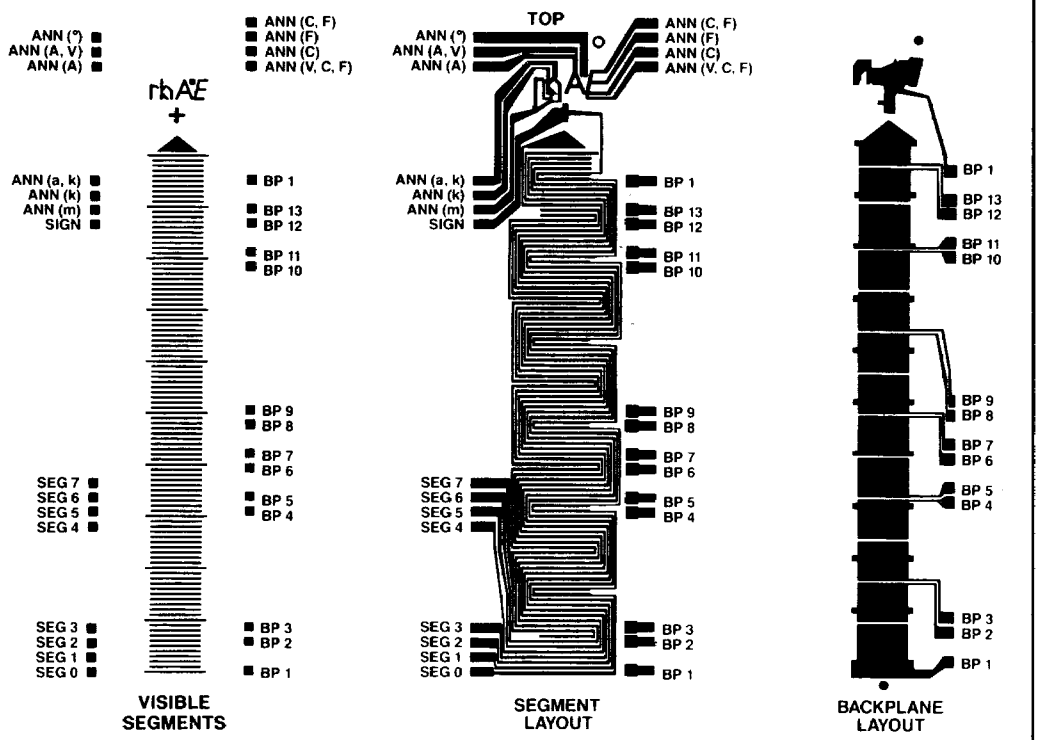


Figure 10: Custom LCD Layout

NOTE: All typical values have been characterized but are not tested.

APPLICATIONS

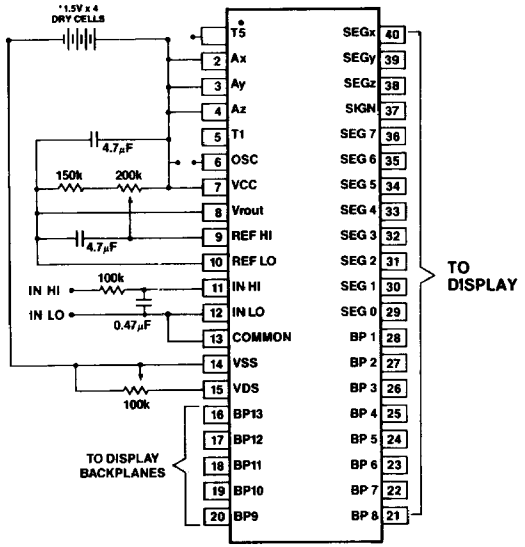


Figure 11: 7182 using the internal reference. Values shown are for 1.00V full-scale, 1% adjustment sensitivity, 24 readings per second, 6V floating supply (four stacked 1.5V dry cells).*

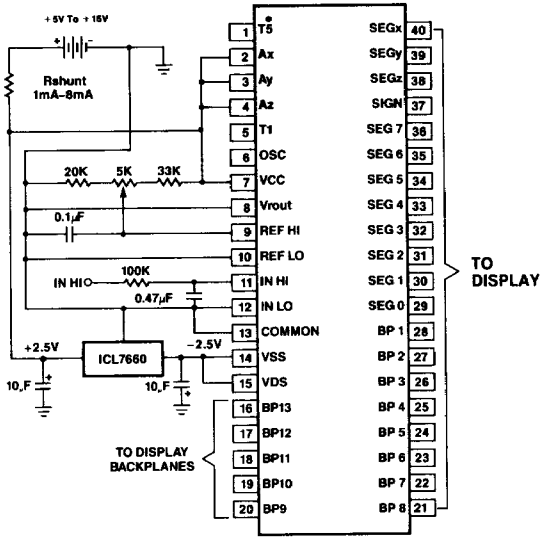


Figure 12: 7182 using the internal reference and ICL7660 as a supply regulator. This allows sensing ground reference bipolar inputs with a single +5V supply. Values shown for 1.00V full-scale, 0.25% adjustment sensitivity.

NOTE: All typical values have been characterized but are not tested.

APPLICATIONS (Continued)

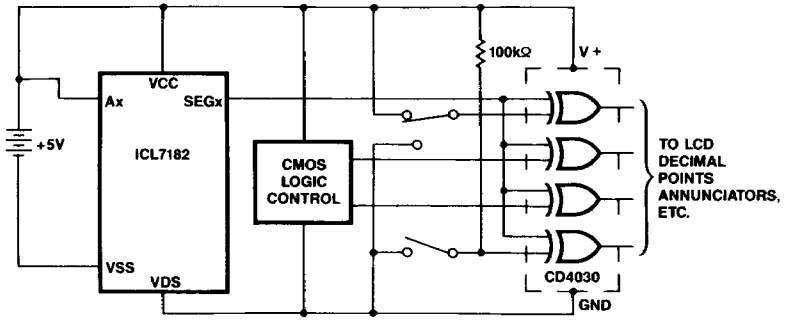


Figure 13: Using Exclusive 'OR' Gate for additional annunciator drivers.

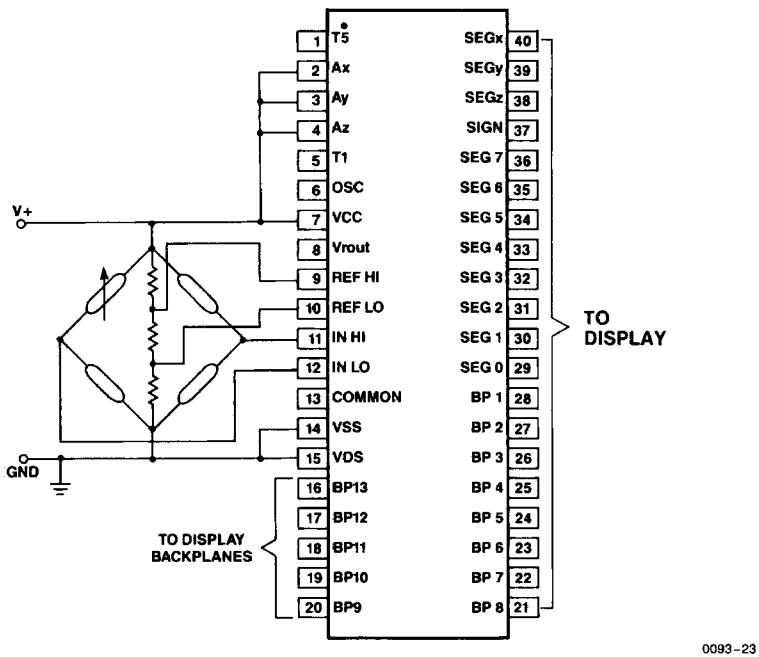
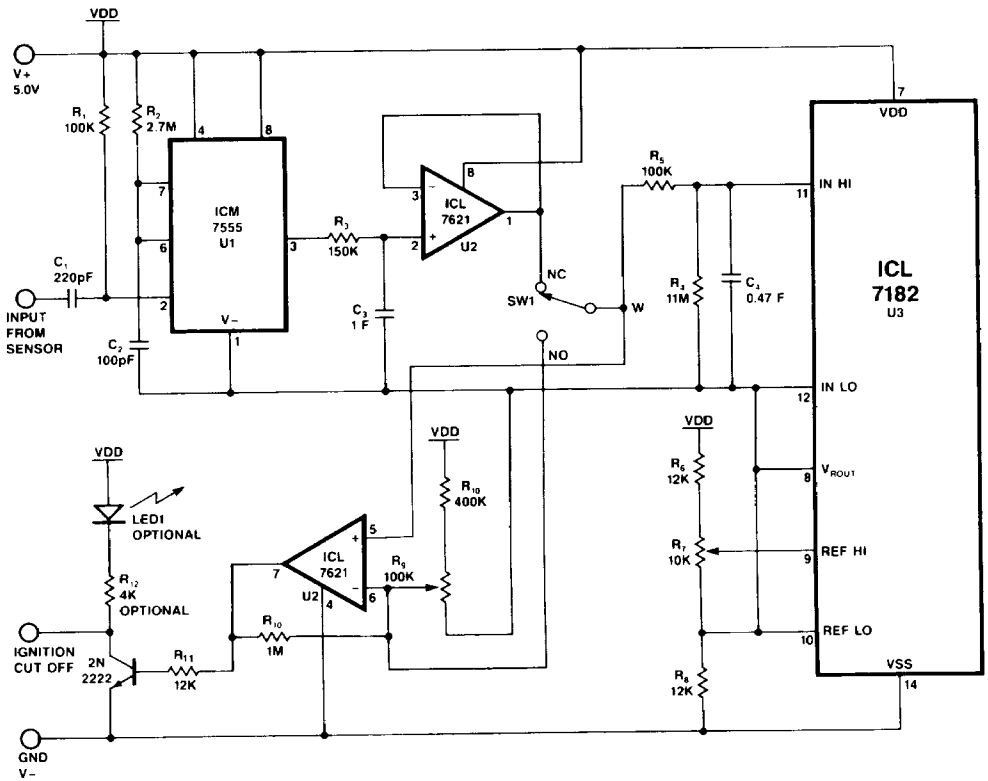


Figure 14: 7182 measuring ratiometric values of Quad Load Cell. The resistor values within bridge are determined by the desired sensitivity.

NOTE: All typical values have been characterized but are not tested.

APPLICATIONS (Continued)



$$\frac{V_O}{V_{IN}} = \frac{1/RC}{S + 1/R_3C_3}$$

$$fc = \frac{1}{2_\pi R_3C_3}$$

SW1 Momentary
Switch SPST

V_{IN} = 264 mV @ 5000 RPM
4 Stroke V8

RPM	Hz	Period
600	10	100 ms
1000	16.7	60 ms
5000	83	12 ms
10,000	166.7	6 ms

No. of Cylinders	Events Per Cycle	Strokes Per Cycle
1	0.5	4
4	2	4
6	3	4
8	4	4

Figure 15: Tachometer with Set Point

NOTE: All typical values have been characterized but are not tested.

APPLICATIONS (Continued)

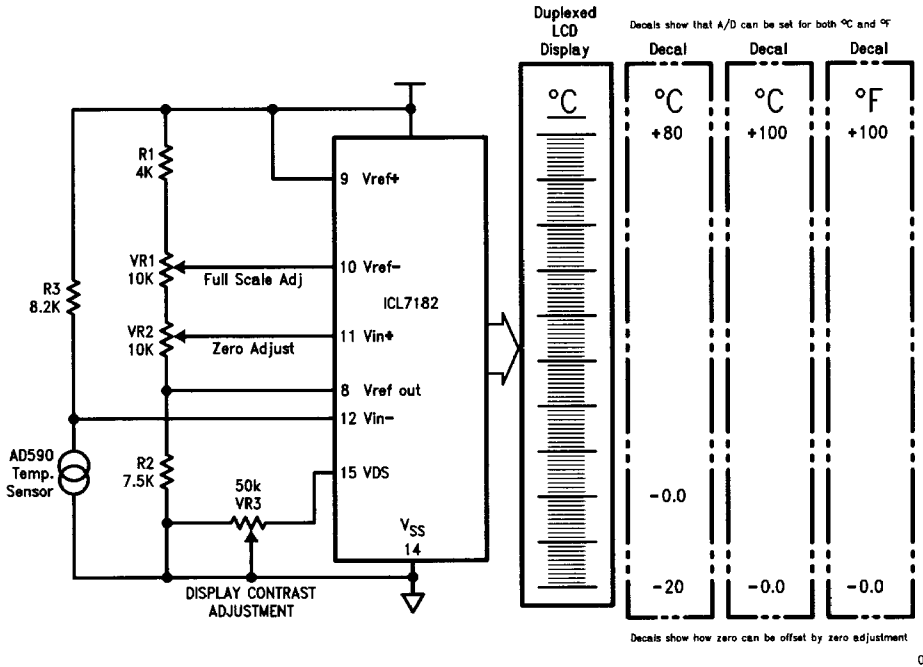


Figure 16: Basic digital thermometer, Celsius and Fahrenheit scales. This V_{DS} pin can be connected as shown in Figure 11.

NOTE: All typical values have been characterized but are not tested.