BURR - BROWN®

DSD1700

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Direct Stream Digital™ (DSD™) SoundPLUS™ Audio DIGITAL-TO-ANALOG CONVERTER

FEATURES

- **DIRECT TRANSFER OF DSD DATA STREAM TO ANALOG OUTPUT SIGNAL**
- **DUAL DIFFERENTIAL ANALOG FIR FILTER**
- **DIRECT, CMOS LOGIC INTERFACE TO DSD™ DECODER IC**
  - **Data Clock: 2.8224 MHz (64 • 44.1kHz)**
  - **System Clock: 11.2896 MHz (256 • 44.1kHz)**
- **EXCELLENT DYNAMIC PERFORMANCE**
  - **THD+N: 0.001% (typ)**
  - **Dynamic Range: 110dB (typ)**
  - **SNR: 110dB (typ)**
  - **Frequency Response (–3dB): 100kHz**
- **SINGLE +5V SUPPLY OPERATION**
- **SMALL 28-LEAD SSOP PACKAGE**

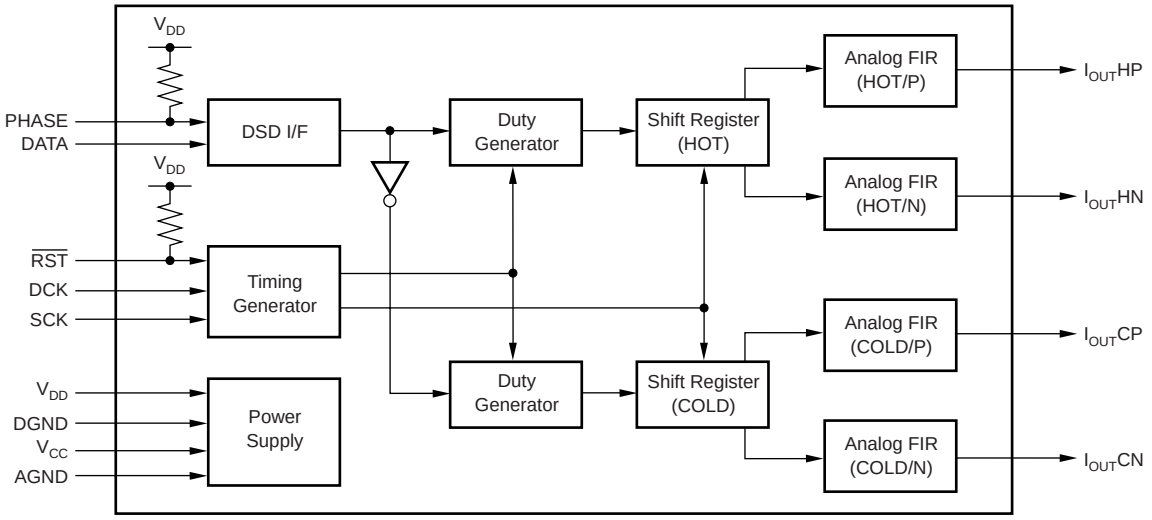
APPLICATIONS

- **SUPER AUDIO CD (SACD™) PLAYERS**
- **PROFESSIONAL DSD PROCESSORS**
- **PROFESSIONAL DSD CONSOLES**

DESCRIPTION

The DSD1700 is a unique digital-to-analog converter designed for DSD audio applications. The DSD1700 consists of a single-channel, 8-tap analog FIR filter constructed using a double differential circuit architecture, ensuring excellent dynamic performance and high power- supply noise rejection. The DSD1700 also includes the necessary logic required to interface directly to a DSD decoder IC.

The overall features and performance of the DSD1700 make it an ideal choice for high-performance Super Audio CD players and DSD studio applications.



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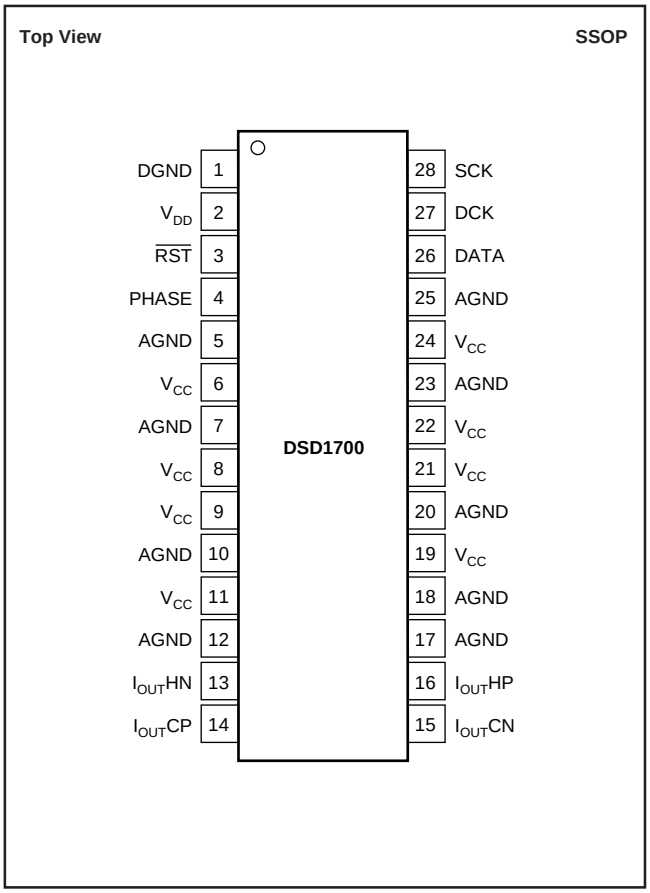
SPECIFICATIONS

All specifications T_A = +25°C, V_{DD} = V_{CC} = 5.0V, f_S = 44.1kHz, data clock = 64f_S, system clock = 256f_S, unless otherwise specified. (Although the sampling frequency of Direct Stream Digital is 2.8224MHz, for convenience, in this specification sheet, it is described that the sampling frequency (f_S) is 44.1kHz and the 2.8224MHz clock is 64f_S).

PARAMETER		CONDITIONS	DSD1700E MIN	DSD1700E TYP	DSD1700E MAX	UNITS
INPUT CLOCK						
Data Clock Frequency (DCK)		64f_S		2.8224		MHz
System Clock Frequency (SCK)		256f_S		11.2896		MHz
SCK AC REQUIREMENT(1)						
Input Clock Duty Cycle				50		%
DIGITAL INPUT						
High Level Input Voltage	V_{IH}		0.7V_{DD}			V
Low Level Input Voltage	V_{IL}				0.3V_{DD}	V
High Level Input Current	I_{IH}				±10	µA
Low Level Input Current	I_{IL}(2)				±10	µA
	I_{IL}(3)				–120	µA
ANALOG OUTPUT(5)						
Full-Scale Voltage				4.1V_{CC}		Vp-p
Gain Error				±4	±10	% of FSR
Offset Error				±0.1	±1	% of FSR
Output Impedance(4)				2		kΩ
DYNAMIC PERFORMANCE(5)						
THD+N, V_{OUT} = 0dB		with 30kHz GIC Filter		0.001		%
Dynamic Range		with 30kHz GIC Filter		110		dB
Signal-to-Noise Ratio		with 30kHz GIC Filter		110		dB
Frequency Response, –3dB				100		kHz
POWER SUPPLY REQUIREMENTS						
Voltage Range		V_{CC}, V_{DD}	4.5	5	5.5	VDC
Supply Current	I_{CC}+I_{DD}	V_{CC} = V_{DD} = 5.0V		5.5	8.0	mA
Power Dissipation		V_{CC} = V_{DD} = 5.0V		27.5	40	mW
TEMPERATURE RANGE						
Operating			–25		+85	°C
Storage			–55		+125	°C
Thermal Resistance	θ_{JA}	28-Pin SSOP		100		°C/W

NOTES: (1) See description of system clock in the Functional Description section of this data sheet. (2) Pins 26, 27, 28: DATA. DCK. SCK. (3) Pins 3, 4: $\overline{RST}$, PHASE (with internal pull-up). (4) Pins 13, 14, 15, 16: I_{OUT}HN, I_{OUT}CP, I_{OUT}CN, I_{OUT}HP. (5) Measure DSD signal modulated f_{SIG} = 1kHz with 50% scaling factor through standard differential to single-ended converter (see Figure 10) using Audio Precision System II in rms mode with 20kHz LPF and 400Hz HPF.

PIN CONFIGURATION



PIN ASSIGNMENTS

PIN	NAME	I/O	DESCRIPTION
1	DGND	—	Digital Ground
2	V_{DD}	—	Digital Power Supply: +5V
3	$\overline{RST}$	IN	Reset Control Input, Active LOW(1)
4	PHASE	IN	Select data phase (LOW = Normal; HIGH = Invert)
5	AGND	—	Analog Ground
6	V_{CC}	—	Analog Power Supply: +5V
7	AGND	—	Analog Ground
8	V_{CC}	—	Analog Power Supply: +5V
9	V_{CC}	—	Analog Power Supply: +5V
10	AGND	—	Analog Ground
11	V_{CC}	—	Analog Power Supply: +5V
12	AGND	—	Analog Ground
13	I_{OUT}HN	OUT	Analog Output from DAC (Hot Negative)
14	I_{OUT}CP	OUT	Analog Output from DAC (Cold Positive)
15	I_{OUT}CN	OUT	Analog Output from DAC (Cold Negative)
16	I_{OUT}HP	OUT	Analog Output from DAC (Hot Positive)
17	AGND	—	Analog Ground
18	AGND	—	Analog Ground
19	V_{CC}	—	Analog Power Supply: +5V
20	AGND	—	Analog Ground
21	V_{CC}	—	Analog Power Supply: +5V
22	V_{CC}	—	Analog Power Supply: +5V
23	AGND	—	Analog Ground
24	V_{CC}	—	Analog Power Supply: +5V
25	AGND	—	Analog Ground
26	DATA	IN	Direct Stream Digital Data Input
27	DCK	IN	Data Clock Input
28	SCK	IN	System Clock Input

NOTE: (1) With internal pull-up resistor

ABSOLUTE MAXIMUM RATINGS(1)

Supply Voltage(2)	+6.5V
Supply Voltage Differences(3)	±0.1V
Ground Voltage Differences(4)	±0.1V
Digital Input Voltage	–0.3V to V_{DD} +0.3V
Input Current (any pins except supplies)	±10mA
Operating Temperature	–25°C to +85°C
Storage Temperature	–55°C to +125°C
Junction Temperature	+150°C
Lead Temperature (soldering, 5s)	+260°C
Package Temperature (IR reflow, peak, 10s)	+235°C

NOTE: (1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. (2) V_{CC}, V_{DD}. (3) Among V_{CC}, V_{DD}. (4) Among AGND, DGND.

ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

PACKAGE/ORDERING INFORMATION

PRODUCT	PACKAGE	PACKAGE DRAWING NUMBER	SPECIFIED TEMPERATURE RANGE	PACKAGE MARKING	ORDERING NUMBER(1)	TRANSPORT MEDIA
DSD1700E	28-Lead SSOP	324	0°C to +70°C	DSD1700E	DSD1700E	Rails
"	"	"	"	"	DSD1700E/2K	Tape and Reel

NOTE: (1) Models with a slash (/) are available only in Tape and Reel in the quantities indicated (e.g., /2K indicates 2000 devices per reel). Ordering 2000 pieces of “DSD1700E/2K” will get a single 2000-piece Tape and Reel.

GENERAL INFORMATION

The DSD1700 is designed solely for use in DSD and SACD applications. It is not compatible with standard CD audio transports, or DVD/MPEG-2 decoders. Burr-Brown manufacturers a wide array of products for these applications. Please refer to our audio brochure and product data sheets, available from our web site (www.burr-brown.com) and local sales offices.

FUNCTIONAL DESCRIPTION

The concept of Direct Stream Digital (DSD) conversion is simple. An analog audio input is digitized by a 1-bit, 64x oversampled delta-sigma modulator. The 1-bit data stream is then stored and may be transferred to a SACD disc at a later time. For playback, the 1-bit, 64x oversampled data is then presented to the DSD1700 directly by a DSD decoder IC. The DSD1700 then low-pass filters the oversampled data to reconstruct the original analog audio waveform. The recording and playback functions are illustrated in Figures 1 and 2 respectively.

To perform the digital-to-analog conversion, the DSD1700 includes both the decoder interface logic and an analog FIR filter. The following paragraphs provide a summary of these functions.

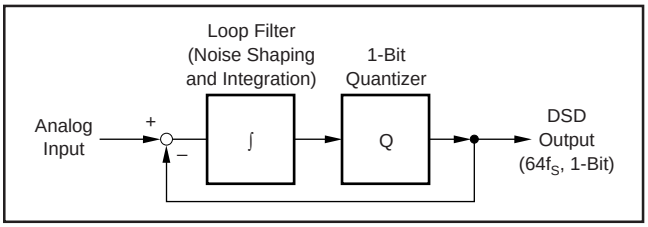


FIGURE 1. DSD Recording.

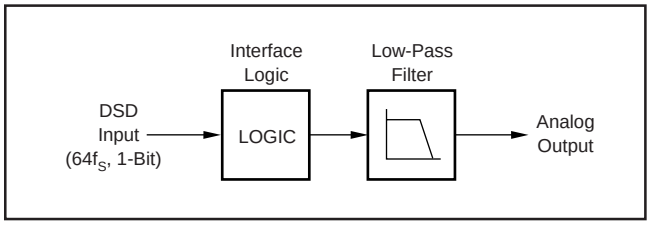
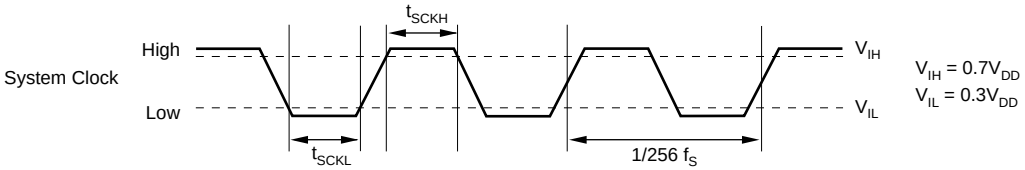


FIGURE 2. DSD Playback.



SYMBOL	DESCRIPTION	MIN	TYP	MAX	UNITS
t_{SCKH}	System Clock Pulse Width High	10			ns
t_{SCKL}	System Clock Pulse Width Low	10			ns

FIGURE 3. System Clock Timing.

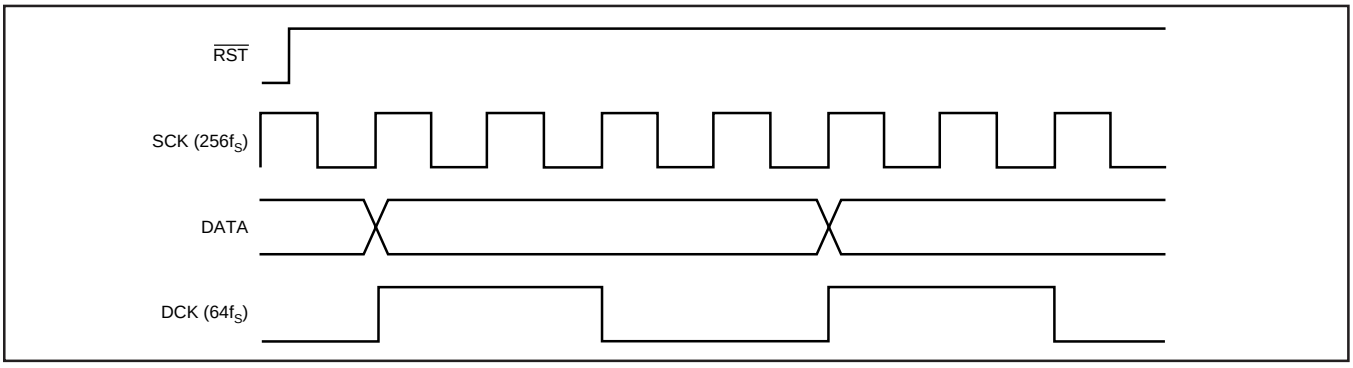


FIGURE 4. Input Signal Timing.

DECODER INTERFACE

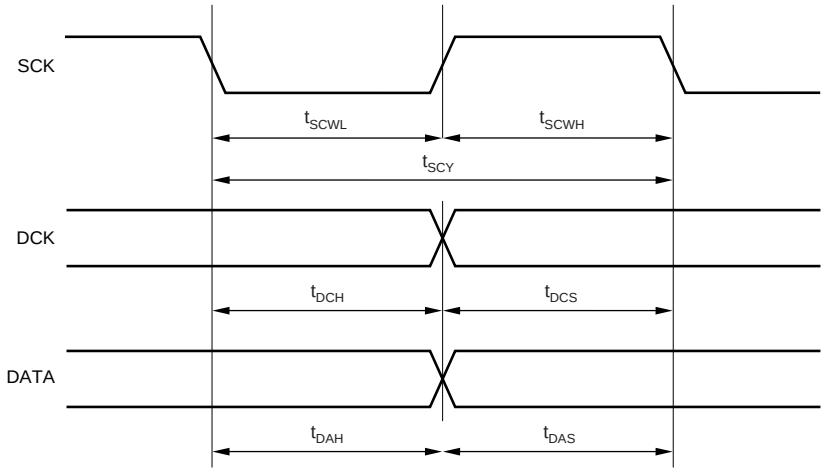
The decoder interface consists of several CMOS logic inputs. The system clock input, SCK (pin 28), operates at 11.2896MHz (256 • 44.1kHz). The data bit clock, DCK (pin 27), operates at 2.8244 MHz (64 • 44.1kHz) and is the 64x oversampled data clock. The 1-bit, 64x oversampled data stream is input at DATA (pin 26). DATA and DCK are synchronized to the SCK falling edge.

The DSD1700 generates HOT and COLD data internally for use with the double differential analog FIR filter. The PHASE input (pin 4) is used to determine the polarity of the HOT and COLD data (normal or inverted). The PHASE input is synchronized to the rising edge of SCK.

The $\overline{RST}$ input (pin 3) is used for system reset purposes. $\overline{RST}$ should be High for normal operation, and Low for reset operation. When $\overline{RST}$ is held Low, the current outputs of the analog FIR filter are set to the bipolar zero (BPZ) level. The $\overline{RST}$ signal is synchronized to the rising edge of SCK.

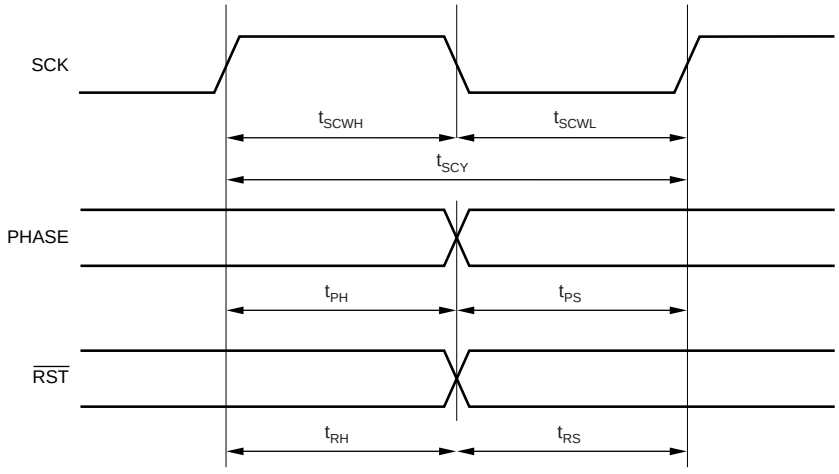
TIMING

Figures 3 though 6 show the timing diagrams for the DSD1700 interface signals. Figure 3 shows the system clock (SCK) timing requirements. Figure 4 shows the general timing for the data input. Figures 5 and 6 show the detailed timing for the DSD data and control data inputs.



SYMBOL	DESCRIPTION	MIN	TYP	MAX	UNITS
t_{SCWH}	SCK Pulse Width High	10			ns
t_{SCWL}	SCK Pulse Width Low	10			ns
t_{SCY}	SCK Pulse Cycle Time		$1/(256f_S)$		sec
t_{DCS}	DCK Setup Time	15			ns
t_{DCH}	DCK Hold Time	5			ns
t_{DAS}	DATA Setup Time	15			ns
t_{DAH}	DATA Hold Time	5			ns

FIGURE 5. DSD Data Input Timing.



SYMBOL	DESCRIPTION	MIN	TYP	MAX	UNITS
t_{SCWH}	SCK Pulse Width High	10			ns
t_{SCWL}	SCK Pulse Width Low	10			ns
t_{SCY}	SCK Pulse Cycle Time		$1/(256f_S)$		sec
t_{PS}	PHASE Setup Time	15			ns
t_{PH}	PHASE Hold Time	5			ns
t_{RS}	$\overline{RST}$ Setup Time	15			ns
t_{RH}	$\overline{RST}$ Hold Time	5			ns

FIGURE 6. Control Data Input Timing.

ANALOG FIR FILTER

The low-pass filter function for the DSD1700 is constructed by using four 8-tap, analog FIR filters with current outputs. The four filters include one each for HOT and COLD positive, and one each for HOT and COLD negative. This is referred to as a double differential architecture. These filters use resistors to set the filter coefficients, as shown in Figure 7. Prior to the analog FIR filters, the duty cycle of the DSD input signal is set to 75% by the DSD1700's duty generators.

Plots of the analog FIR filter response is shown in Figure 8. The stop-band attenuation of the filters dictates that additional low-pass filtering is required at the output of the external current-to-voltage converter circuit (see Figure 10).

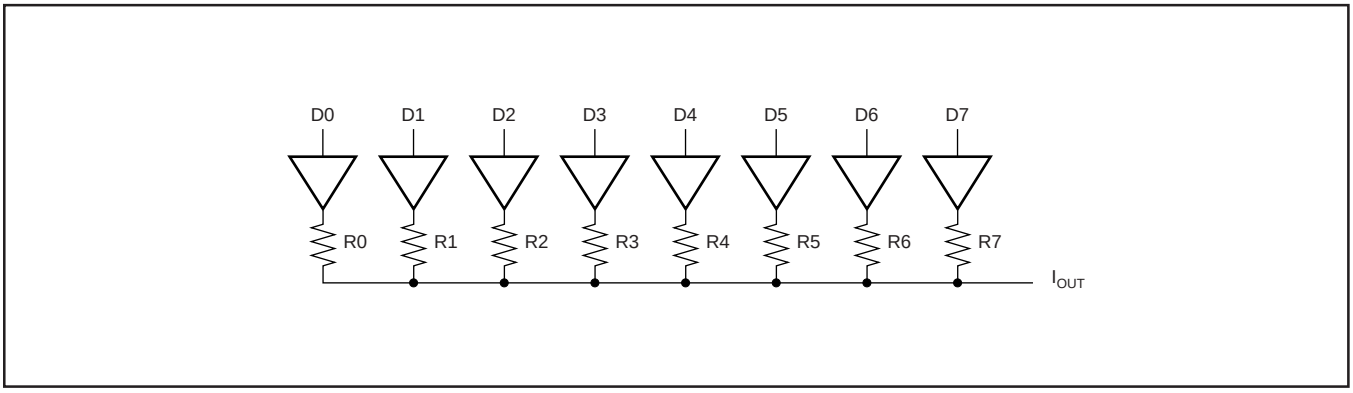


FIGURE 7. Analog FIR Filter Structure.

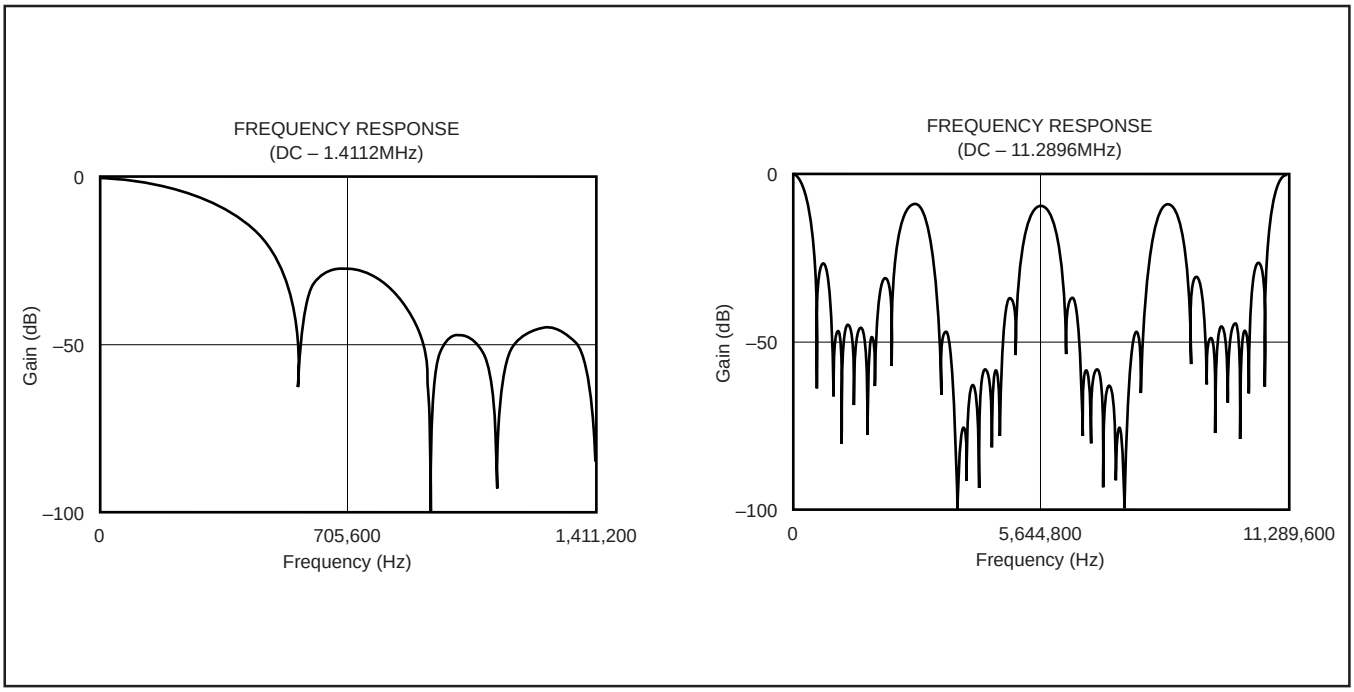


FIGURE 8. Analog FIR Filter Frequency Response.

APPLICATIONS INFORMATION

TYPICAL CONNECTIONS

Figure 9 shows the basic connection diagram for the DSD1700. A significant number of power supply bypass capacitors are required, and Burr-Brown recommends the indicated values for optimal performance.

CURRENT-TO-VOLTAGE (I/V) CONVERTER CIRCUIT

The DSD1700 is a current output device, and requires an I/V conversion circuit to transform the double-differential outputs into a usable voltage output. The circuit in Figure 10 is recommended for this purpose. Op amps are OPA134 or equivalent.

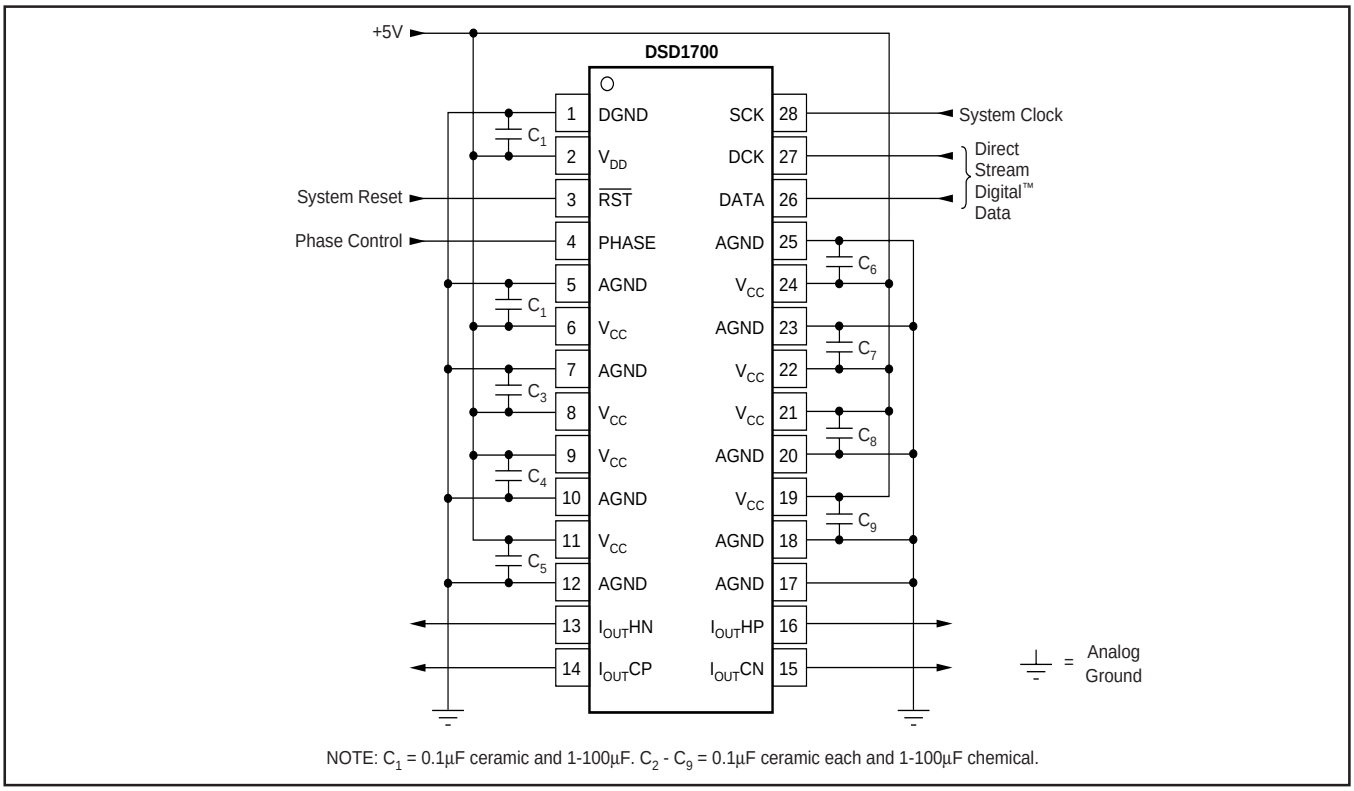


FIGURE 9. Basic Connection Diagram.

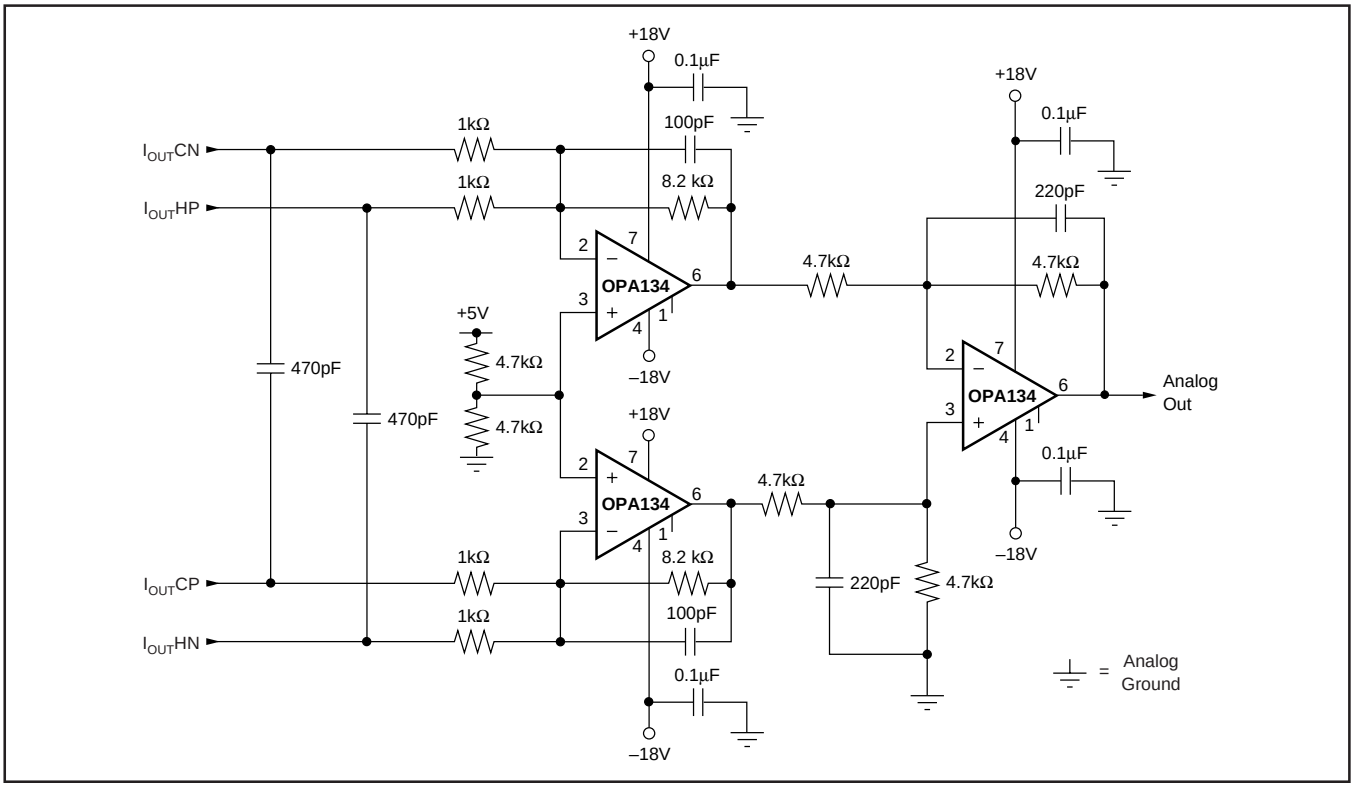


FIGURE 10. Recommended I/V Conversion Circuit.

PRINTED CIRCUIT BOARD LAYOUT

A typical PCB floor plan for the DSD1700 is shown in Figure 11. A ground plane is recommended, with the analog and digital sections being isolated from one another using a split in the plane. The DSD1700 should be oriented with the digital I/O pins facing the ground plane split/cut, allowing for direct connection to the DSD decoder and control signals originating from the digital section of the board.

Separate power supplies are recommended for the digital and analog sections of the board. This prevents the switching noise present on the digital supply from contaminating the analog power supply and degrading the dynamic performance of the DSD1700.

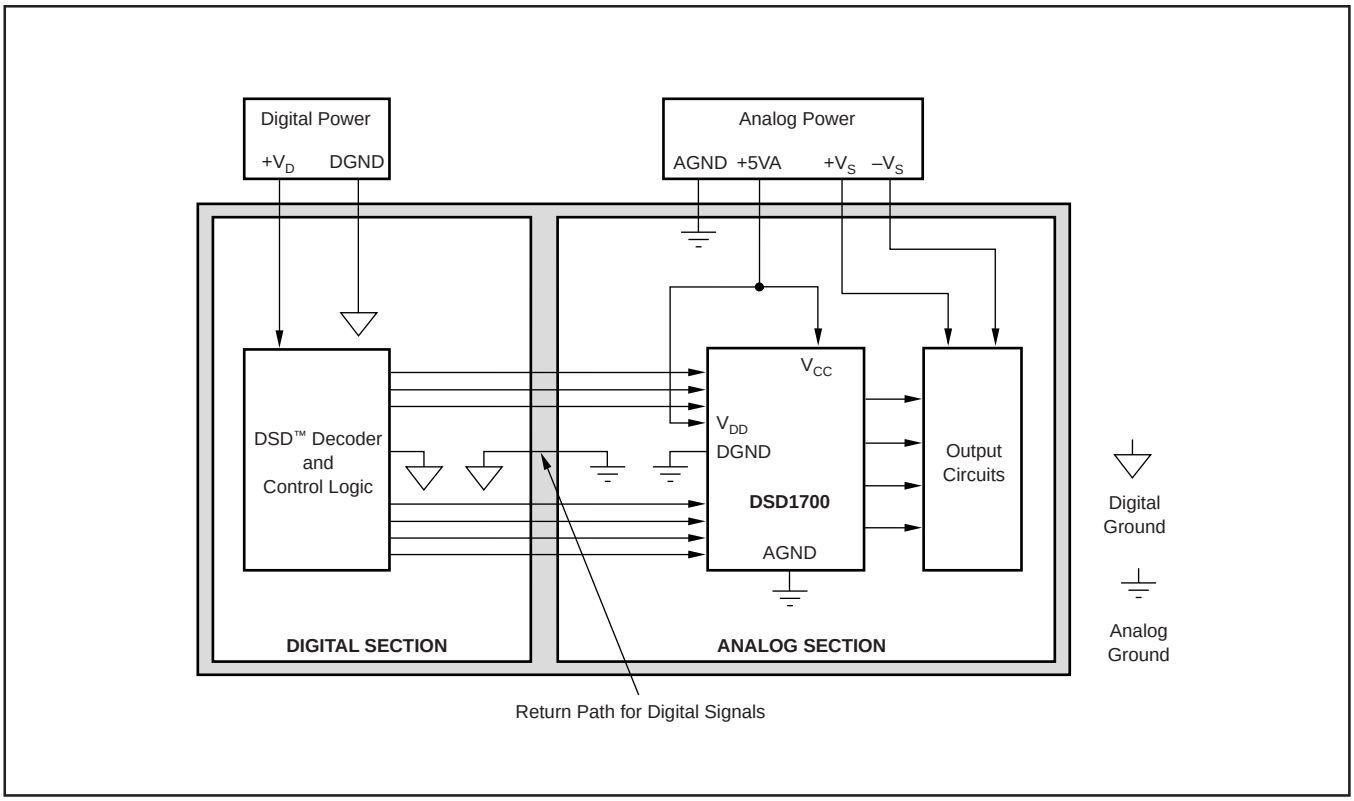


FIGURE 11. Recommended PCB Layout Technique.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
DSD1700E/2K	ACTIVE	SSOP	DB	28	2000	TBD	Call TI	Call TI

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS) or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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