

Z86C72/C92/L72/L92

IR/LOW-VOLTAGE MICROCONTROLLER

FEATURES

Part	ROM (KB)	RAM* (Bytes)	I/O	Voltage Range
Z86C72	16	748	31	4.5V to 5.5V
Z86C92	0	748	31	4.5V to 5.5V
Z86L72	16	748	31	2.0V to 3.9V
Z86L92	0	748	31	2.0V to 3.9V

Note: *General-Purpose

- Expanded Register File Control Registers
- Low Power Consumption - 40 mW (typical)
- Three Standby Modes:
 - STOP
 - HALT
 - Low Voltage
- Automatic External ROM Access Beyond 16K (Z86LX2/C72 Version)
- Special Architecture to Automate Both Generation and Reception of Complex Pulses or Signals:
 - One Programmable 8-Bit Counter/Timer with Two Capture Register
- One Programmable 16-Bit Counter/Timer with One Capture Register
- Programmable Input Glitch Filter for Pulse Reception
- Five Priority Interrupts
 - Three External
 - Two Assigned to Counter/Timers
- Low Voltage Detection and Standby Mode
- Programmable Watch-Dog/Power-On Reset Circuits
- Two Independent Comparators with Programmable Interrupt Polarity
- On-Chip Oscillator that Accepts a Crystal, Ceramic Resonator, LC, RC (mask option), or External Clock Drive
- Mask Selectable 200 KOhms Pull-Ups on Ports 0, 2, 3
 - Port 2 Pull-Ups are Bit Selectable
 - Pull-Ups Automatically Disabled as Outputs
- Maskable Mouse/Trackball Interface on P00 Through P03 is available on the L72 version.
- 32 kHz Oscillator Mask Option

GENERAL DESCRIPTION

The Z86LX2/CX2 family of IR (Infrared) are ROM/ROM-less-based members of the Z8[®] MCU single-chip microcontroller family with 768 bytes of internal RAM. The differentiating factor between these devices is the availability of RAM, ROM and package options. The use of external memory enables these Z8 microcontrollers to be used where code flexibility is required. Offering the 5V versions (Z86CXX) and gives optimum performance in both the low and high voltage ranges. Zilog's CMOS microcontrollers

offer fast execution, efficient use of memory, sophisticated interrupts, input/output bit manipulation capabilities, automated pulse generation/reception, and internal key-scan pull-up resistors. The Z86LX2/CX2 product line offers easy hardware/software system expansion with cost-effective and low power consumption.

The Z86LX2/CX2 architecture is based on Zilog's 8-bit microcontroller core with an Expanded Register File to allow access to register mapped peripherals, I/O circuits, and

GENERAL DESCRIPTION (Continued)

powerful counter/timer circuitry. The Z86C72/C92/L72/L92 offers a flexible I/O scheme, an efficient register and address space structure, and a number of ancillary features that are useful in many consumer, automotive, computer peripheral, and battery operated hand-held applications.

Many applications demand powerful I/O capabilities. The Z86LX2/CX2 family fulfills this with three package options in which the L72 version provides 31 pins of dedicated input and output. These lines are grouped into four ports. Each port consists of eight lines (Port 3 has seven lines) and is configurable under software control to provide timing, status signals, parallel I/O with or without handshake, and an address/data bus for interfacing external memory.

There are five basic address spaces available to support a wide range of configurations: Program Memory, Register

File, Expanded Register File, Extended Data RAM and External Memory. The register file is composed of 256 bytes of RAM. It includes four I/O port registers, 16 control and status registers and the rest are General-Purpose registers. The Extended Data RAM adds 512 bytes of usable general-purpose registers. The Expanded Register File consists of two additional register groups (F and D).

To unburden the program from coping with such real-time problems as generating complex waveforms or receiving and demodulating complex waveform/pulses, the Z86LX2/CX2 family offers a new intelligent counter/timer architecture with 8-bit and 16-bit counter/timers (Figure 1). Also included are a large number of user-selectable modes, and two on-board comparators to process analog signals with separate reference voltages (Figure 2).

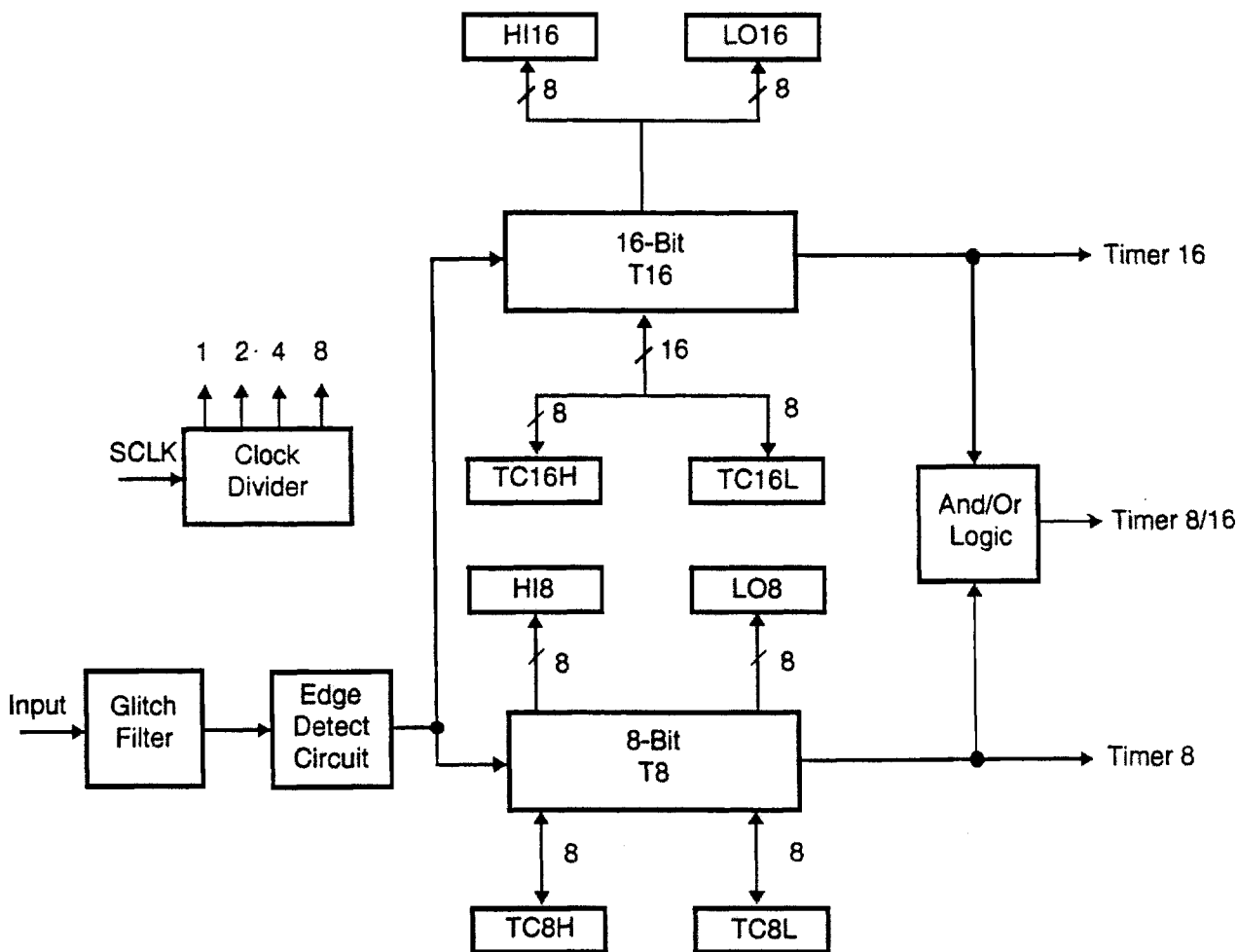


Figure 1. Counter/Timer Block Diagram

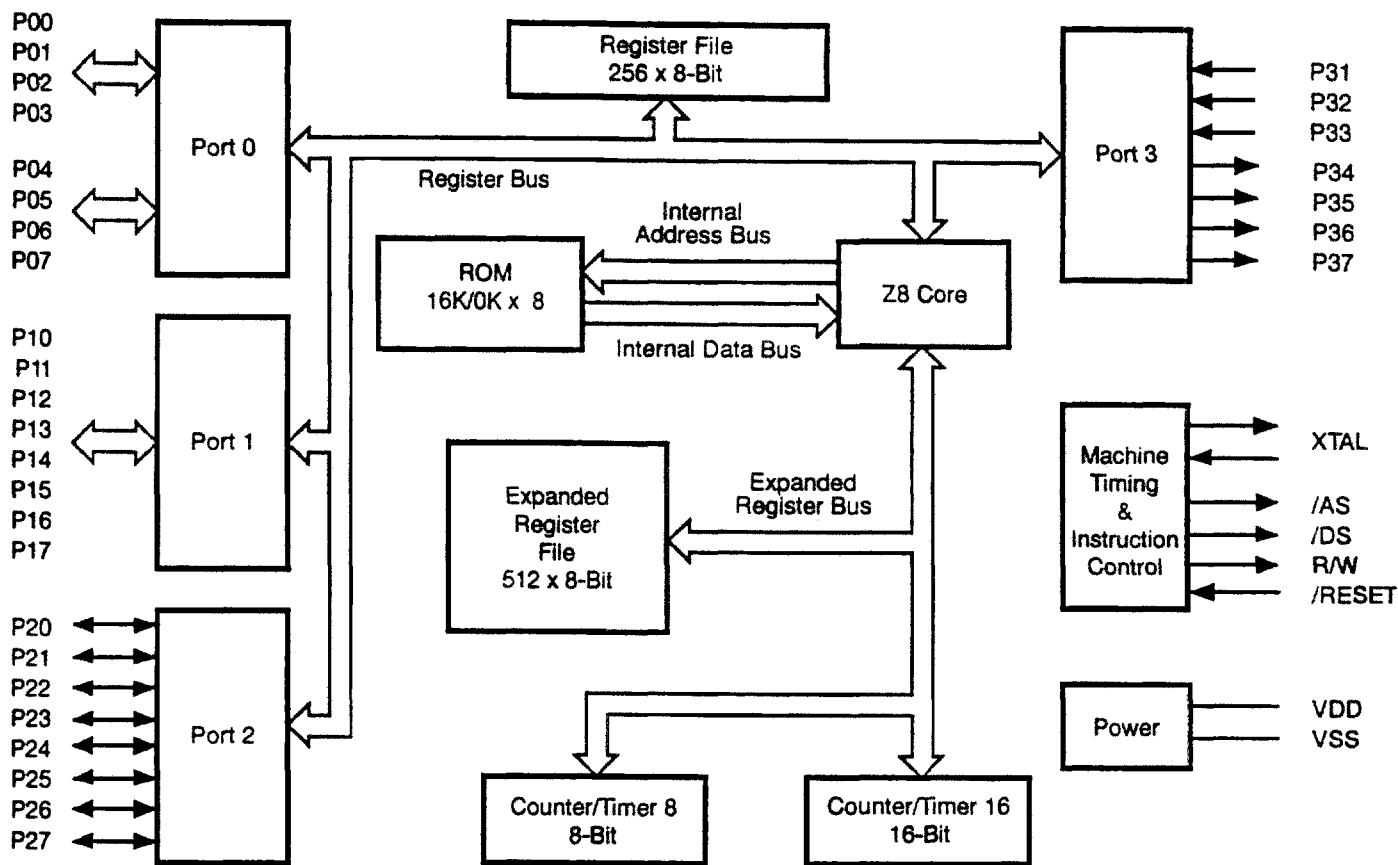


Figure 2. Functional Block Diagram

Note: All Signals with a preceding front slash, "/", are active Low, for example, B/ \overline{W} (WORD is active Low); /B/ \overline{W} (BYTE is active Low, only).

Power connections follow conventional descriptions below:

Connection	Circuit	Device
Power	V _{CC}	V _{DD}
Ground	GND	V _{SS}

PIN DESCRIPTION

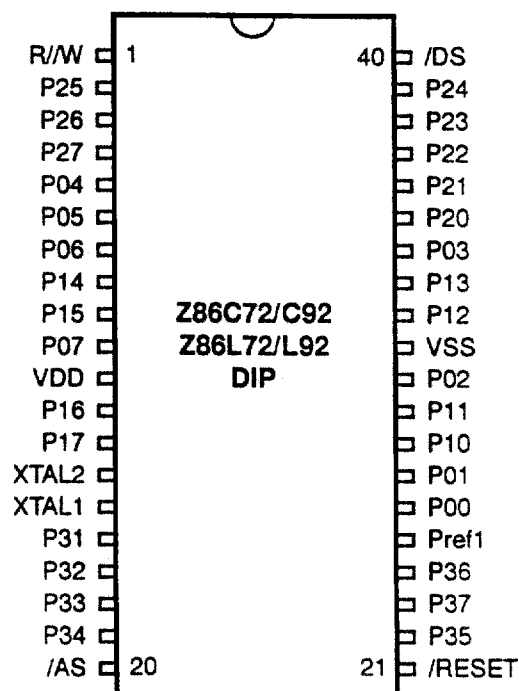


Figure 3. 40-Pin DIP Pin Assignments

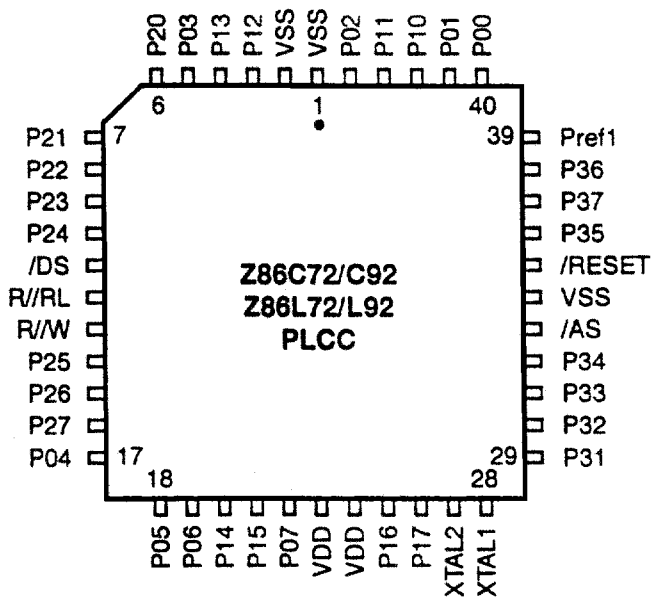


Figure 4. 44-Pin PLCC Pin Assignments

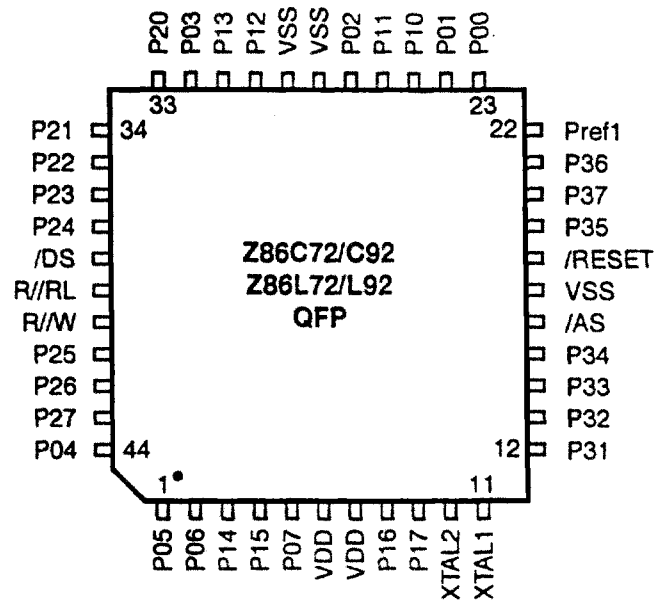


Figure 5. 44-Pin QFP Pin Assignments

PIN DESCRIPTION (Continued)

Table 1. Pin Identification

40-Pin DIP #	44-Pin PLCC	44-Pin QFP#	Symbol	Direction	Description
26	40	23	P00	Input/Output	Port 0 is Nibble Programmable Port 0 can be configured as A15-A8 external program ROM/DATA Address Bus. Port 0 can be configured as a mouse/trackball input.
27	41	24	P01	Input/Output	
30	44	27	P02	Input/Output	
34	5	32	P03	Input/Output	
5	17	44	P04	Input/Output	
6	18	1	P05	Input/Output	
7	19	2	P06	Input/Output	
10	22	5	P07	Input/Output	
28	42	25	P10	Input/Output	Port 1 is byte programmable Port 1 can be configured as multiplexed A7-A0/D7-D0 external program ROM Address/Data Bus.
29	43	26	P11	Input/Output	
32	3	30	P12	Input/Output	
33	4	31	P13	Input/Output	
8	20	3	P14	Input/Output	
9	21	4	P15	Input/Output	
12	25	8	P16	Input/Output	
13	26	9	P17	Input/Output	
35	6	33	P20	Input/Output	Port 2 pins are individually configurable as input or output.
36	7	34	P21	Input/Output	
37	8	35	P22	Input/Output	
38	9	36	P23	Input/Output	
39	10	37	P24	Input/Output	
2	14	41	P25	Input/Output	
3	15	42	P26	Input/Output	
4	16	43	P27	Input/Output	
16	29	12	P31	Input	IRQ2/Modulator Input
17	30	13	P32	Input	IRQ0
18	31	14	P33	Input	IRQ1
19	32	15	P34	Output	T8 output
22	36	19	P35	Output	T16 output
24	38	21	P36	Output	T8/T16 output
23	37	20	P37	Output	
20	33	16	/AS	Output	Address Strobe
40	11	38	/DS	Output	Data Strobe
1	13	40	R/W	Output	Read/Write
21	35	18	/RESET	Input	Reset
15	28	11	XTAL1	Input	Crystal, Oscillator Clock
14	27	10	XTAL2	Output	Crystal, Oscillator Clock
11	23,24	6,7	V _{DD}		Power Supply
31	1,2,34	17,28,29	V _{SS}		Ground
25	39	22	Pref1	Input	Comparator 1 Reference
	12	39	R//RL	Input	ROM/ROMless

ABSOLUTE MAXIMUM RATINGS

Symbol	Description	Min	Max	Units
V_{CC}	Supply Voltage (*)	-0.3	+7.0	V
T_{STG}	Storage Temp.	-65°	+150°	C
T_A	Oper. Ambient Temp.		†	C

Notes:

* Voltage on all pins with respect to GND.

† See Ordering Information.

Stresses greater than those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; operation of the device at any condition above those indicated in the operational sections of these specifications is not implied. Exposure to absolute maximum rating conditions for an extended period may affect device reliability.

STANDARD TEST CONDITIONS

The characteristics listed below apply for standard test conditions as noted. All voltages are referenced to GND. Positive current flows into the referenced pin (Figure 6).

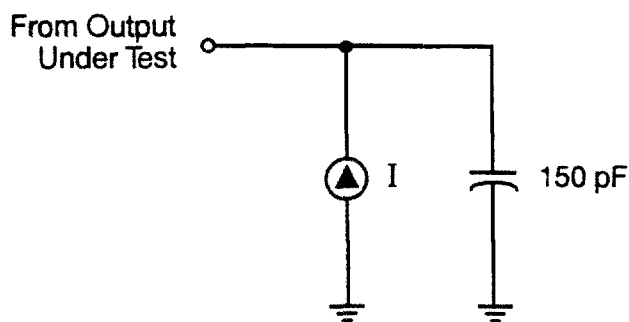


Figure 6. Test Load Diagram

CAPACITANCE

$T_A = 25^\circ\text{C}$, $V_{CC} = \text{GND} = 0\text{V}$, $f = 1.0\text{ MHz}$, unmeasured pins returned to GND.

Parameter	Max
Input capacitance	12 pF
Output capacitance	12 pF
I/O capacitance	12 pF

DC CHARACTERISTICS (Z86L72/L92 LOW VOLTAGE SPECIFICATIONS)

Preliminary

Sym	Parameter	V _{CC}	T _A = 0°C to +70°C		Typ @ 25°C	Units	Conditions	Notes
			Min	Max				
	Max Input Voltage	2.0V		7		V	I _{IN} < 250 μA	
		3.9V		7		V	I _{IN} < 250 μA	
CH	Clock Input High Voltage	2.0V	0.8 V _{CC}	V _{CC} + 0.3		V	Driven by External Clock Generator	
		3.9V	0.8 V _{CC}	V _{CC} + 0.3		V	Driven by External Clock Generator	
CL	Clock Input Low Voltage	2.0V	V _{SS} - 0.3	0.2 V _{CC}		V	Driven by External Clock Generator	
		3.9V	V _{SS} - 0.3	0.2 V _{CC}		V	Driven by External Clock Generator	
IH	Input High Voltage	2.0V	0.7 V _{CC}	V _{CC} + 0.3	0.5V _{CC}	V		
		3.9V	0.7 V _{CC}	V _{CC} + 0.3	0.5V _{CC}	V		
IL	Input Low Voltage	2.0V	V _{SS} - 0.3	0.2 V _{CC}	0.5V _{CC}	V		
		3.9V	V _{SS} - 0.3	0.2 V _{CC}	0.5V _{CC}	V		
OH1	Output High Voltage	2.0V	V _{CC} - 0.4		1.7	V	I _{OH} = -0.5 mA	
		3.9V	V _{CC} - 0.4		3.7	V	I _{OH} = -0.5 mA	
OH2	Output High Voltage (P36, P37, P00, P01)	2.0V	V _{CC} - 0.8			V	I _{OH} = -7 mA	
		3.9V	V _{CC} - 0.8			V	I _{OH} = -7 mA	
OL1	Output Low Voltage	2.0V		0.4	0.1	V	I _{OL} = 1.0 mA	
		3.9V		0.4	0.2	V	I _{OL} = 4.0 mA	
OL2*	Output Low Voltage	2.0V		0.8	0.5	V	I _{OL} = 5.0 mA	
		3.9V		0.8	0.3	V	I _{OL} = 7.0 mA	
OL2	Output Low Voltage (P36, P37, P00, P01)	2.0V		0.8	0.3	V	I _{OL} = 10 mA	
		3.9V		0.8	0.2	V	I _{OL} = 10 mA	
RH	Reset Input High Voltage	2.0V	0.8 V _{CC}	V _{CC}	1.5	V		
		3.9V	0.8 V _{CC}	V _{CC}	2.0	V		
RI	Reset Input Low Voltage	2.0V	V _{SS} - 0.3	0.2 V _{CC}	0.5	V		
		3.9V	V _{SS} - 0.3	0.2 V _{CC}	0.9	V		
OFFSET	Comparator Input Offset Voltage	2.0V		25	10	mV		
		3.9V		25	10	mV		
L	Input Leakage	2.0V	-1	1	< 1	μA	V _{IN} = O _V , V _{CC}	
		3.9V	-1	1	< 1	μA	V _{IN} = O _V , V _{CC}	
OL	Output Leakage	2.0V	-1	1	< 1	μA	V _{IN} = O _V , V _{CC}	
		3.9V	-1	1	< 1	μA	V _{IN} = O _V , V _{CC}	
R	Reset Input Pull-Up Current	2.0V		-230	-50	μA	V _{IN} = O _V	
		3.9V		-400	-90	μA	V _{IN} = O _V	
IC	Supply Current	2.0V		10	4	mA	@ 8.0 MHz	1,2
		3.9V		15	10	mA	@ 8.0 MHz	1,2
		2.0V		250	100	μA	@ 32 kHz	1,2,8
		3.9V		850	500	μA	@ 32 kHz	1,2,8

Sym	Parameter	V _{CC}	T _A = 0°C to +70°C		Typ @ 25°C	Units	Conditions	Notes
			Min	Max				
I _{CC1}	Standby Current (WDT Off)	2.0V		3	1	mA	HALT Mode V _{IN} = 0 _V , V _{CC} @ 8.0 MHz	1,2
		3.9V		5	4	mA	HALT Mode V _{IN} = 0 _V , V _{CC} @ 8.0 MHz	1,2
		2.0V		2	0.8	mA	Clock Divide-by- 16 @ 8.0 MHz	1,2
		3.9V		4	2.5	mA	Clock Divide-by- 16 @ 8.0 MHz	1,2
I _{CC2}	Standby Current	2.0V		8	2	μA	STOP Mode V _{IN} = 0 _V , V _{CC} WDT is not Running	3,5
		3.9V		10	3	μA	STOP Mode V _{IN} = 0 _V , V _{CC} WDT is not Running	3,5
		2.0V		500	310	μA	STOP Mode V _{IN} = 0 _V , V _{CC} WDT is not Running	
		3.9V		800	600	μA	STOP Mode V _{IN} = 0 _V , V _{CC} WDT is not Running	
T _{POR}	Power-On Reset	2.0V	12	75	18	ms		
		3.9V	5	20	7	ms		
V _{RAM}	Static RAM Data Retention Voltage	V _{RAM}	0.8		0.5	V		6
V _{LV}	V _{CC} Low Voltage Protection			2.15	1.7	V	8 MHz max Ext. CLK Freq.	4
Notes:	I _{CC1}	Typ	Max	Unit	Frequency			
	Crystal/Resonator	3.0 mA	5	mA	8.0 MHz			
	External Clock Drive	0.3 mA	5	mA	8.0 MHz			

1. All outputs unloaded, inputs at rail.
2. CL1 = CL2 = 100 pF.
3. Same as note [4] except inputs at V_{CC}.
4. The V_{LV} increases as the temperature decreases.
5. Oscillator stopped
6. Oscillator stops when V_{CC} falls below V_{LV} limit.
7. 32 kHz clock driver input

* All Outputs excluding P00, P01, P36, and P37.

DC CHARACTERISTICS (Z86C72/C92 SPECIFICATIONS)

Preliminary

Sym	Parameter	V _{CC}	T _A = 0°C to +70°C		Typ @ 25°C	Units	Conditions	Notes
			Min	Max				
	Max Input Voltage	4.5V		7		V	I _{IN} 250 μA	
		5.5V		7		V	I _{IN} 250 μA	
V _{CH}	Clock Input High Voltage	4.5V 5.5V	0.9 V _{CC} 0.9 V _{CC}	V _{CC} + 0.3 V _{CC} + 0.3		V	Driven by External Clock Generator	
V _{CL}	Clock Input Low Voltage	4.5V 5.5V	V _{SS} - 0.3 V _{SS} - 0.3	0.2 V _{CC} 0.2 V _{CC}		V	Driven by External Clock Generator	
V _{IH}	Input High Voltage	4.5V 5.5V	0.7 V _{CC} 0.7 V _{CC}	V _{CC} + 0.3 V _{CC} + 0.3	0.5V _{CC} 0.5V _{CC}	V	Driven by External Clock Generator	
V _{IL}	Input Low Voltage	4.5V 5.5V	V _{SS} - 0.3 V _{SS} - 0.3		0.5V _{CC} 0.5V _{CC}	V		
V _{OH1}	Output High Voltage	4.5V 5.5V	V _{CC} - 0.4 V _{CC} - 0.4		4.4 5.4	V	I _{OH} = -0.5 mA I _{OH} = -0.5 mA	
V _{OH2}	Output High Voltage (P36, P37)	4.5V 5.5V	V _{CC} - 0.8 V _{CC} - 0.8			V V	I _{OH} = -7 mA I _{OH} = -7 mA	
V _{OL1}	Output Low Voltage	4.5V 5.5V		0.4 0.4	0.1 0.2	V V	I _{OL} = 1.0 mA I _{OL} = 4.0 mA	
V _{OL2*}	Output Low Voltage	4.5V 3.9 V		0.8 0.8	0.3 0.4	V V	I _{OL} = 5.0 mA I _{OL} = 7.0 mA	
V _{OL2}	Output Low Voltage (P00, P01, P36,P37)	4.5V 5.5V		0.8 0.8	0.3 0.2	V	I _{OL} = 10 mA	
V _{RH}	Reset Input High Voltage	4.5V 5.5V	0.8 V _{CC} 0.8 V _{CC}	V _{CC} V _{CC}	2.5 3.0	V V		
V _{RI}	Reset Input Low Voltage	4.5V 5.5V	V _{SS} - 0.3 V _{SS} - 0.3	0.2 V _{CC} 0.2 V _{CC}	0.5 0.9			
V _{OFFSET}	Comparator Input Offset Voltage	4.5V 5.5V		25 25	10 10	mV mV		
I _{IL}	Input Leakage	4.5V 5.5V	-1 -1	1 1	<1 <1	μA μA	V _{IN} = 0 _V , V _{CC} V _{IN} = 0 _V , V _{CC}	
I _{OL}	Output Leakage	4.5V 5.5V	-1 -1	1 1	<1 <1	μA μA	V _{IN} = 0 _V , V _{CC} V _{IN} = 0 _V , V _{CC}	
I _{IR}	Reset Input Current	4.5V 5.5V		-500 -800		μA μA		
I _{CC}	Supply Current	4.5V 5.5V		20 30		mA mA	@8.0 MHz @8.0 MHz	1,2 1,2
	WDT Off	4.5V 5.5V		1000 1250		μA μA	@ 32 kHz @ 32 kHz	1,2,8 1,2,8

Sym	Parameter	V _{CC}	T _A = 0°C to +70°C		Typ @ 25°C	Units	Conditions	Notes
			Min	Max				
I _{CC1}	Standby Current (WDT Off)	4.5V		6	2	mA	HALT Mode V _{IN} = 0 _V , V _{CC} @ 8.0 MHz	1,2
		5.5V		8	5	mA	HALT Mode	1,2
		4.5V		5	1.0	mA	V _{IN} = 0 _V , V _{CC} @ 8.0 MHz	1,2
		5.5V		7	3.0	mA	Clock Divide-by- 16 @ 8.0 MHz Clock Divide-by- 16 @ 8.0 MHz	1,2
I _{CC2}	Standby Current	4.5V		8	2	μA	STOP Mode V _{IN} = 0 _V , V _{CC} WDT is not Running	3,5
		5.5V		10	3	μA	STOP Mode	3,5
		4.5V		500	310	μA	V _{IN} = 0 _V , V _{CC}	3,5
		5.5V		800	600	μA	WDT is not Running STOP Mode V _{IN} = 0 _V , V _{CC} WDT is Running	
T _{POR}	Power-On Reset	4.5V	5.0	75	8.0	ms		
		5.5V	4.0	20	6.0	ms		
V _{RAM}	Static RAM Data Retention Voltage	V _{ram}	0.8		0.5	V		6
V _{LV}	V _{CC} Low Voltage Protection			2.15	1.7	V	8 MHz max Ext. CLK Freq.	4
Notes:	I _{CC1}	Typ	Max	Unit	Frequency			
	Crystal/Resonator	3.5 mA	5	mA	8.0 MHz			
	External Clock Drive	0.8 mA	5	mA	8.0 MHz			

1. All outputs unloaded, inputs at rail.
 2. CL1 = CL2 = 100 pF
 3. Same as note [4] except inputs at V_{CC}.
 4. The V_{LV} increases as the temperature decreases.
 5. Oscillator stopped
 6. Oscillator stops when V_{CC} falls below V_{LV} limit.
 7. 32 kHz clock driver input
- * All Outputs excluding P00, P01, P36, and P37.

AC CHARACTERISTICS

External I/O or Memory Read and Write Timing Diagram

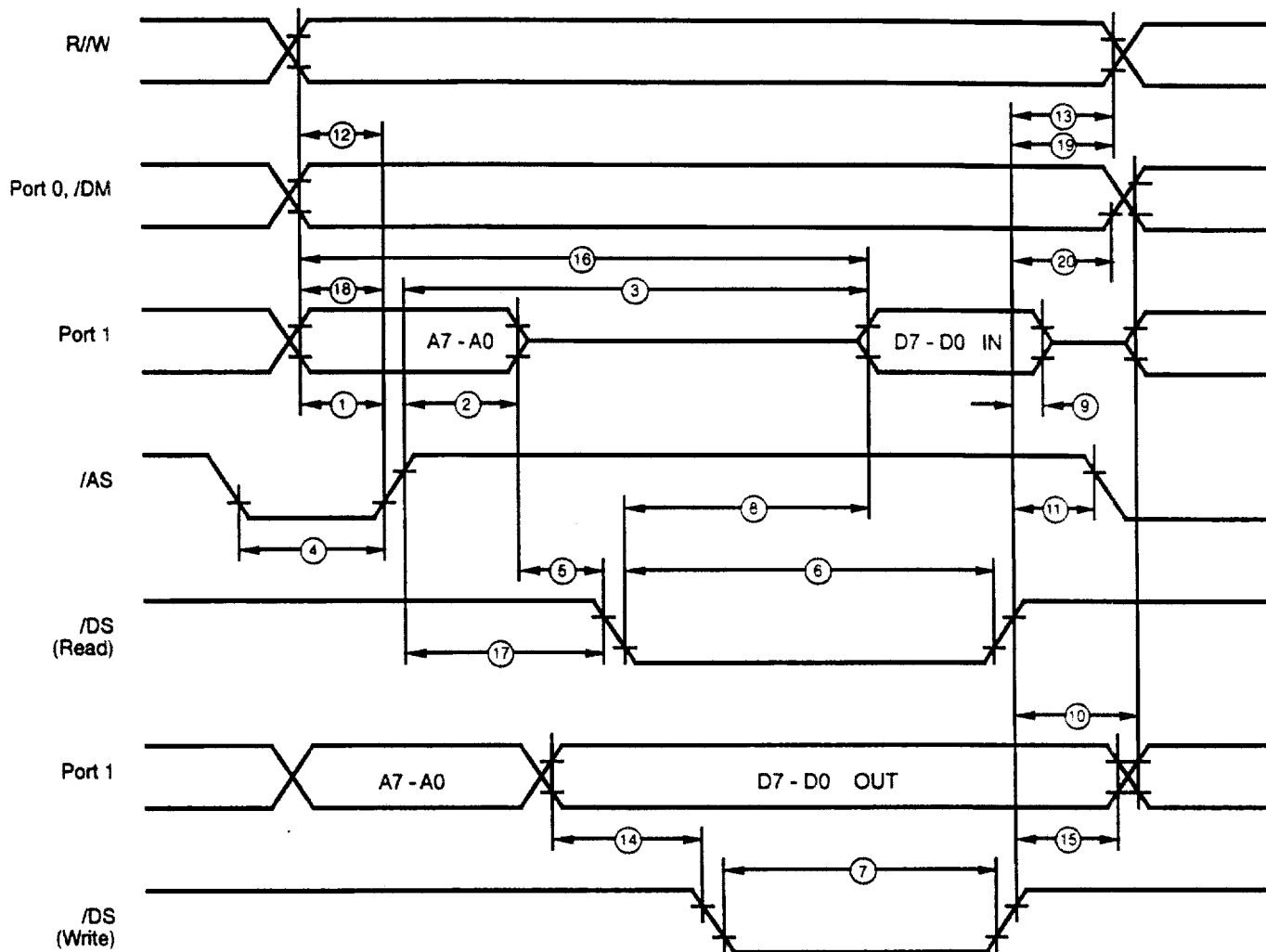


Figure 7. External I/O or Memory Read/Write Timing

AC CHARACTERISTICS (Z86L72/L92 LOW VOLTAGE SPECIFICATIONS)

Preliminary

External I/O or Memory Read and Write Timing Table

$T_A = 0^\circ\text{C to } +70^\circ\text{C}$ 8.0MHz							
No	Symbol	Parameter	V_{CC}	Min	Max	Units	Notes
1	TdA(AS)	Address Valid to /AS Rising Delay	2.0V	55		ns	2
			3.9V	55		ns	
2	TdAS(A)	/AS Rising to Address Float Delay	2.0V	70		ns	2
			3.9V	70		ns	
3	TdAS(DR)	/AS Rising to Read Data Required Valid	2.0V		400	ns	1,2
			3.9V		400	ns	
4	TwAS	/AS Low Width	2.0V	80		ns	2
			3.9V	80		ns	
5	Td	Address Float to /DS Falling	2.0V	0		ns	
			3.9V	0		ns	
6	TwDSR	/DS (Read) Low Width	2.0V	300		ns	1,2
			3.9V	300		ns	
7	TwDSW	/DS (Write) Low Width	2.0V	165		ns	1,2
			3.9V	165		ns	
8	TdDSR(DR)	/DS Falling to Read Data Required Valid	2.0V		260	ns	1,2
			3.9V		260	ns	
9	ThDR(DS)	Read Data to /DS Rising Hold Time	2.0V	0		ns	2
			3.9V	0		ns	
10	TdDS(A)	/DS Rising to Address Active Delay	2.0V	85		ns	2
			3.9V	95		ns	
11	TdDS(AS)	/DS Rising to /AS Falling Delay	2.0V	60		ns	2
			3.9V	70		ns	
12	TdRW(AS)	R/W Valid to /AS Rising Delay	2.0V	70		ns	2
			3.9V	70		ns	
13	TdDS(R/W)	/DS Rising to R/W Not Valid	2.0V	70		ns	2
			3.9V	70		ns	
14	TdDW(DSW)	Write Data Valid to /DS Falling (Write) Delay	2.0V	80		ns	2
			3.9V	80		ns	
15	TdDS(DW)	/DS Rising to Write Data Not Valid Delay	2.0V	70		ns	2
			3.9V	80		ns	
16	TdA(DR)	Address Valid to Read Data Required Valid	2.0V		475	ns	1,2
			3.9V		475	ns	
17	TdAS(DS)	/AS Rising to /DS Falling Delay	2.0V	100		ns	2
			3.9V	100		ns	
18	TdDM(AS)	/DM Valid to /AS Falling Delay	2.0V	55		ns	2
			3.9V	55		ns	
19	TdDS(DM)	/DS Rise to /DM Valid Delay	2.0V	70		ns	
			3.9V	70		ns	
20	ThDS(A)	/DS Rise to Address Valid Hold Time	2.0V	70		ns	
			3.9V	70			

Notes:

1. When using extended memory timing add 2 TpC.
2. Timing numbers given are for minimum TpC.

Standard Test LoadAll timing references use 0.9 V_{CC} for a logic 1 and 0.1 V_{CC} for a logic 0.

AC CHARACTERISTICS (Z86C72/C92 SPECIFICATIONS)

Preliminary

External I/O or Memory Read and Write Timing Table

$T_A = 0^\circ\text{C to } +70^\circ\text{C}$							
16.0 MHz							
No	Symbol	Parameter	V_{CC}	Min	Max	Units	Notes
1	TdA(AS)	Address Valid to /AS	4.5V	25		ns	2
		Rising Delay	5.5V	25		ns	
2	TdAS(A)	/AS Rising to Address	4.5V	35		ns	2
		Float Delay	5.5V	35		ns	
3	TdAS(DR)	/AS Rising to Read	4.5V		180	ns	1,2
		Data Required Valid	5.5V		180	ns	
4	TwAS	/AS Low Width	4.5V	40		ns	2
			5.5V	40		ns	
5	Td	Address Float to /DS	4.5V	0		ns	
		Falling	5.5V	0		ns	
6	TwDSR	/DS (Read) Low Width	4.5V	135		ns	1,2
			5.5V	135		ns	
7	TwDSW	/DS (Write) Low Width	4.5V	80		ns	1,2
			5.5V	80		ns	
8	TdDSR(DR)	/DS Falling to Read	4.5V		75	ns	1,2
		Data Required Valid	5.5V		75	ns	
9	ThDR(DS)	Read Data to	4.5V	0		ns	2
		/DS Rising Hold Time	5.5V	0		ns	
10	TdDS(A)	/DS Rising to Address	4.5V	50		ns	2
		Active Delay	5.5V	50		ns	
11	TdDS(AS)	/DS Rising to /AS	4.5V	35		ns	2
			5.5V	35		ns	
12	TdR/W(AS)	R/W Valid to /AS	4.5V	25		ns	2
		Rising Delay	5.5V	25		ns	
13	TdDS(R/W)	/DS Rising to	4.5V	35		ns	2
		R/W Not Valid	5.5V	35		ns	
14	TdDW(DSW)	Write Data Valid to	4.5V	25		ns	2
		/DS Falling (Write) Delay	5.5V	25		ns	
15	TdDS(DW)	/DS Rising to Write	4.5V	35		ns	2
		Data Not Valid Delay	5.5V	35		ns	
16	TdA(DR)	Address Valid to Read	4.5V		230	ns	1,2
		Data Required Valid	5.5V		230	ns	
17	TdAS(DS)	/AS Rising to /DS	4.5V	45		ns	2
		Falling Delay	5.5V	45		ns	
18	TdM(AS)	/DM Valid to /AS	4.5V	30		ns	2
		Falling Delay	5.5V	30		ns	
19	TdDS(DM)	/DS Rise to /DM Valid	4.5V	70		ns	
		Delay	5.5V	70		ns	
20	ThDS(A)	/DS Rise to Address	4.5V	70		ns	
		Valid Hold Time	5.5V	70		ns	

Notes:

1. When using extended memory timing add 2 TpC.
2. Timing numbers given are for minimum TpC.

Standard Test Load

All timing references use 0.9 V_{CC} for a logic 1 and 0.1 V_{CC} for a logic 0.

AC CHARACTERISTICS
Additional Timing Diagram

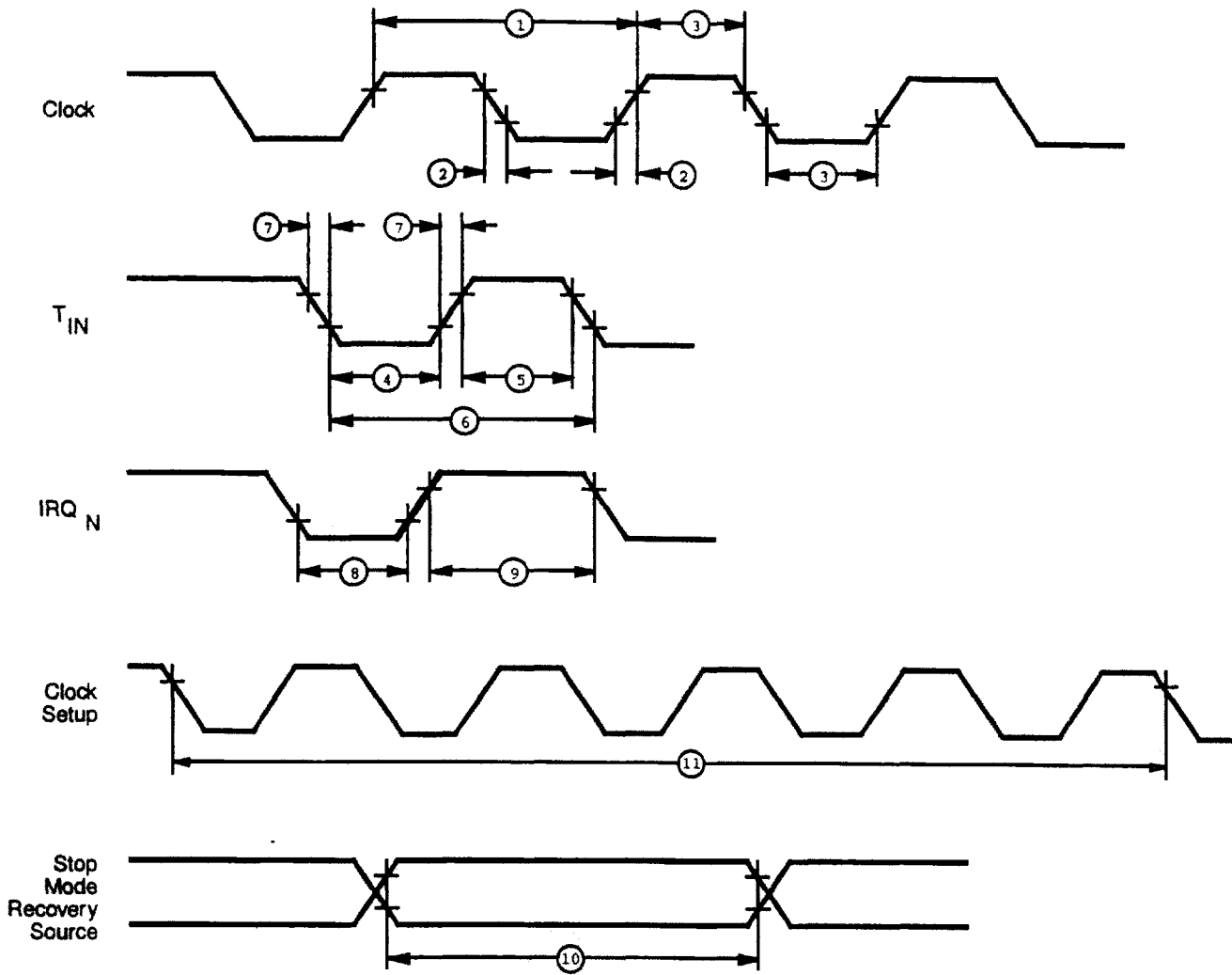


Figure 8. Additional Timing

AC CHARACTERISTICS (Z86L72/L92 LOW VOLTAGE SPECIFICATIONS)

Preliminary
Additional Timing Table

T _A = 0°C to +70°C 8.0MHz							
No	Sym	Parameter	V _{CC}	Min	Max	Units	Notes
1	TpC	Input Clock Period	2.0V	121	DC	ns	1
			3.9V	121	DC	ns	1
2	TrC,TfC	Clock Input Rise and Fall Times	2.0V		25	ns	1
			3.9V		25	ns	1
3	TwC	Input Clock Width	2.0V	37		ns	1
			3.9V	37		ns	1
4	TwTinL	Timer Input Low Width	2.0V	100		ns	1
			3.9V	70		ns	1
5	TwTinH	Timer Input High Width	2.0V	3TpC			1
			3.9V	3TpC			1
6	TpTin	Timer Input Period	2.0V	8TpC			1
			3.9V	8TpC			1
7	TrTin,TfTin	Timer Input Rise and Fall Timers	2.0V		100	ns	1
			3.9V		100	ns	1
8A	TwlL	Interrupt Request Low Time	2.0V	100		ns	1,2
			3.9V	70		ns	1,2
8B	TwlL	Interrupt Request Low Time	2.0V	5TpC			1,3
			3.9V	5TpC			1,3
9	TwhH	Interrupt Request Input High Time	2.0V	5TpC			1,2
			3.9V	5TpC			1,2
10	Twsm	Stop-Mode Recovery Width Spec	2.0V	12		ns	7
			3.9V	12		ns	7
			2.0V	5 TpC		ns	6
			3.9V	5 TpC		ns	6
11	Tost	Oscillator Start-Up Time	2.0V		5TpC		4
			3.9V		5TpC		4
12	Twdt	Watch-Dog Timer Delay Time (5 ms) (10 ms) (20 ms) (80 ms)	2.0V	12	75	ms	
			3.9V	5	20	ms	
			2.0V	25	150	ms	
			3.9V	10	40	ms	
			2.0V	50	300	ms	
			3.9V	20	80	ms	
		2.0V	225	1200	ms		
		3.9V	80	320	ms		

- Notes:**
1. Timing Reference uses 0.9 V_{CC} for a logic 1 and 0.1 V_{CC} for a logic 0.
 2. Interrupt request through Port 3 (P33-P31).
 3. Interrupt request through Port 3 (P30).
 4. SMR bit D5 = 0

AC CHARACTERISTICS(Z86C72/C92 SPECIFICATIONS)

Preliminary

Additional Timing Table

$T_A = 0^\circ\text{C to } +70^\circ\text{C}$ 16.0 MHz							
No	Symbol	Parameter	V_{CC}	Min	Max	Units	Notes
1	TpC	Input Clock Period	4.5V	63	DC	ns	1
			5.5V	63	DC	ns	1
2	TrC, TfC	Clock Input Rise and Fall Times	4.5V		15	ns	1
			5.5V		15	ns	1
3	TwC	Input Clock Width	4.5V	31		ns	1
			5.5V	31		ns	1
4	TwTinL	Timer Input Low Width	4.5V	100		ns	1
			5.5V	70		ns	1
5	TwTinH	Timer Input High Width	4.5V	5TpC			1
			5.5V	5TpC			1
6	TpTin	Timer Input Period	4.5V	8TpC			1
			5.5V	8TpC			1
7	TrTin, Tftin	Timer Input Rise	4.5V		100	ns	1
			5.5V		100	ns	1
8A	TwIL	Interrupt Request Low Time	4.5V	100		ns	1,2
			5.5V	70		ns	1,2
8B	TwIL	Int. Request Low Time	4.5V	5TpC			1,3
			5.5V	5TpC			1,3
9	TwIH	Interrupt Request Input High Time	4.5V	5TpC			1,2
			5.5V	5TpC			1,2
10	Twsm	Stop-Mode Recovery Width Spec	4.5V	12		ns	8
			5.5V	12		ns	8
			4.5V	5TpC			7
			5.5V	5TpC			7
11	Tost	Oscillator Start-up Time	4.5V		5TpC		4
			5.5V		5TpC		4
12	Twdt	Watch-Dog Timer Delay Time (2.0 ms)	4.5V	2.0		ms	D0=0, 5
			5.5V	2.0		ms	D1=0, 5
			4.5V	4.0		ms	D0=1, 5
			5.5V	4.0		ms	D1=0, 8
			4.5V	8.0		ms	D0=1, 5
			5.5V	8.0		ms	D1=0, 8
			4.5V	32		ms	D0=1, 5
			5.5V	32		ms	D1=0, 8

Notes:

1. Timing Reference uses 0.9 V_{CC} for a logic 1 and 0.1 V_{CC} for a logic 0.
2. Interrupt request through Port 3 (P33-P31).
3. Interrupt request through Port 3 (P30).
4. SMR bit D5 = 0
5. Reg. WDTMR bit D0=1
6. Reg. SMR bit D5 = 0
7. Reg. SMR bit D5 = 1
8. Reg. WDTMR bit D1=0

AC CHARACTERISTICS
 Handshake Timing Diagrams

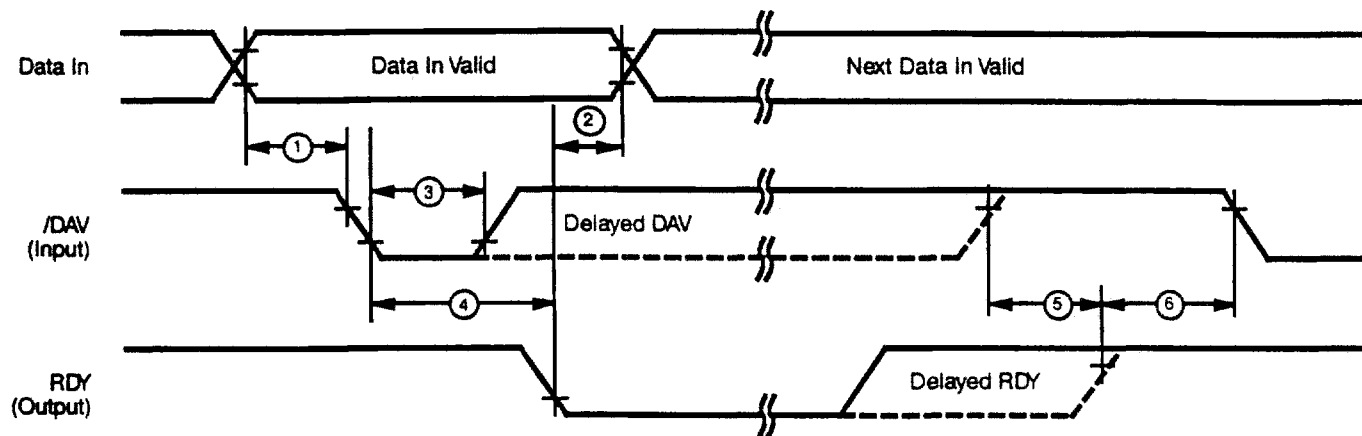


Figure 9. Port I/O with Input Handshake Timing

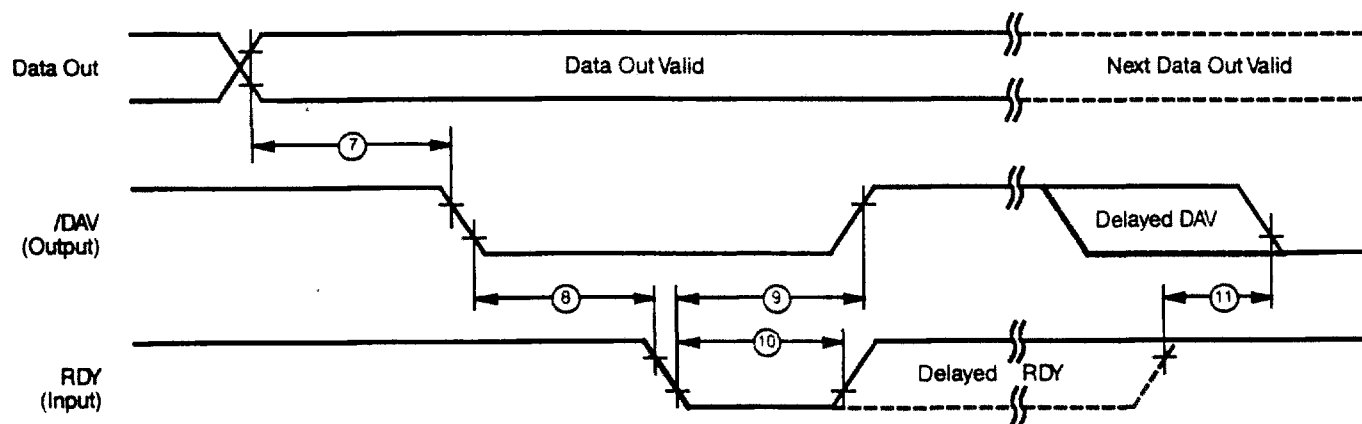


Figure 10. Port I/O with Output Handshake Timing

AC CHARACTERISTICS (Z86L72/L92 LOW VOLTAGE SPECIFICATIONS)

Preliminary

Handshake Timing Table

No	Sym	Parameter	V _{CC}	T _A = 0°C to +70°C		Data
				Min	Max	Direction
1	TsDI(DAV)	Data In Setup Time	2.0V	0		IN
			3.9V	0		IN
2	ThDI(DAV)	Data In Hold Time	2.0V	0		IN
			3.9V	0		IN
3	TwDAV	Data Available Width	2.0V	155		IN
			3.9V	110		IN
4	TdDAVI(RDY)	DAV Falling to RDY Falling Delay	2.0V		160	IN
			3.9V		115	IN
5	TdDAVIId(RDY)	DAV Rising to RDY Falling Delay	2.0V		120	IN
			3.9V		80	IN
6	TdRDYO(DAV)	RDY Rising to DAV Falling Delay	2.0V	0		IN
			3.9V	0		IN
7	TdDO(DAV)	Data Out to DAV Falling Delay	2.0V	63		OUT
			3.9V	63		OUT
8	TdDAV0(RDY)	DAV Falling to RDY Falling Delay	2.0V	0		OUT
			3.9V	0		OUT
9	TdRDY0(DAV)	RDY Falling to DAV Rising Delay	2.0V		160	OUT
			3.9V		115	OUT
10	TwRDY	RDY Width	2.0V	110		OUT
			3.9V	80		OUT
11	TdRDY0d(DAV)	RDY Rising to DAV Falling Delay	2.0V		110	OUT
			3.9V		80	OUT

AC CHARACTERISTICS(Z86C72/C92 SPECIFICATIONS)

Preliminary

Handshake Timing Table

T _A = 0°C to +70°C 16.0 MHz						
No	Symbol	Parameter	V _{CC}	Min	Max	Data Direction
1	TSD(DAV)	Data in Setup Time	4.5V	0		IN
			5.5V	0		IN
2	ThD(DAV)	Data in Hold Time	4.5V	160		IN
			5.5V	115		IN
3	TwDAV	Data Available Width	4.5V	155		IN
			5.5V	110		IN
4	TdDAVI(RDY)	DAV Falling to RDY Falling Delay	4.5V		160	IN
			5.5V		115	IN
5	TdDAVIId(RDY)	DAV Rising to RDY Falling Delay	4.5V		120	IN
			5.5V		80	IN
6	TdRDY)(DAV)	RDY Rising to DAV Falling Delay	4.5V	0		IN
			5.5V	0		IN
7	TdD0(DAV)	Data Out to DAV Falling Delay	4.5V	31		OUT
			5.5V	31		OUT
8	TdDAV0(RDY)	DAV Falling to RDY Falling Delay	4.5V	0		OUT
			5.5V	0		OUT
9	TdRDY0(DAV)	RDY Falling to DAV	4.5V		160	OUT
			5.5V		115	OUT
10	TwrDY	RDY Width	4.5V	110		OUT
			5.5V	80		OUT
11	TdRDY0d(DAV)	RDY Rising to DAV Falling Dealy	4.5V		110	OUT
			5.5V		80	OUT

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The product represented by this CPS is newly introduced and Zilog has not completed the full characterization of the product. The CPS states what Zilog knows about this product at this time, but additional features or non-conformance with some aspects of the CPS may be found,

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