

Features

- 3.3 V operation (3.0 V–3.6 V)
- High speed
 - $t_{AA} = 15$ ns
- CMOS for optimum speed/power
- Low Active Power
 - 576 mW (max)
- Low CMOS Standby Power
 - 1.80 mW (max)
- Automatic power-down when deselected
- Independent control of upper and lower bits
- Available in 44-pin TSOP II and 400-mil SOJ
- Available in a 48-ball Mini BGA package

Functional Description^[1]

The CY7C1021BNV33 is a high-performance CMOS static RAM organized as 65,536 words by 16 bits. This device has an automatic power-down feature that significantly reduces power consumption when deselected.

Writing to the device is accomplished by taking Chip Enable (\overline{CE}) and Write Enable (WE) inputs LOW. If Byte Low Enable (BLE) is LOW, then data from I/O pins (I/O₀ through I/O₇), is written into the location specified on the address pins (A₀ through A₁₅). If Byte High Enable (BHE) is LOW, then data from I/O pins (I/O₈ through I/O₁₅) is written into the location specified on the address pins (A₀ through A₁₅).

Reading from the device is accomplished by taking Chip Enable (\overline{CE}) and Output Enable (\overline{OE}) LOW while forcing the Write Enable (WE) HIGH. If Byte Low Enable (BLE) is LOW, then data from the memory location specified by the address pins will appear on I/O₀ to I/O₇. If Byte High Enable (BHE) is LOW, then data from memory will appear on I/O₈ to I/O₁₅. See the truth table at the back of this data sheet for a complete description of read and write modes.

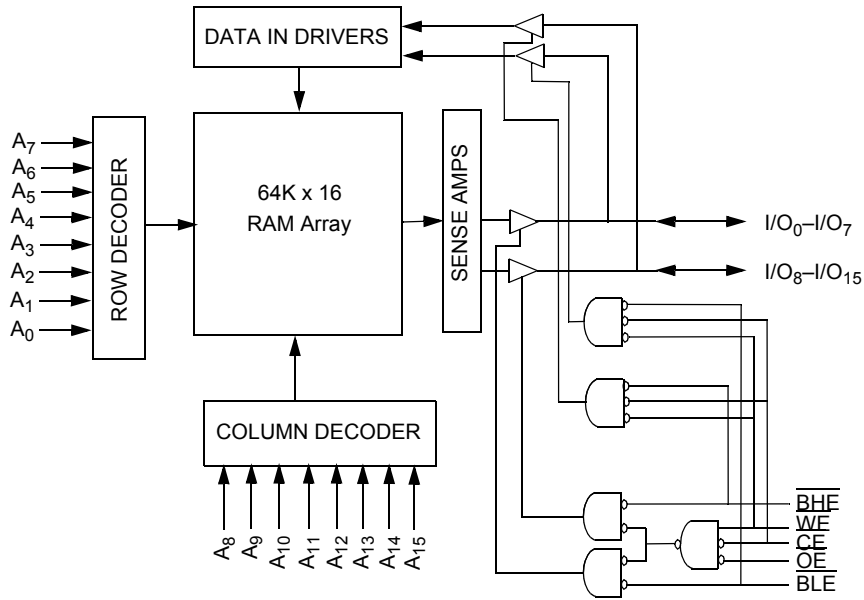
The input/output pins (I/O₀ through I/O₁₅) are placed in a high-impedance state when the device is deselected (\overline{CE} HIGH), the outputs are disabled (\overline{OE} HIGH), the BHE and BLE are disabled (BHE, BLE HIGH), or during a write operation (\overline{CE} LOW, and WE LOW).

The CY7C1021BNV33 is available in 400-mil-wide SOJ, standard 44-pin TSOP Type II, and 48-ball mini BGA packages.

Note

1. For guidelines on SRAM system design, please refer to the 'System Design Guidelines' Cypress application note, available on the internet at www.cypress.com.

Logic Block Diagram



Selection Guide

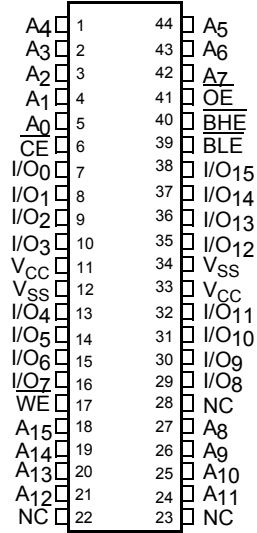
| | -15 |
|-----------------------------------|------------|
| Maximum Access Time (ns) | 15 |
| Maximum Operating Current (mA) | 160 |
| Maximum CMOS Standby Current (mA) | 0.5 |

Contents

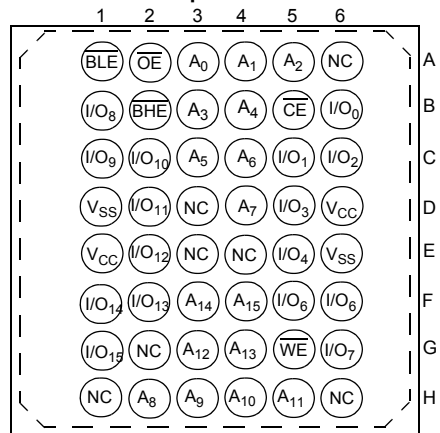
| | | | |
|----------------------------------------------------------------|----------|------------------------------------------------------|-----------|
| Pin Configurations | 4 | Truth Table | 11 |
| Maximum Ratings | 5 | Ordering Information | 12 |
| Operating Range | 5 | Ordering Code Definitions | 12 |
| Electrical Characteristics | 5 | Package Diagrams | 13 |
| Capacitance | 5 | Acronyms | 15 |
| AC Test Loads and Waveforms | 6 | Document Conventions | 15 |
| Switching Characteristics | 7 | Units of Measure | 15 |
| Data Retention Characteristics | 8 | Document History Page | 16 |
| Data Retention Waveform | 8 | Sales, Solutions, and Legal Information | 17 |
| Switching Waveforms | 9 | Worldwide Sales and Design Support | 17 |
| Read Cycle No. 1 | 9 | Products | 17 |
| Read Cycle No. 2 (<u>OE</u> Controlled) | 9 | PSoC Solutions | 17 |
| Write Cycle No. 1 (<u>CE</u> Controlled) | 10 | | |
| Write Cycle No. 2 (<u>BLE</u> or <u>BHE</u> Controlled) | 10 | | |
| Write Cycle No. 2 (<u>WE</u> Controlled, <u>OE</u> LOW) | 11 | | |

Pin Configurations

SOJ / TSOP II
Top View



Mini BGA
Top View



Maximum Ratings

Exceeding maximum ratings may shorten the useful life of the device. User guidelines are not tested.

Storage Temperature -65 °C to +150 °C
 Ambient Temperature with
 Power Applied -55 °C to +125 °C
 Supply Voltage on V_{CC} to Relative GND^[2] ... -0.5 V to +4.6 V
 DC Voltage Applied to Outputs
 in High Z State^[2] -0.5 V to $V_{CC} + 0.5$ V

DC Input Voltage^[2] -0.5 V to $V_{CC} + 0.5$ V
 Current into Outputs (LOW) 20 mA
 Static Discharge Voltage > 2001 V
 (per MIL-STD-883, Method 3015)
 Latch-Up Current > 200 mA

Operating Range

| Range | Ambient Temperature | V_{CC} |
|------------|---------------------|-------------|
| Industrial | -40 °C to +85 °C | 3.3 V ± 10% |

Electrical Characteristics

Over the Operating Range

| Parameter | Description | Test Conditions | -15 | | Unit |
|-----------|-------------------------------------------------|-------------------------------------------------------------------------------------------------------|------|------------------|------|
| | | | Min | Max | |
| V_{OH} | Output HIGH Voltage | $V_{CC} = \text{Min}, I_{OH} = -4.0$ mA | 2.4 | – | V |
| V_{OL} | Output LOW Voltage | $V_{CC} = \text{Min}, I_{OL} = 8.0$ mA | – | 0.4 | V |
| V_{IH} | Input HIGH Voltage | | 2.2 | $V_{CC} + 0.3$ V | V |
| V_{IL} | Input LOW Voltage ^[2] | | -0.3 | 0.8 | V |
| I_{IX} | Input Load Current | $GND \leq V_I \leq V_{CC}$ | -1 | +1 | µA |
| I_{OZ} | Output Leakage Current | $GND \leq V_I \leq V_{CC}$, Output Disabled | -1 | +1 | µA |
| I_{CC} | V_{CC} Operating Supply Current | $V_{CC} = \text{Max}, I_{OUT} = 0$ mA, $f = f_{MAX} = 1/t_{RC}$ | – | 160 | mA |
| I_{SB1} | Automatic CE Power Down Current —TTL Inputs | Max V_{CC} , $CE \geq V_{IH}$, $V_{IN} \geq V_{IH}$ or $V_{IN} \leq V_{IL}$, $f = f_{MAX}$ | – | 40 | mA |
| I_{SB2} | Automatic CE Power Down Current —CMOS Inputs | Max V_{CC} , $CE \geq V_{CC} - 0.3$ V, $V_{IN} \geq V_{CC} - 0.3$ V or $V_{IN} \leq 0.3$ V, $f = 0$ | – | 500 | µA |

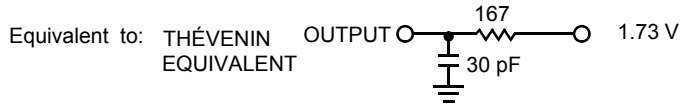
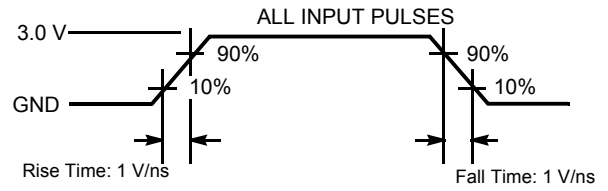
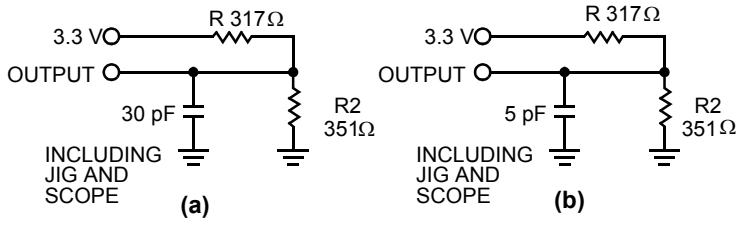
Capacitance^[3]

| Parameter | Description | Test Conditions | Max | Unit |
|-----------|--------------------|----------------------------|-----|------|
| C_{IN} | Input Capacitance | $T_A = 25$ °C, $f = 1$ MHz | 6 | pF |
| C_{OUT} | Output Capacitance | | 8 | pF |

Notes

- Minimum voltage is -2.0 V for pulse durations of less than 20 ns.
- Tested initially and after any design or process changes that may affect these parameters.

AC Test Loads and Waveforms



Switching Characteristics^[4]

Over the Operating Range

| Parameter | Description | -15 | | Unit |
|----------------------------------|--------------------------------------------------|-----|-----|------|
| | | Min | Max | |
| READ CYCLE | | | | |
| t_{RC} | Read Cycle Time | 15 | – | ns |
| t_{AA} | Address to Data Valid | – | 15 | ns |
| t_{OHA} | Data Hold from Address Change | 3 | – | ns |
| t_{ACE} | \overline{CE} LOW to Data Valid | – | 15 | ns |
| t_{DOE} | \overline{OE} LOW to Data Valid | – | 7 | ns |
| t_{LZOE} | \overline{OE} LOW to Low Z | 0 | – | ns |
| t_{HZOE} | \overline{OE} HIGH to High Z ^[5, 6] | – | 7 | ns |
| t_{LZCE} | \overline{CE} LOW to Low Z ^[6] | 3 | – | ns |
| t_{HZCE} | \overline{CE} HIGH to High Z ^[5, 6] | – | 7 | ns |
| t_{PU} | \overline{CE} LOW to Power-Up | 0 | – | ns |
| t_{PD} | \overline{CE} HIGH to Power-Down | – | 15 | ns |
| t_{DBE} | Byte Enable to Data Valid | – | 7 | ns |
| t_{LZBE} | Byte Enable to Low Z | 0 | – | ns |
| t_{HZBE} | Byte Disable to High Z | – | 7 | ns |
| WRITE CYCLE^[7] | | | | |
| t_{WC} | Write Cycle Time | 15 | – | ns |
| t_{SCE} | \overline{CE} LOW to Write End | 10 | – | ns |
| t_{AW} | Address Set-Up to Write End | 10 | – | ns |
| t_{HA} | Address Hold from Write End | 0 | – | ns |
| t_{SA} | Address Set-Up to Write Start | 0 | – | ns |
| t_{PWE} | \overline{WE} Pulse Width | 10 | – | ns |
| t_{SD} | Data Set-Up to Write End | 8 | – | ns |
| t_{HD} | Data Hold from Write End | 0 | – | ns |
| t_{LZWE} | \overline{WE} HIGH to Low Z ^[6] | 3 | – | ns |
| t_{HZWE} | \overline{WE} LOW to High Z ^[5, 6] | – | 7 | ns |
| t_{BW} | Byte Enable to End of Write | 9 | – | ns |

Notes

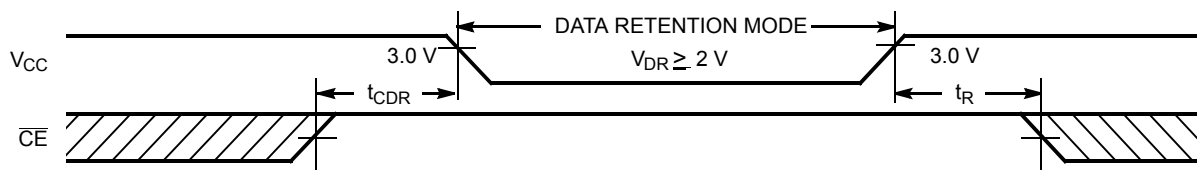
- Test conditions assume signal transition time of 3 ns or less, timing reference levels of 1.5 V, input pulse levels of 0 to 3.0 V, and output loading of the specified I_{OL}/I_{OH} and 30-pF load capacitance.
- t_{HZOE} , t_{HZBE} , t_{HZCE} , and t_{HZWE} are specified with a load capacitance of 5 pF as in part (b) of [AC Test Loads and Waveforms on page 6](#). Transition is measured ± 500 mV from steady-state voltage.
- At any given temperature and voltage condition, t_{HZCE} is less than t_{LZCE} , t_{HZOE} is less than t_{LZOE} , and t_{HZWE} is less than t_{LZWE} for any given device.
- The internal write time of the memory is defined by the overlap of \overline{CE} LOW, \overline{WE} LOW and \overline{BHE} / \overline{BLE} LOW. \overline{CE} , \overline{WE} and \overline{BHE} / \overline{BLE} must be LOW to initiate a write, and the transition of these signals can terminate the write. The input data set-up and hold timing should be referenced to the leading edge of the signal that terminates the write.

Data Retention Characteristics

Over the Operating Range (L version only)

| Parameter | Description | Conditions ^[8] | Min | Max | Unit |
|-----------------|--------------------------------------|----------------------------------------------------------------------------------------------------------------------------------------------|-----|-----|---------------|
| V_{DR} | V_{CC} for Data Retention | | 2.0 | – | V |
| I_{CCDR} | Data Retention Current | $V_{CC} = V_{DR} = 2.0\text{ V}$, $CE \geq V_{CC} - 0.3\text{ V}$, $V_{IN} \geq V_{CC} - 0.3\text{ V}$ or $V_{IN} \leq 0.3\text{ V}$ | – | 100 | μA |
| $t_{CDR}^{[9]}$ | Chip Deselect to Data Retention Time | | 0 | – | ns |
| $t_R^{[10]}$ | Operation Recovery Time | | 15 | – | ns |

Data Retention Waveform

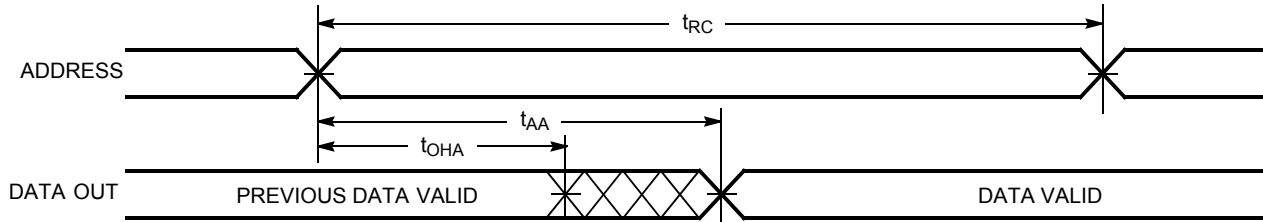


Notes

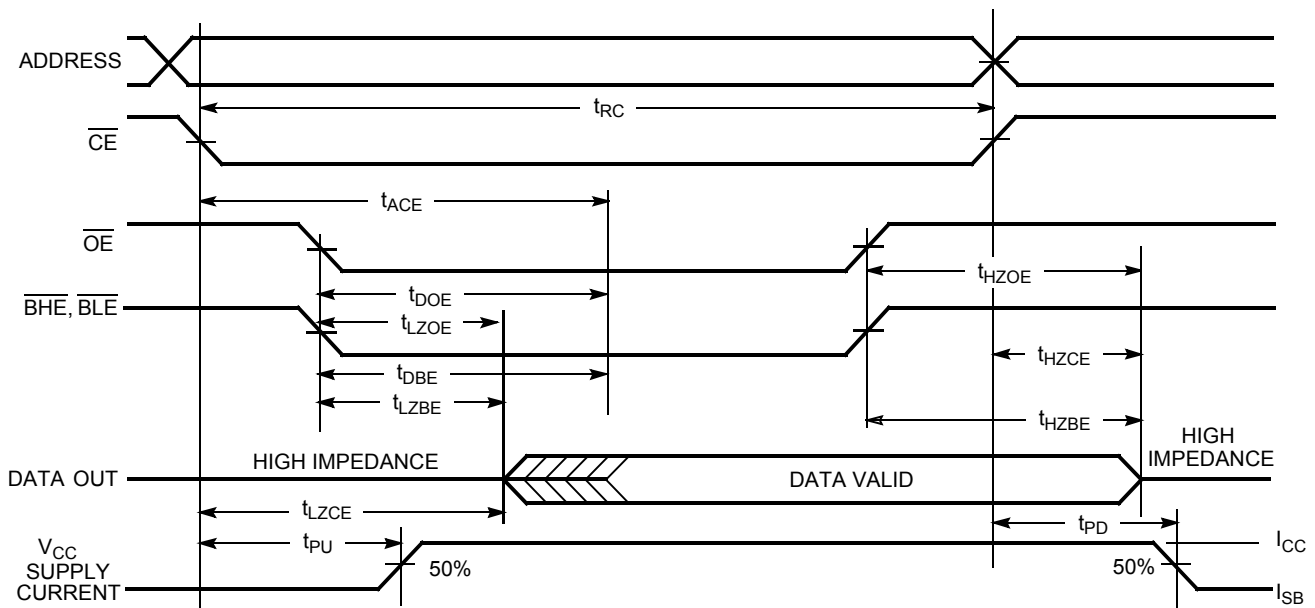
- 8. No input may exceed $V_{CC} + 0.5\text{ V}$.
- 9. Tested initially and after any design or process changes that may affect these parameters.
- 10. $t_r \leq 3\text{ ns}$ for the -12 and -15 speeds. $t_r \leq 5\text{ ns}$ for the -20 and slower speeds.

Switching Waveforms

Read Cycle No. 1^[11, 12]



Read Cycle No. 2 (\overline{OE} Controlled)^[12, 13]

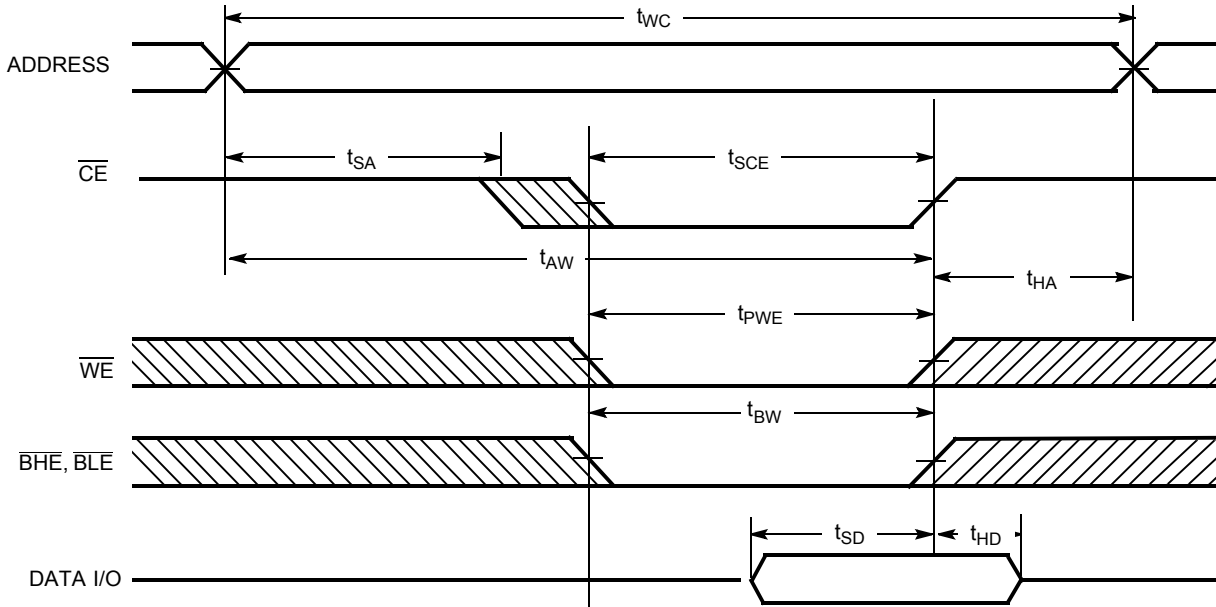


Notes

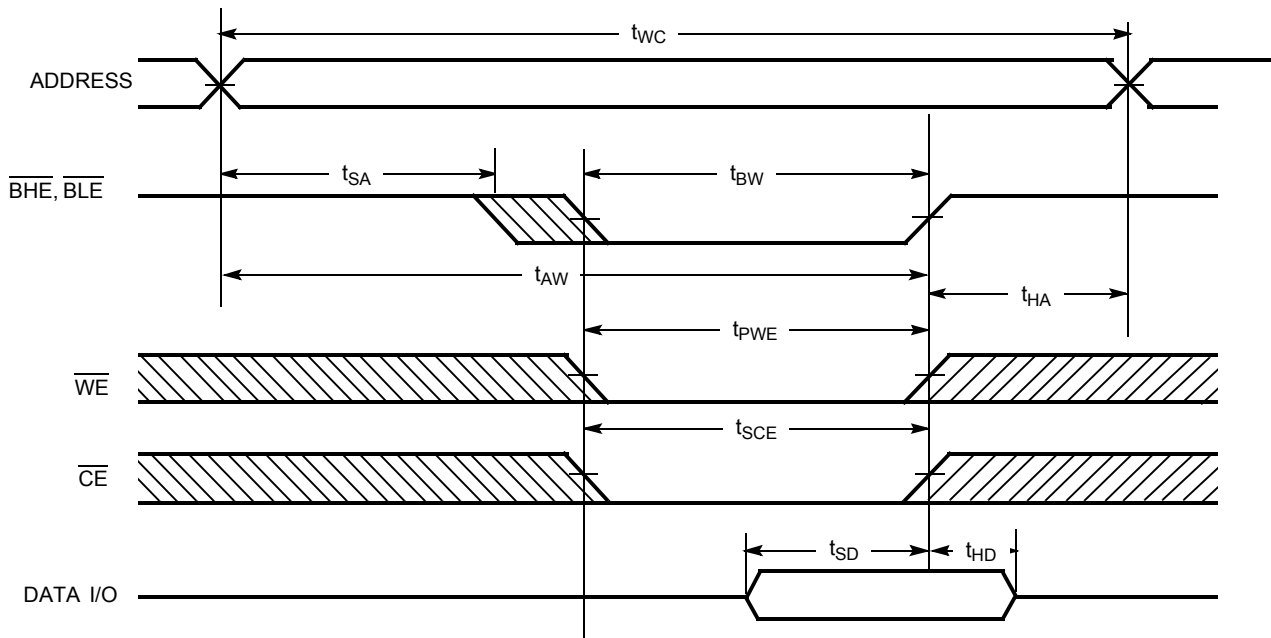
- 11. Device is continuously selected. \overline{OE} , \overline{CE} , \overline{BHE} and/or \overline{BLE} = V_{IL} .
- 12. \overline{WE} is HIGH for read cycle.
- 13. Address valid prior to or coincident with \overline{CE} transition LOW.

Switching Waveforms(continued)

Write Cycle No. 1 ($\overline{\text{CE}}$ Controlled)^[14, 15]



Write Cycle No. 2 ($\overline{\text{BLE}}$ or $\overline{\text{BHE}}$ Controlled)

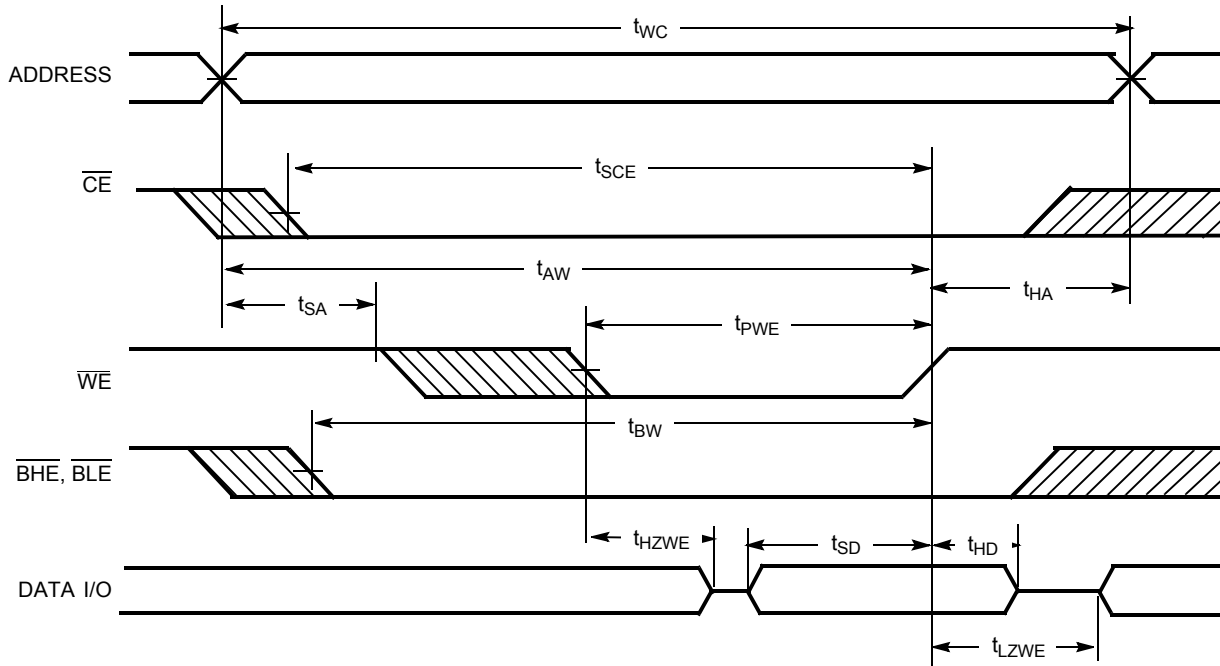


Notes

- 14. Data I/O is high impedance if $\overline{\text{OE}}$ or $\overline{\text{BHE}}$ and/or $\overline{\text{BLE}} = V_{IH}$.
- 15. If $\overline{\text{CE}}$ goes HIGH simultaneously with $\overline{\text{WE}}$ going HIGH, the output remains in a high-impedance state.

Switching Waveforms(continued)

Write Cycle No. 2 (\overline{WE} Controlled, \overline{OE} LOW)



Truth Table

| \overline{CE} | \overline{OE} | \overline{WE} | \overline{BLE} | \overline{BHE} | I/O ₀ -I/O ₇ | I/O ₈ -I/O ₁₅ | Mode | Power |
|-----------------|-----------------|-----------------|------------------|------------------|------------------------------------|-------------------------------------|----------------------------|----------------------|
| H | X | X | X | X | High Z | High Z | Power-Down | Standby (I_{SB}) |
| L | L | H | L | L | Data Out | Data Out | Read - All bits | Active (I_{CC}) |
| | | | L | H | Data Out | High Z | Read - Lower bits only | Active (I_{CC}) |
| | | | H | L | High Z | Data Out | Read - Upper bits only | Active (I_{CC}) |
| L | X | L | L | L | Data In | Data In | Write - All bits | Active (I_{CC}) |
| | | | L | H | Data In | High Z | Write - Lower bits only | Active (I_{CC}) |
| | | | H | L | High Z | Data In | Write - Upper bits only | Active (I_{CC}) |
| L | H | H | X | X | High Z | High Z | Selected, Outputs Disabled | Active (I_{CC}) |
| L | X | X | H | H | High Z | High Z | Selected, Outputs Disabled | Active (I_{CC}) |

Ordering Information

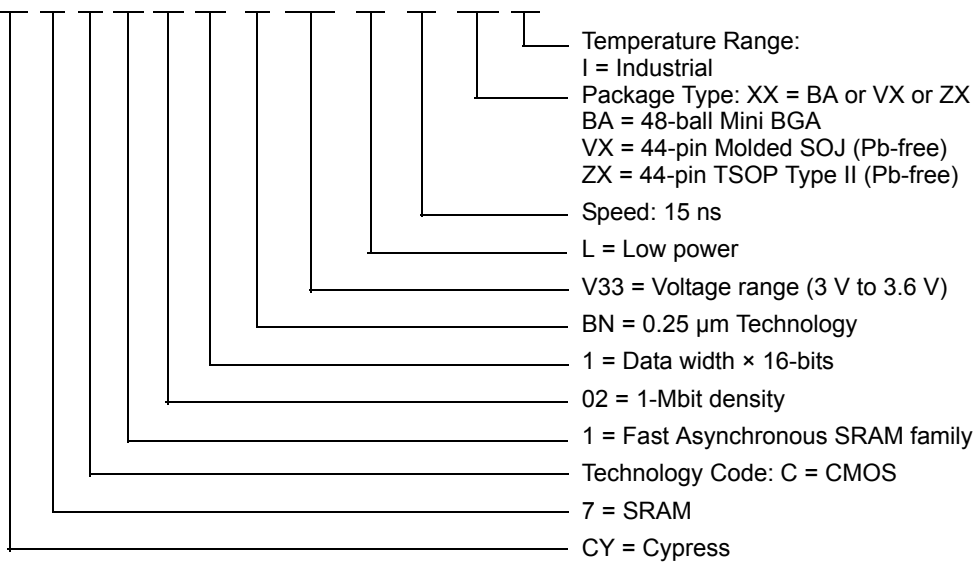
Cypress offers other versions of this type of product in many different configurations and features. The following table contains only the list of parts that are currently available. For a complete listing of all options, visit the Cypress website at <http://www.cypress.com> and refer to the product summary page at <http://www.cypress.com/products> or contact your local sales representative.

Cypress maintains a worldwide network of offices, solution centers, manufacturer’s representatives and distributors. To find the office closest to you, visit us at <http://www.cypress.com/go/datasheet/offices>.

| Speed (ns) | Ordering Code | Package Diagram | Package Type | Operating Range |
|------------|----------------------|-----------------|---------------------------------------|-----------------|
| 15 | CY7C1021BNV33L-15BAI | 51-85096 | 48-ball Mini BGA (7 mm × 7 mm) | Industrial |
| | CY7C1021BNV33L-15VXI | 51-85082 | 44-pin (400-Mil) Molded SOJ (Pb-free) | |
| | CY7C1021BNV33L-15ZXI | 51-85087 | 44-pin TSOP Type II (Pb-free) | |

Ordering Code Definitions

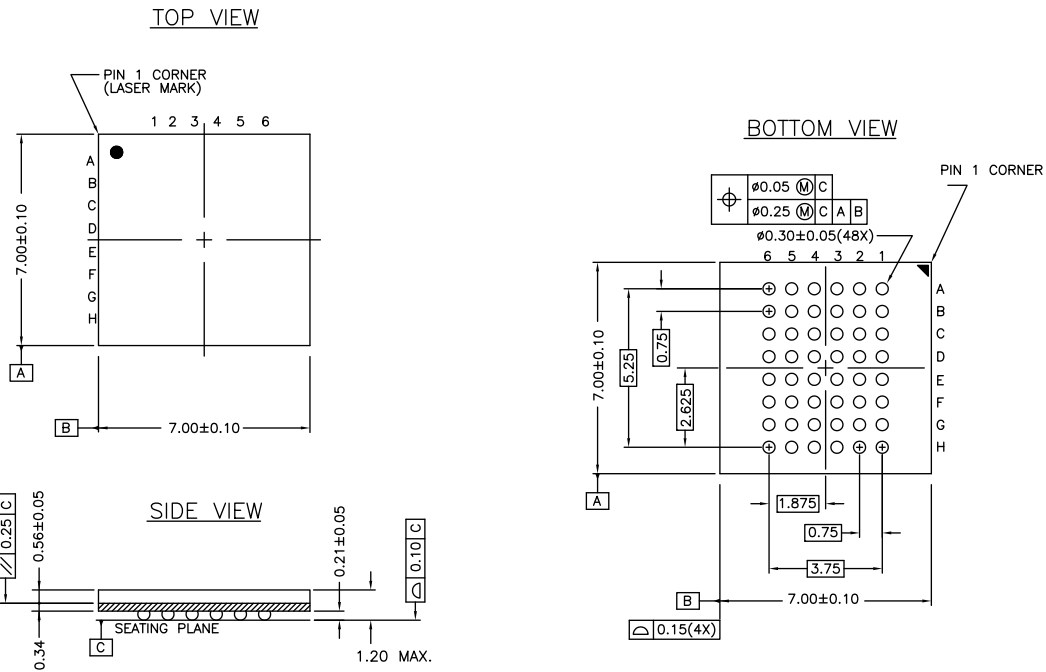
CY 7 C 1 02 1 BN V33 L - 15 XX I



Please contact local sales representative regarding availability of these parts.

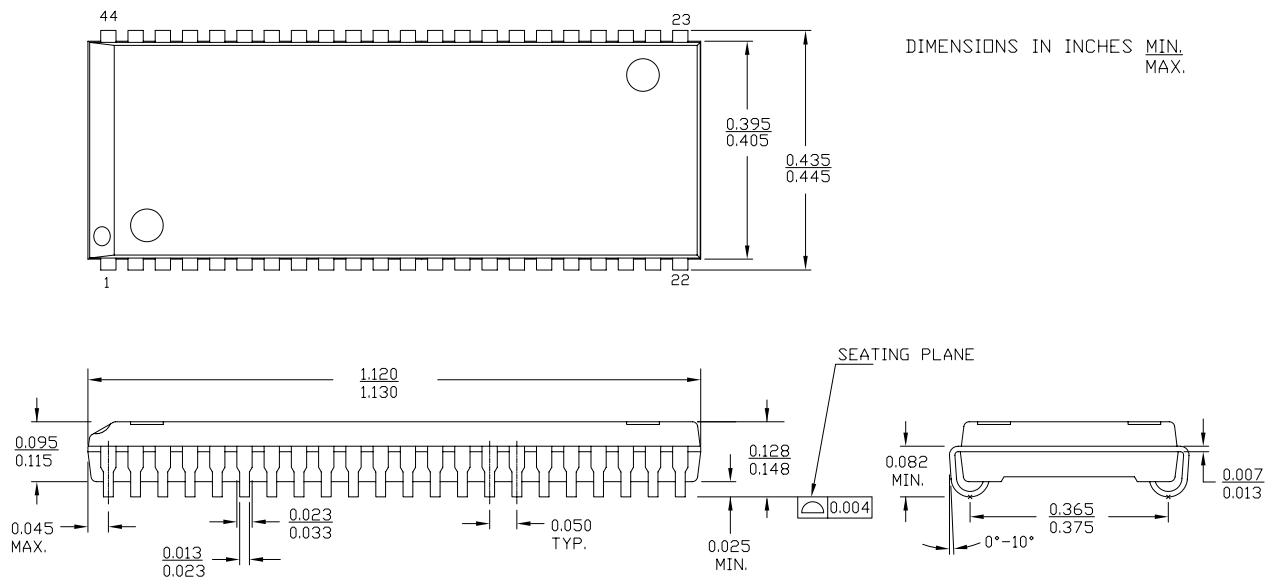
Package Diagrams

Figure 1. 48-ball FBGA (7 mm × 7 mm × 1.2 mm), 51-85096



51-85096 *1

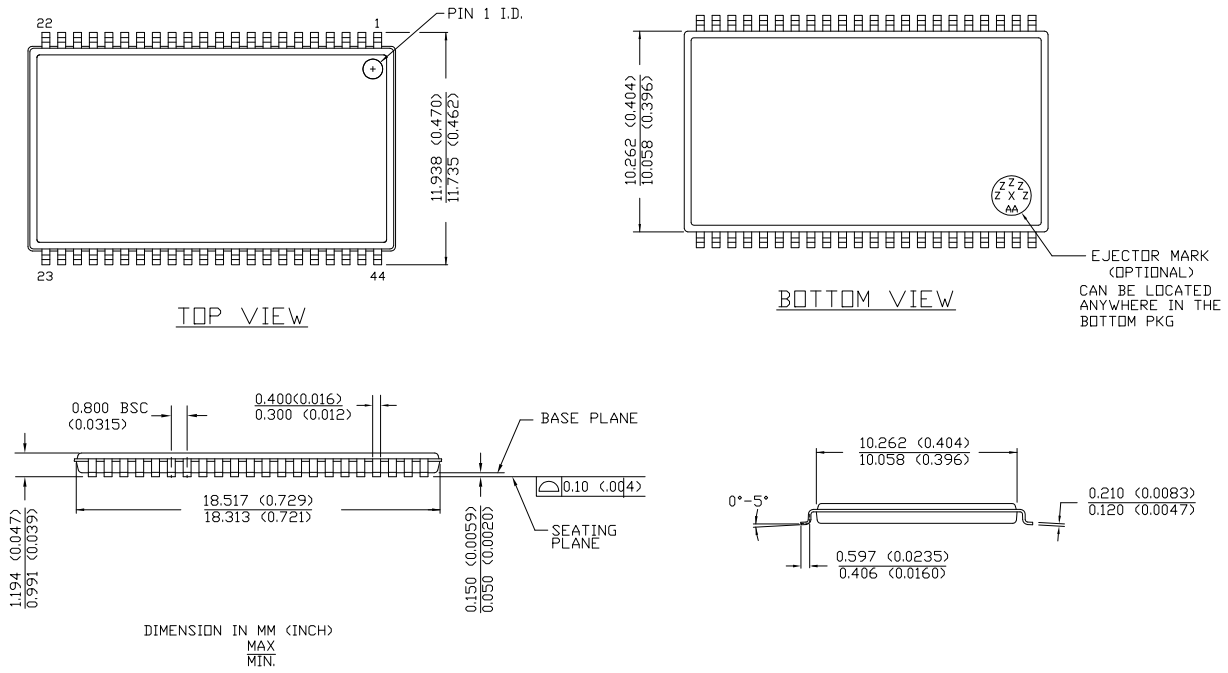
Figure 2. 44-pin (400-Mil) Molded SOJ, 51-85082



51-85082 *C

Package Diagrams(continued)

Figure 3. 44-pin TSOP Type II, 51-85087



51-85087 °C

Acronyms

| Acronym | Description |
|-----------------|-----------------------------------------|
| BGA | ball grid array |
| CMOS | complementary metal oxide semiconductor |
| \overline{CE} | chip enable |
| FBGA | Fine-Pitch Ball Grid Array |
| I/O | input/output |
| \overline{OE} | output enable |
| SOJ | small outline J-lead |
| SRAM | static random access memory |
| TTL | transistor-transistor logic |
| TSOP | thin small-outline package |
| \overline{WE} | write enable |

Document Conventions

Units of Measure

| Symbol | Unit of Measure |
|--------------|-----------------|
| ns | nano seconds |
| μ s | micro seconds |
| Ω | ohms |
| V | Volts |
| μ A | micro Amperes |
| mA | milli Amperes |
| mm | milli meter |
| MHz | Mega Hertz |
| pF | pico Farad |
| $^{\circ}$ C | degree Celcius |
| % | percent |
| mW | milli Watts |
| W | Watts |

Document History Page

| Document Title: CY7C1021BNV33 64 K × 16 Static RAM Document Number: 001-06433 | | | | |
|----------------------------------------------------------------------------------|---------|------------|-----------------|-------------------------------------------------------------------------------------------------------------------------------------------------|
| REV. | ECN NO. | Issue Date | Orig. of Change | Description of Change |
| ** | 423847 | See ECN | NXR | New Data Sheet |
| *A | 2897061 | 03/22/10 | AJU | Removed obsolete parts from ordering information table Updated package diagrams |
| *B | 3109897 | 12/14/2010 | AJU | Added Ordering Code Definitions |
| *C | 3103073 | 03/08/2011 | PRAS | Updated Package Diagrams . Added Acronyms and Units of Measure . Updated in new template. |

Sales, Solutions, and Legal Information

Worldwide Sales and Design Support

Cypress maintains a worldwide network of offices, solution centers, manufacturer's representatives, and distributors. To find the office closest to you, visit us at [Cypress Locations](#).

Products

| | |
|----------------------------------------------|--------------------------------------------------------------------------------------------------------------------------------------|
| Automotive | cypress.com/go/automotive |
| Clocks & Buffers | cypress.com/go/clocks |
| Interface | cypress.com/go/interface |
| Lighting & Power Control | cypress.com/go/powerpsoc cypress.com/go/plc |
| Memory | cypress.com/go/memory |
| Optical & Image Sensing | cypress.com/go/image |
| PSoC | cypress.com/go/psoc |
| Touch Sensing | cypress.com/go/touch |
| USB Controllers | cypress.com/go/USB |
| Wireless/RF | cypress.com/go/wireless |

PSoC Solutions

psoc.cypress.com/solutions
PSoC 1 | PSoC 3 | PSoC 5

© Cypress Semiconductor Corporation, 2006-2011. The information contained herein is subject to change without notice. Cypress Semiconductor Corporation assumes no responsibility for the use of any circuitry other than circuitry embodied in a Cypress product. Nor does it convey or imply any license under patent or other rights. Cypress products are not warranted nor intended to be used for medical, life support, life saving, critical control or safety applications, unless pursuant to an express written agreement with Cypress. Furthermore, Cypress does not authorize its products for use as critical components in life-support systems where a malfunction or failure may reasonably be expected to result in significant injury to the user. The inclusion of Cypress products in life-support systems application implies that the manufacturer assumes all risk of such use and in doing so indemnifies Cypress against all charges.

Any Source Code (software and/or firmware) is owned by Cypress Semiconductor Corporation (Cypress) and is protected by and subject to worldwide patent protection (United States and foreign), United States copyright laws and international treaty provisions. Cypress hereby grants to licensee a personal, non-exclusive, non-transferable license to copy, use, modify, create derivative works of, and compile the Cypress Source Code and derivative works for the sole purpose of creating custom software and or firmware in support of licensee product to be used only in conjunction with a Cypress integrated circuit as specified in the applicable agreement. Any reproduction, modification, translation, compilation, or representation of this Source Code except as specified above is prohibited without the express written permission of Cypress.

Disclaimer: CYPRESS MAKES NO WARRANTY OF ANY KIND, EXPRESS OR IMPLIED, WITH REGARD TO THIS MATERIAL, INCLUDING, BUT NOT LIMITED TO, THE IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS FOR A PARTICULAR PURPOSE. Cypress reserves the right to make changes without further notice to the materials described herein. Cypress does not assume any liability arising out of the application or use of any product or circuit described herein. Cypress does not authorize its products for use as critical components in life-support systems where a malfunction or failure may reasonably be expected to result in significant injury to the user. The inclusion of Cypress' product in a life-support systems application implies that the manufacturer assumes all risk of such use and in doing so indemnifies Cypress against all charges.

Use may be limited by and subject to the applicable Cypress software license agreement.