

August 1991

Features

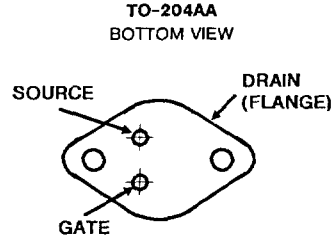
- 4.5A and 5.5A, 350V - 400V
- $r_{DS(on)} = 1.0\Omega$ and 1.5Ω
- SOA is Power-Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance
- Majority Carrier Device

Description

The 2N6759 and 2N6760 are n-channel enhancement-mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

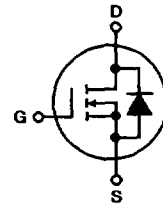
These types are supplied in the JEDEC TO-204AA steel package.

Package



Terminal Diagram

N-CHANNEL ENHANCEMENT MODE



Absolute Maximum Ratings ($T_C = +25^\circ\text{C}$), Unless Otherwise Specified

	2N6759	2N6760	UNITS
Drain-Source Voltage V_{DS}	350*	400*	V
Drain-Gate Voltage ($R_{GS} = 20k\Omega$) V_{DGR}	350*	400*	V
Continuous Drain Current			
$T_C = +25^\circ\text{C}$ I_D	4.5*	5.5*	A
$T_C = +100^\circ\text{C}$ I_D	3.0*	3.5*	A
Pulsed Drain Current I_{DM}	7.0	8.0	A
Gate-Source Voltage V_{GS}	± 20	± 20	V
Maximum Power Dissipation			
$T_C = +25^\circ\text{C}$ (See Figure 11) P_D	75*	75*	W
$T_C = +100^\circ\text{C}$ (See Figure 11) P_D	30*	30*	W
Linear Derating Factor (See Figure 11)	0.6*	0.6*	W/ $^\circ\text{C}$
Inductive Current, Clamped I_{LM}	7.0	8.0	A
(See Figures 1 and 2, $L = 100\mu\text{H}$)			
Operating and Storage Junction Temperature Range T_J, T_{STG}	-55 to +150*	-55 to +150*	$^\circ\text{C}$
Maximum Lead Temperature for Soldering T_L	300*	300*	$^\circ\text{C}$
(0.063" (1.6mm) from case for 10s)			

*JEDEC registered values

4
N-CHANNEL
POWER MOSFETS

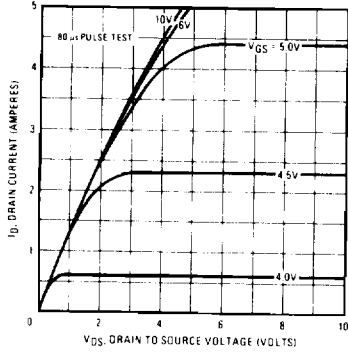


Fig. 5 - Typical Saturation Characteristics (2N6759)

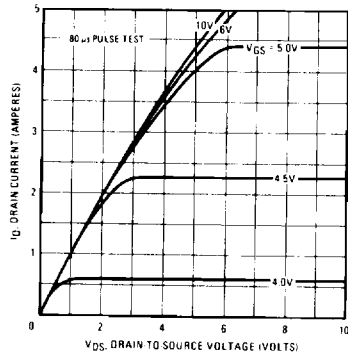


Fig. 6 - Typical Saturation Characteristics (2N6760)

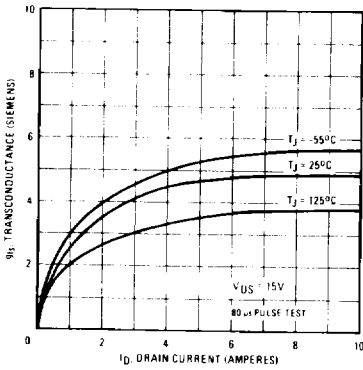


Fig. 7 - Typical Transconductance Vs. Drain Current

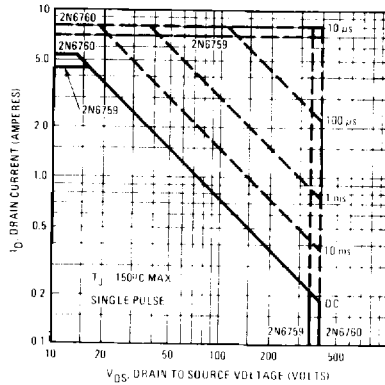


Fig. 8 - Maximum Safe Operating Area

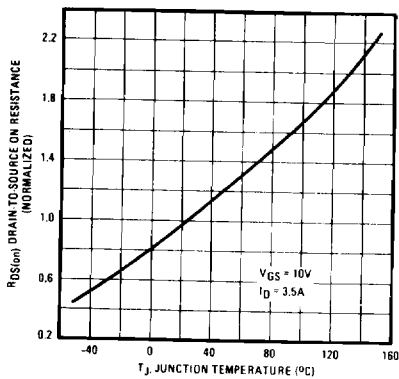


Fig. 9 - Normalized Typical On-Resistance Vs. Temperature

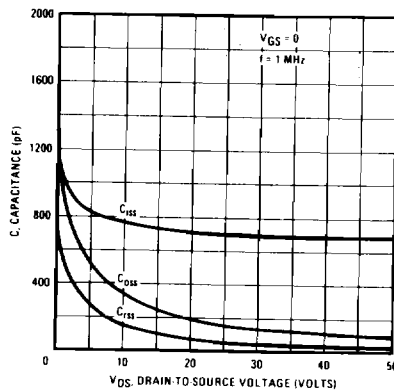


Fig. 10 - Typical Capacitance Vs. Drain-to-Source Voltage

2N6759, 2N6760

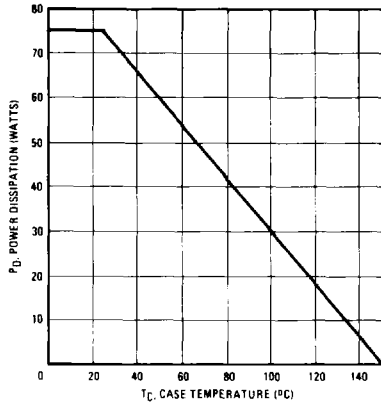


Fig. 11 - Power Vs. Temperature Derating Curve

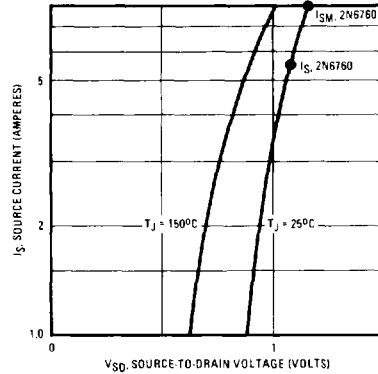


Fig. 12 - Typical Body-Drain Diode Forward Voltage

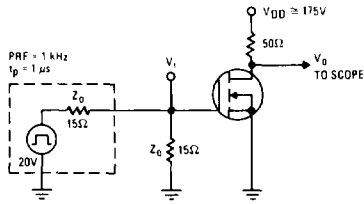


Fig. 13 - Switching Time Test Circuit

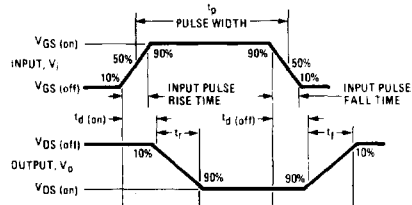


Fig. 14 - Switching Time Waveforms