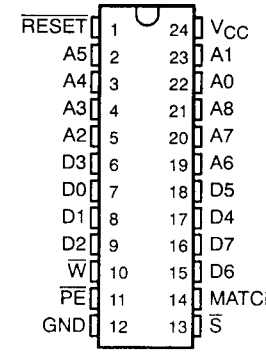
D3183, NOVEMBER 1988—REVISED MARCH 1990

- **Address to MATCH Valid Time**
  - **'ACT2150A 20 ns MAX**
  - **'ACT2150A 30 ns MAX**
- **300-Mil 24-Pin Ceramic Side-Brazed or Plastic Dual-In-Line or Small Outline Packages**
- **53 mA Typical Supply Current**
- **On-Chip Parity Generation and Checking**
- **Parity Error Output/Force Parity Error Input**
- **On-Chip Address/Data Comparator**
- **Asynchronous, Single-Cycle Reset**
- **Easily Expandable**
- **Fully Static**
- **Reliable Advanced CMOS Technology**
- **Fully TTL Compatible**

DW, JD, OR NT PACKAGE
(TOP VIEW)



description

This 8-bit-slice cache address comparator consists of a high-speed 512 × 9 static RAM array, parity generator, parity checker, and 9-bit high-speed comparator. It is fabricated using N-channel silicon gate technology for high speed and simple interface with MOS and bipolar TTL circuits. The cache address comparator is easily cascadable for wider tag addresses or deeper tag memories. Significant reductions in cache memory component count, board area, and power dissipation can be achieved with this device.

When $\overline{S}$ is low and $\overline{W}$ is high, the cache address comparator compares the contents of the memory location addressed by A0-A8 with the data on D0-D7 plus generated parity. An equality is indicated by the high level on the MATCH output. A low-level output from $\overline{PE}$ signifies a parity error in the internal RAM data. $\overline{PE}$ is an N-channel open-drain output for easy OR-tying. During a write cycle ($\overline{S}$ and $\overline{W}$ low), data on D0-D7 plus generated even parity are written in the 9-bit memory location addressed by A0-A8. Also during write, a parity error may be forced by holding $\overline{PE}$ low.

A $\overline{RESET}$ input is provided for initialization. When $\overline{RESET}$ goes low, all 512 × 9 RAM locations are cleared to zero (with valid parity) and the MATCH output is forced high. If an input word of zero is compared to any memory location that has not been written into since reset, MATCH will be high indicating that input data, plus generated parity, is equal to the reset memory location. $\overline{PE}$ will be high for every addressed memory location after reset indicating no parity error in the RAM data. By tying a single data input pin high, this bit will function as a valid bit and a match will not occur unless sata has been written into the addressed memeory location. When cascading in the width direction, only one bit needs to be tied high regardless of the address width.

The SN74ACT2150A operates from a single 5-V supply and is offered in a 24-pin 300-mil ceramic side-brazed or plastic dual-in-line packages and plastic "Small Outline" packages. The device is fully TTL compatible and is characterized for operation from 0°C to 70°C.

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MATCH OUTPUT DESCRIPTION

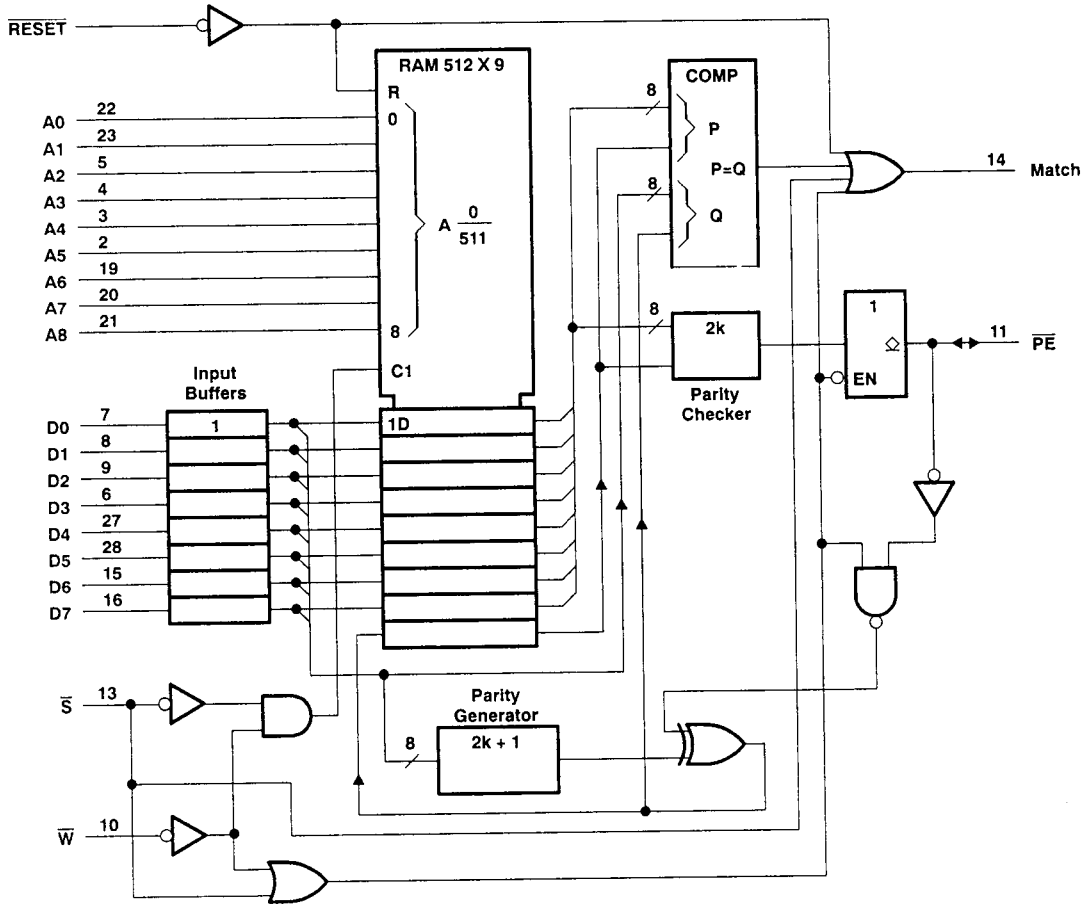
MATCH = V_{OH} if: [A0-A8] = D0-D7 + parity,
or: $\overline{RESET} = V_{IL}$,
or: $\overline{S} = V_{IH}$,
or: $\overline{W} = V_{IL}$

MATCH = V_{OL} if: [A0-A8] ≠ D0-D7 + parity,
with $\overline{RESET} = V_{IH}$,
$\overline{S} = V_{IL}$, and $\overline{W} = V_{IH}$

FUNCTION TABLE

OUTPUTS		FUNCTION DESCRIPTION
MATCH	$\overline{PE}$	
L	L	Parity Error
L	H	Not Equal
H	L	Undefined Error
H	H	Equal

logic diagram (positive logic)



for complete data sheet

The complete version of this data sheet and application information can be found in the *Cache Memory Management Data Book*, Literature #SCAD002. To obtain a copy of this data book, contact your local TI sales representative or call the TI Customer Response Center at 1-800-223-3200.