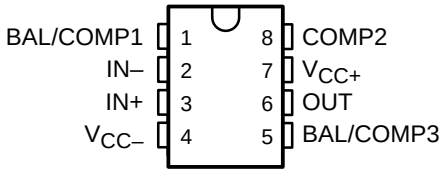
The LM118 and LM218 are obsolete and are no longer supplied.

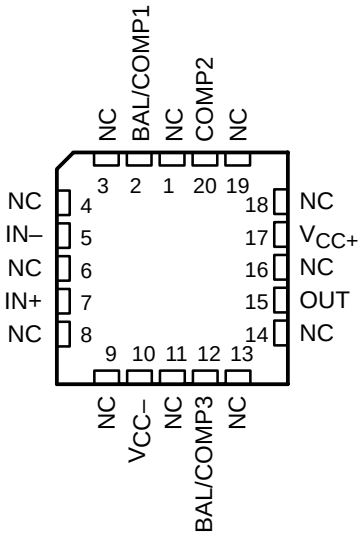
SLOS063B – JUNE 1976 – REVISED DECEMBER 2002

- **Small Signal Bandwidth . . . 15 MHz Typ**
- **Slew Rate . . . 50 V/μs Min**
- **Bias Current . . . 250 nA Max (LM118, LM218)**
- **Supply Voltage Range . . . ±5 V to ±20 V**
- **Internal Frequency Compensation**
- **Input and Output Overload Protection**
- **Same Pin Assignments as General-Purpose Operational Amplifiers**

LM118 . . . JG PACKAGE
LM218 . . . D OR P PACKAGE
LM318 . . . D, P, OR PS PACKAGE
(TOP VIEW)



LM118 . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

description/ordering information

The LM118, LM218, and LM318 are precision, fast operational amplifiers designed for applications requiring wide bandwidth and high slew rate. They feature a factor-of-ten increase in speed over general-purpose devices without sacrificing dc performance.

These operational amplifiers have internal unity-gain frequency compensation. This considerably simplifies their application because no external components are necessary for operation. However, unlike most internally compensated amplifiers, external frequency compensation may be added for optimum performance. For inverting applications, feed-forward compensation boosts the slew rate to over 150 V/μs and almost double the bandwidth. Overcompensation can be used with the amplifier for greater stability when maximum bandwidth is not needed. Further, a single capacitor can be added to reduce the settling time for 0.1% error band to under 1 μs.

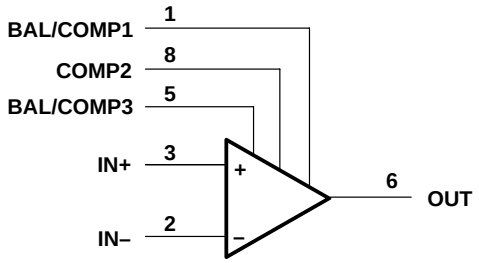
The high speed and fast settling time of these operational amplifiers make them useful in A/D converters, oscillators, active filters, sample-and-hold circuits, and general-purpose amplifiers.

ORDERING INFORMATION

T_A	V_{IO}max AT 25°C	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
0°C to 70°C	10 mV	PDIP (P)	Tube of 50	LM318P	LM318P
		SOIC (D)	Tube of 75	LM318D	LM318
			Reel of 2500	LM318DR	
		SOP (PS)	Reel of 2000	LM318PSR	LM18

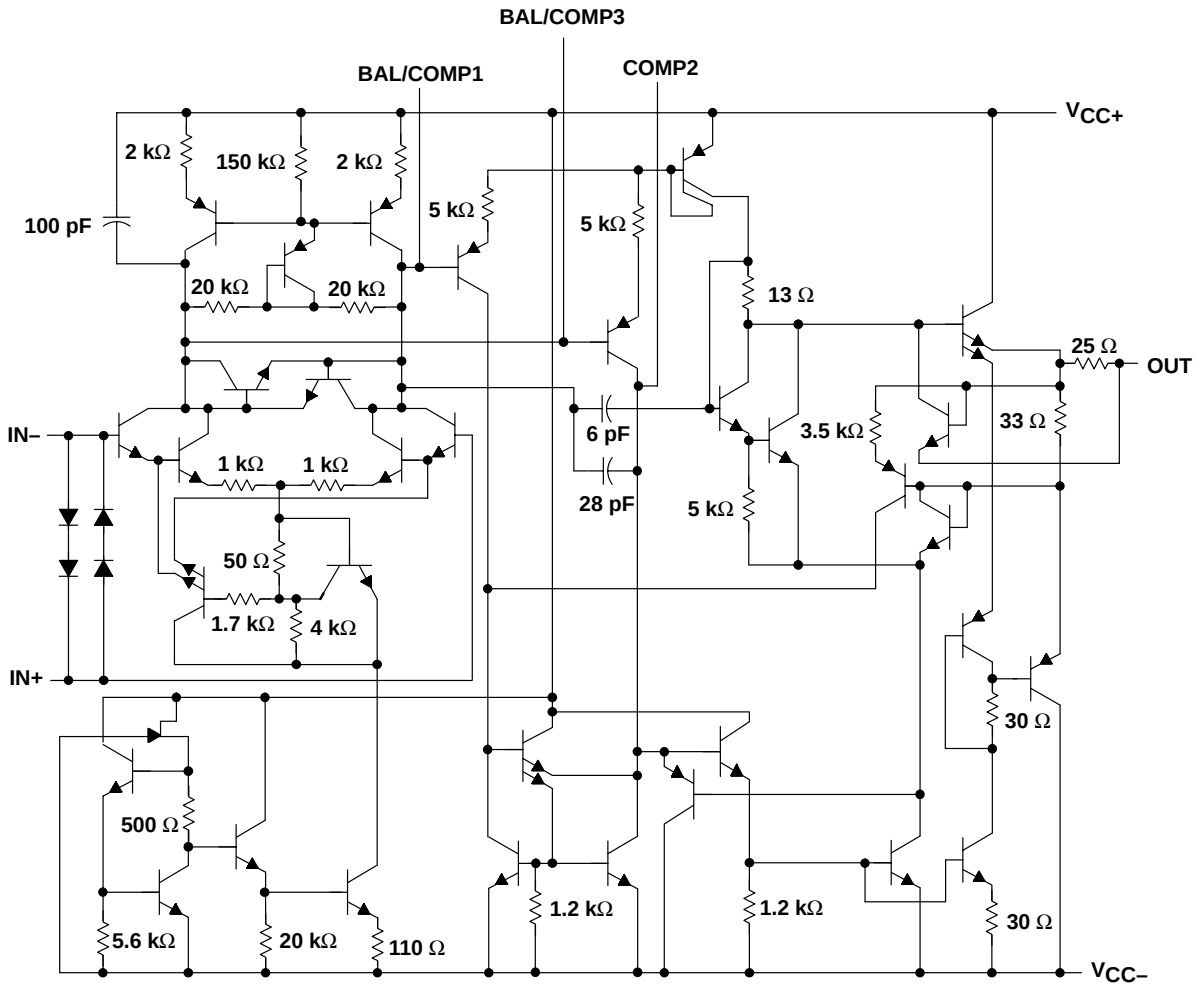
† Package drawings, standard packing quantities, thermal data, symboliztion, and PCB design guidelines are available at www.ti.com/sc/package.

symbol



Pin numbers shown are for the D, JG, P, and PS packages.

schematic



Component values shown are nominal.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage: V_{CC+} (see Note 1)	20 V
V_{CC-} (see Note 1)	–20 V
Input voltage, V_I (either input, see Notes 1 and 2)	±15 V
Differential input current, V_{ID} (see Note 3)	±10 V
Duration of output short circuit (see Note 4)	Unlimited
Operating virtual junction temperature, T_J	150°C
Package thermal impedance, θ_{JA} (see Notes 5 and 6): D package	97°C/W
P package	85°C/W
PS package	95°C/W
Package thermal impedance, θ_{JC} (see Notes 7 and 8): FK package	5.61°C/W
JG package	14.5°C/W
Case temperature for 60 seconds: FK package	260°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: JG package	300°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: D, P, PS, or PW package	260°C
Storage temperature range, T_{stg}	–65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES:
1. All voltage values, unless otherwise noted, are with respect to the midpoint between V_{CC+} and V_{CC-}.
2. The magnitude of the input voltage must never exceed the magnitude of the supply voltage or 15 V, whichever is less.
3. The inputs are shunted with two opposite-facing base-emitter diodes for overvoltage protection. Therefore, excessive current flows if a different input voltage in excess of approximately 1 V is applied between the inputs unless some limiting resistance is used.
4. The output can be shorted to ground or either power supply. For the LM118 and LM218 only, the unlimited duration of the short circuit applies at (or below) 85°C case temperature or 75°C free-air temperature.
5. Maximum power dissipation is a function of $T_J(max)$, θ_{JA}, and T_A. The maximum allowable power dissipation at any allowable ambient temperautre is $P_D = (T_J(max) – T_A)/\theta_{JA}$. Operating at the absolute maximum T_J of 150°C can affect reliability.
6. The package thermal impedance is calculated in accordance with JESD 51-7.
7. Maximum power dissipation is a function of $T_J(max)$, θ_{JC}, and T_C. The maximum allowable power dissipation at any allowable ambient temperautre is $P_D = (T_J(max) – T_C)/\theta_{JC}$. Operating at the absolute maximum T_J of 150°C can affect reliability.
8. The package thermal impedance is calculated in accordance with MIL-STD-883.

electrical characteristics at specified free-air temperature (see Note 5)

PARAMETER		TEST CONDITIONS†	T_A‡	LM118, LM218			LM318			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_O = 0	25°C		2	4		4	10	mV
			Full range			6			15	
I_{IO}	Input offset current	V_O = 0	25°C		6	50		30	200	nA
			Full range			100			300	
I_{IB}	Input bias current	V_O = 0	25°C		120	250		150	500	nA
			Full range			500			750	
V_{ICR}	Common-mode input voltage range	$V_{CC\pm}$ = ±15 V	Full range	±11.5			±11.5			V
V_{OM}	Maximum peak output voltage swing	$V_{CC\pm}$ = ±15 V, R_L = 2 kΩ	Full range	±12	±13		±12	±13		V
A_{VD}	Large-signal differential voltage amplification	$V_{CC\pm}$ = ±15 V, V_O = ±10 V, $R_L \geq$ 2 kΩ	25°C	50	200		25	200		V/mV
			Full range	25			20			
B_1	Unity-gain bandwidth	$V_{CC\pm}$ = ±15 V	25°C		15			15		MHz
r_i	Input resistance		25°C	1*	3		0.5	3		MΩ
CMRR	Common-mode rejection ratio	$V_{IC} = V_{ICR}$min	Full range	80	100		70	100		dB
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC}/\Delta V_{IO}$)		Full range	70	80		65	80		dB
I_{CC}	Supply current	V_O = 0, No load	25°C		5	8		5	10	mA

* On products compliant to MIL-STD-883, Class B, this parameter is not production tested.
† All characteristics are measured under open-loop conditions with common-mode input voltage, unless otherwise specified.
‡ Full range for LM118 is –55°C to 125°C, full range for LM218 is –25°C to 85°C, and full range for LM318 is 0°C to 70°C.
NOTE 9: Unless otherwise noted, V_{CC} = ±5 V to ±20 V. All typical values are at $V_{CC\pm}$ = ±15 V and T_A = 25°C.

operating characteristics, $V_{CC\pm}$ = ±15 V, T_A = 25°C

PARAMETER		TEST CONDITIONS			MIN	TYP	MAX	UNIT
SR	Slew rate at unity gain	ΔV_I = 10 V,	C_L = 100 pF,	See Figure 1	50*	70		V/μs

* On products compliant to MIL-STD-883, Class B, this parameter is not production tested.

PARAMETER MEASUREMENT INFORMATION

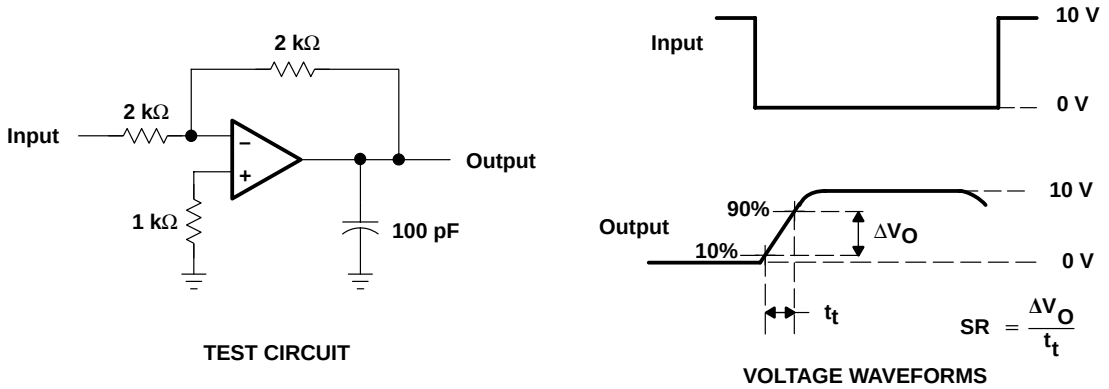


Figure 1. Slew Rate

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LM318D	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	0 to 70	LM318	Samples
LM318DR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	0 to 70	LM318	Samples
LM318DRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	0 to 70	LM318	Samples
LM318P	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	NIPDAU	N / A for Pkg Type	0 to 70	LM318P	Samples
LM318PE4	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	NIPDAU	N / A for Pkg Type	0 to 70	LM318P	Samples
LM318PSR	ACTIVE	SO	PS	8	2000	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	0 to 70	L318	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

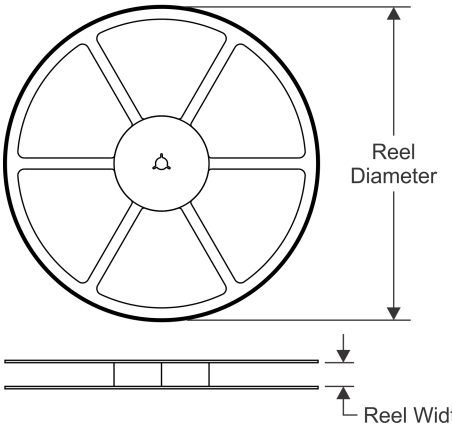
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

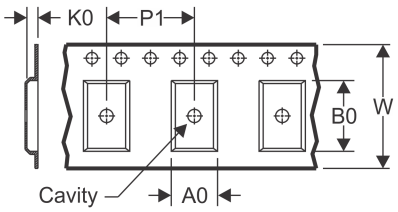
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

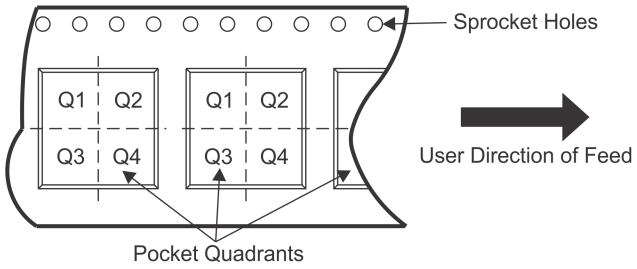


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

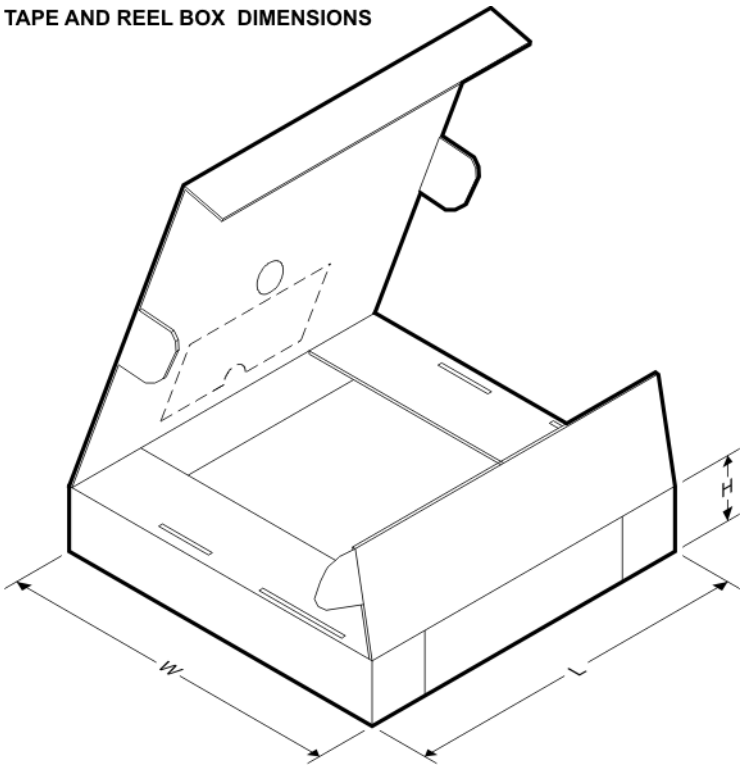
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

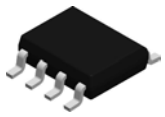
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM318DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM318DR	SOIC	D	8	2500	340.5	338.1	20.6

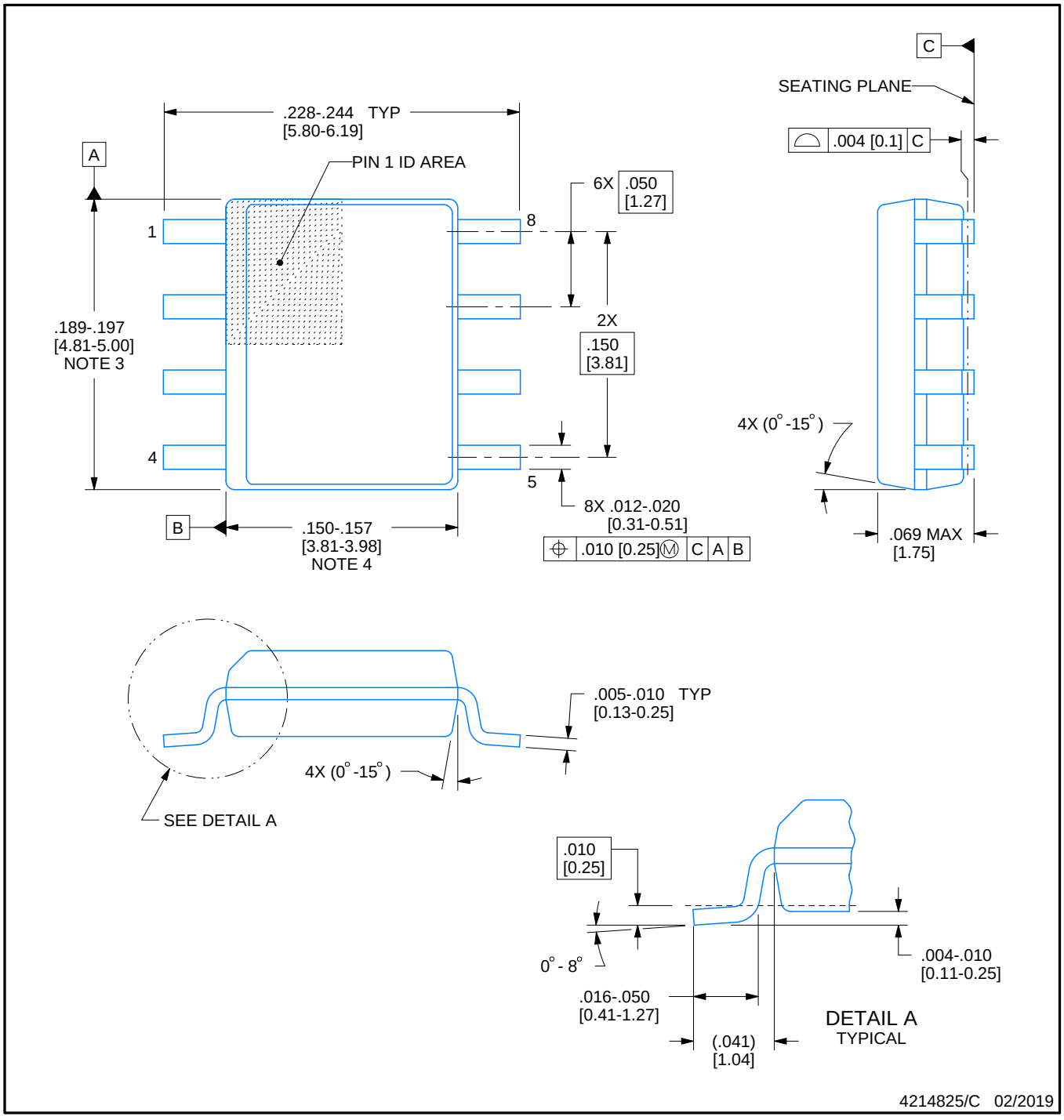


PACKAGE OUTLINE

D0008A

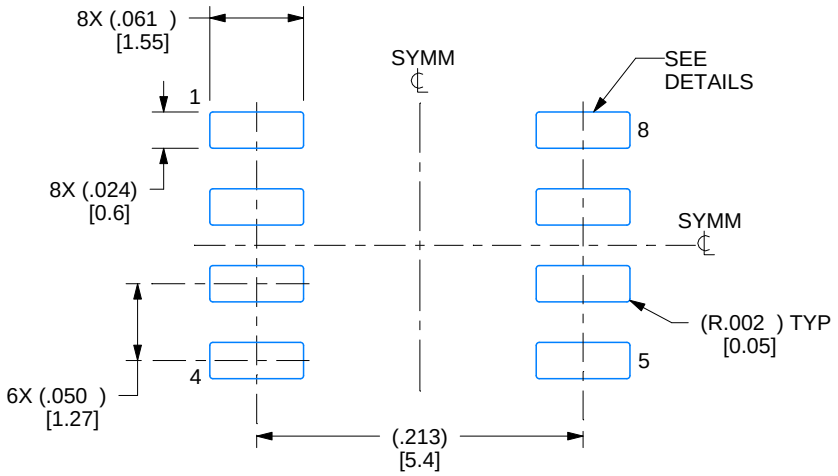
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

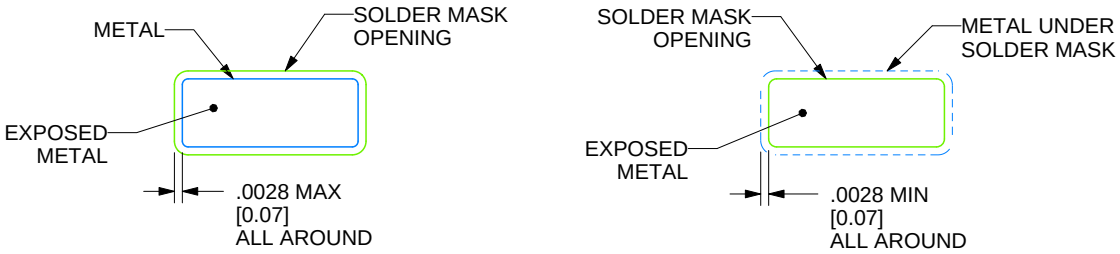


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

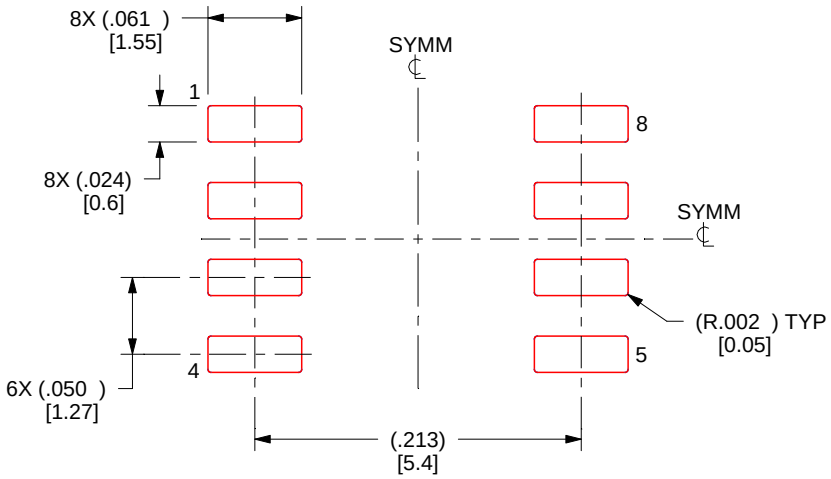
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

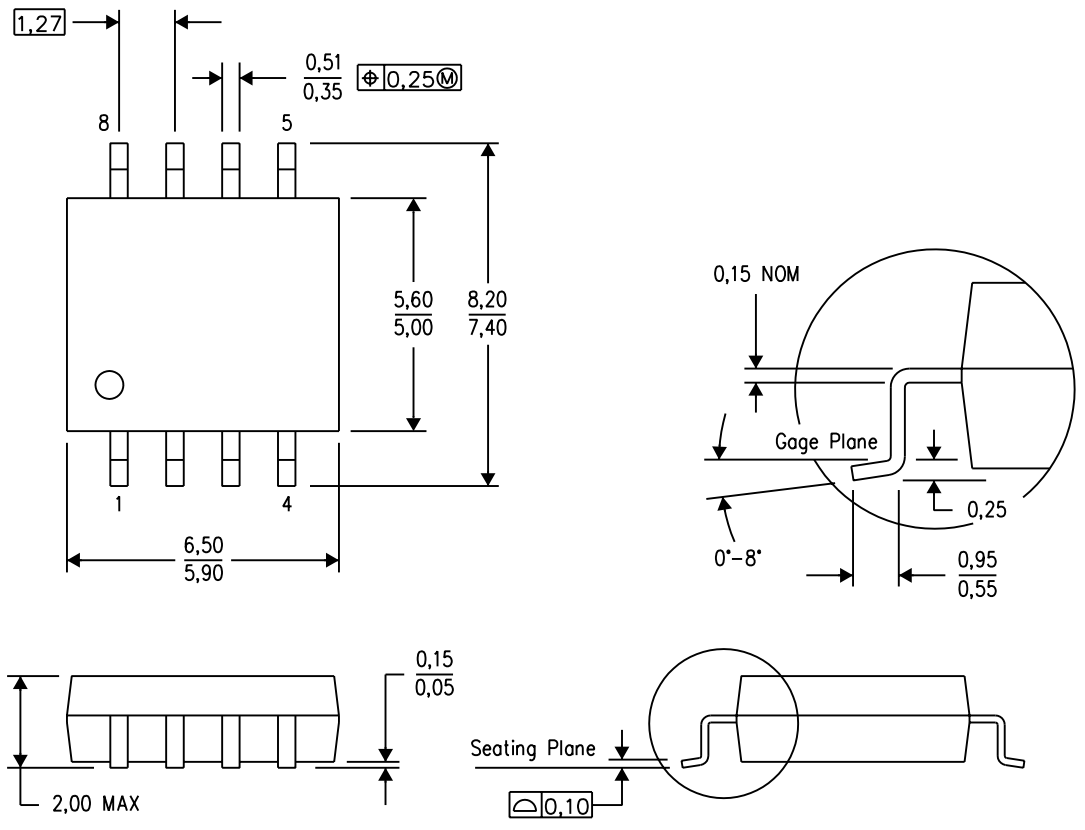
4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

MECHANICAL DATA

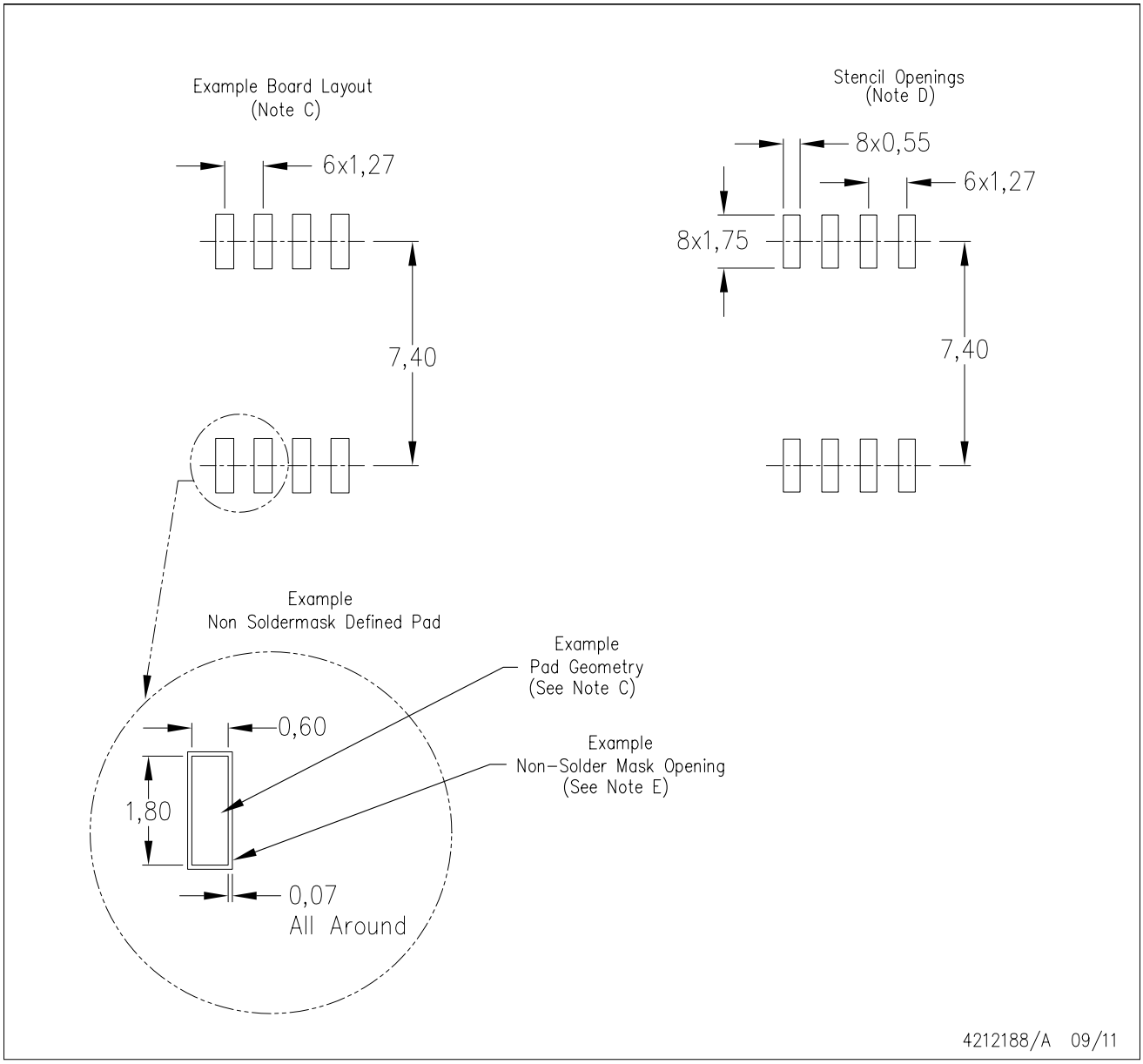
PS (R-PDSO-G8) **PLASTIC SMALL-OUTLINE PACKAGE**



4040063/C 03/03

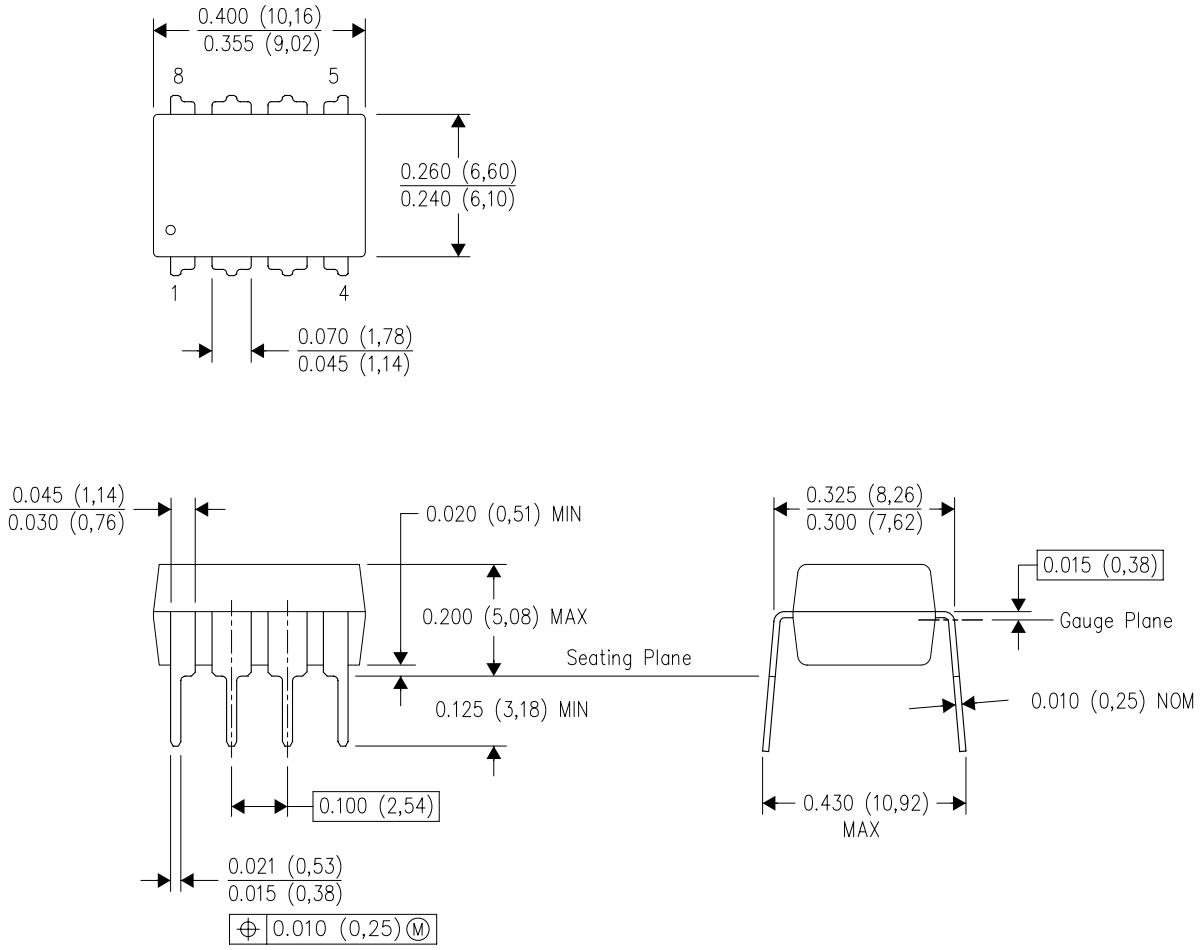
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

PS (R–PDSO–G8) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

P (R–PDIP–T8) PLASTIC DUAL–IN–LINE PACKAGE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001 variation BA.

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