HARRIS SEMICONDUCTOR

HSP43216

January 1997

Halfband Filter

Features

- Sample Rates to 52 MSPS
- Architected to Support Sample Rates to 104 MSPS Using External Multiplexer
- Four Modes of Operation:
  - Interpolate by 2 Filtering
  - Decimate by 2 Filtering
  - Quadrature to Real Signal Conversion
  - $F_S/4$ Quadrature Down Conversion Followed by Decimate by 2 Filtering
- 16-Bit Inputs and Outputs
- 67-Tap Halfband FIR Filter with 20-Bit Coefficients
- Two's Complement or Offset Binary Outputs
- Programmable Rounding on Outputs
- 1.24:1 FIlter Shape Factor
- >90dB Stopband Attenuation
- <0.0003dB Passband Ripple
- Saturation Logic on Output

Applications

- Digital Down Conversion
- D/A and A/D pre/post Filtering
- Tuning Bandwidth Expansion for HSP45116 and HSP45106

Description

The HSP43216 Halfband Filter addresses a wide variety of applications by combining $F_S/4$ (F_S = sample frequency) quadrature up/down convert circuitry with a fixed coefficient halfband filter processor as shown in the block diagram. These elements may be configured to operate in one of the four following modes: decimate by 2 filtering of a real input signal; interpolate by 2 filtering of a real input signal; $F_S/4$ quadrature down conversion of a real input signal followed by decimate-by-2 filtering to produce a complex analytic signal; interpolate-by-2 filtering of a complex analytic signal followed by $F_S/4$ quadrature up conversion to produce a real valued output.

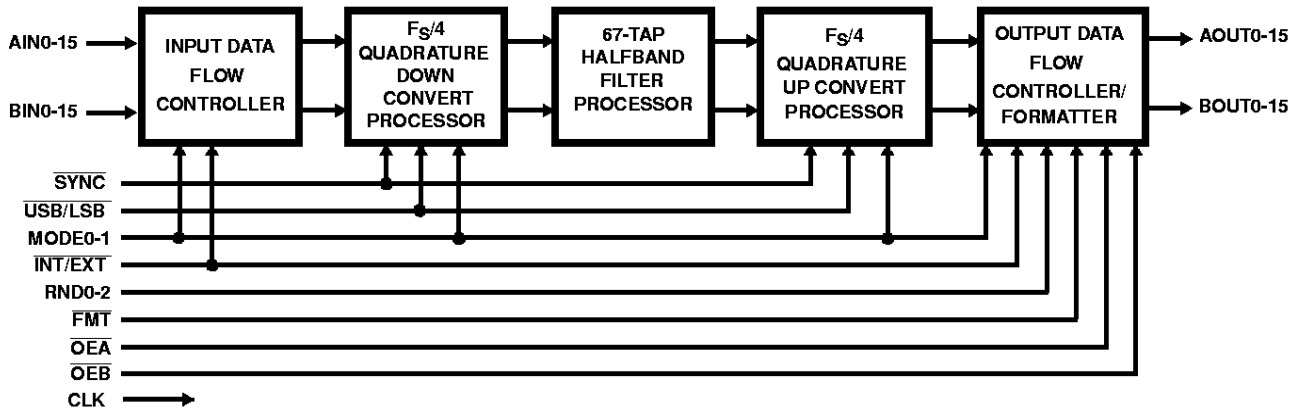
The frequency response of the HSP43216's halfband filter has a shape factor, (passband+transition band)/passband, of 1.24:1 with 90dB of stopband attenuation. The passband has less than 0.0003dB of ripple from $0F_S$ to $0.2F_S$ with stopband attenuation of greater than 90dB from $0.3F_S$ to Nyquist. At $0.25F_S$ the filter provides 6dB of attenuation.

The HSP43216 processes data streams with word widths up to 16 bits and data rates up to 52 MSPS. The processing throughput of the part is easily doubled to rates of up to 104 MSPS by using the part together with an external multiplexer or demultiplexer. Programmable rounding is provided to support output precisions from 8 bits to 16 bits.

Ordering Information

PART NUMBER	TEMP. RANGE (^oC)	PACKAGE TYPE	PKG. NO.
HSP43216GC-52	0 to 70	85 Ld CPGA	G85.A
HSP43216JC-52	0 to 70	84 Ld PLCC	N84.1.15
HSP43216VC-52	0 to 70	100 Ld MQFP	Q100.14x20
HSP43216JI-52	-40 to 85	84 Ld PLCC	N84.1.15

Block Diagram

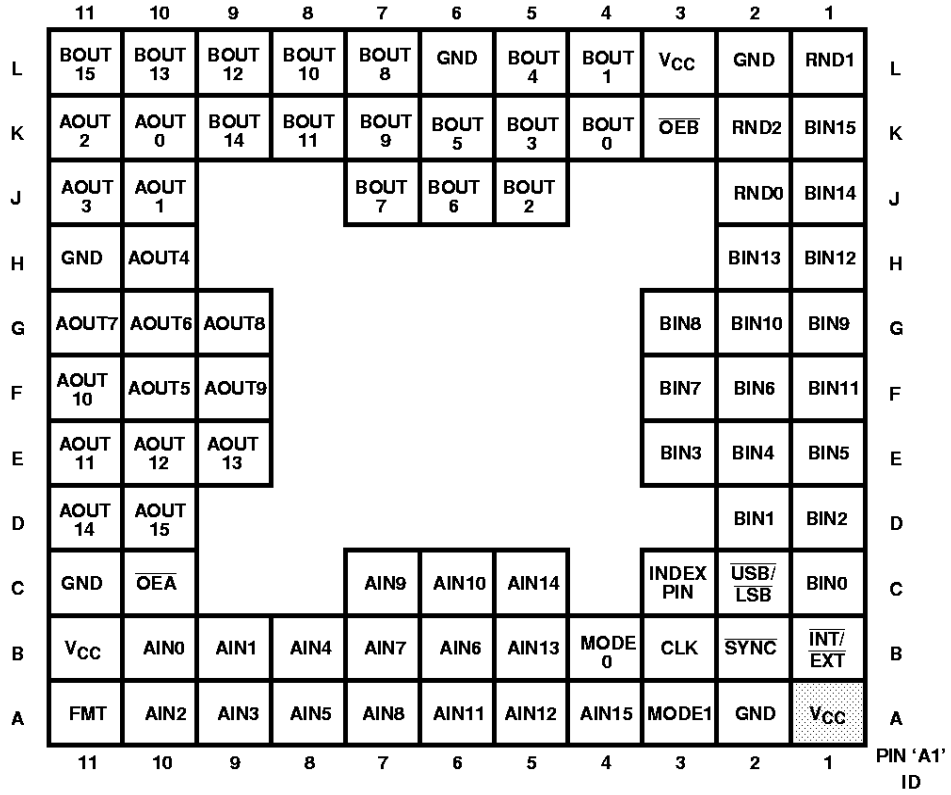


CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.

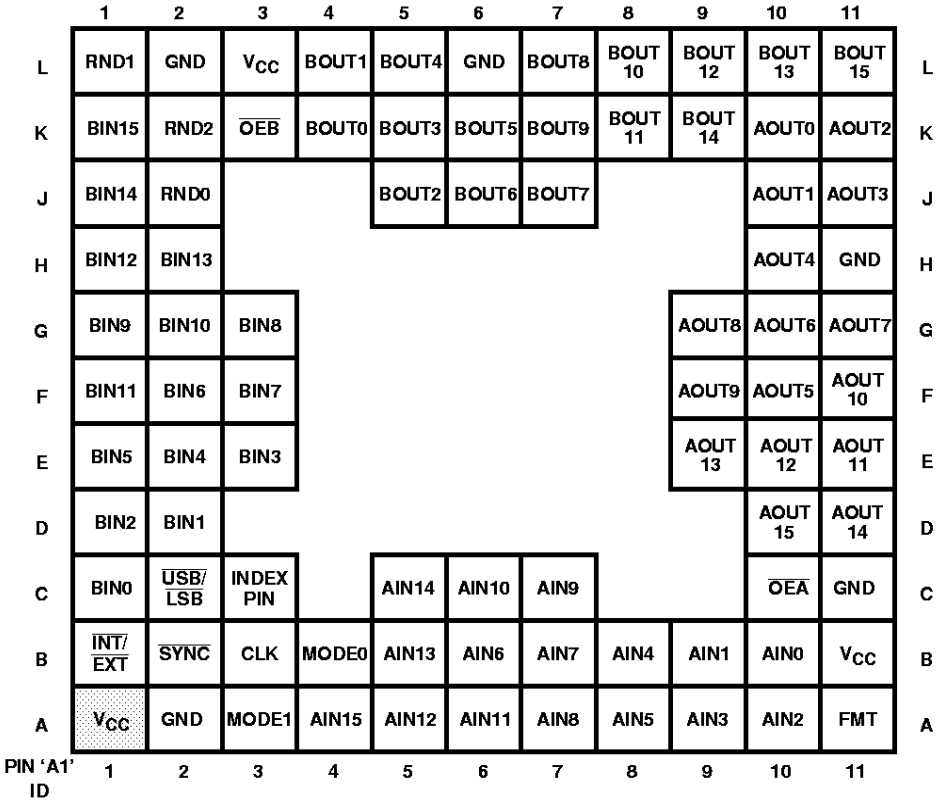
File Number **3365.6**

Pinouts

85 PIN PGA
TOP VIEW

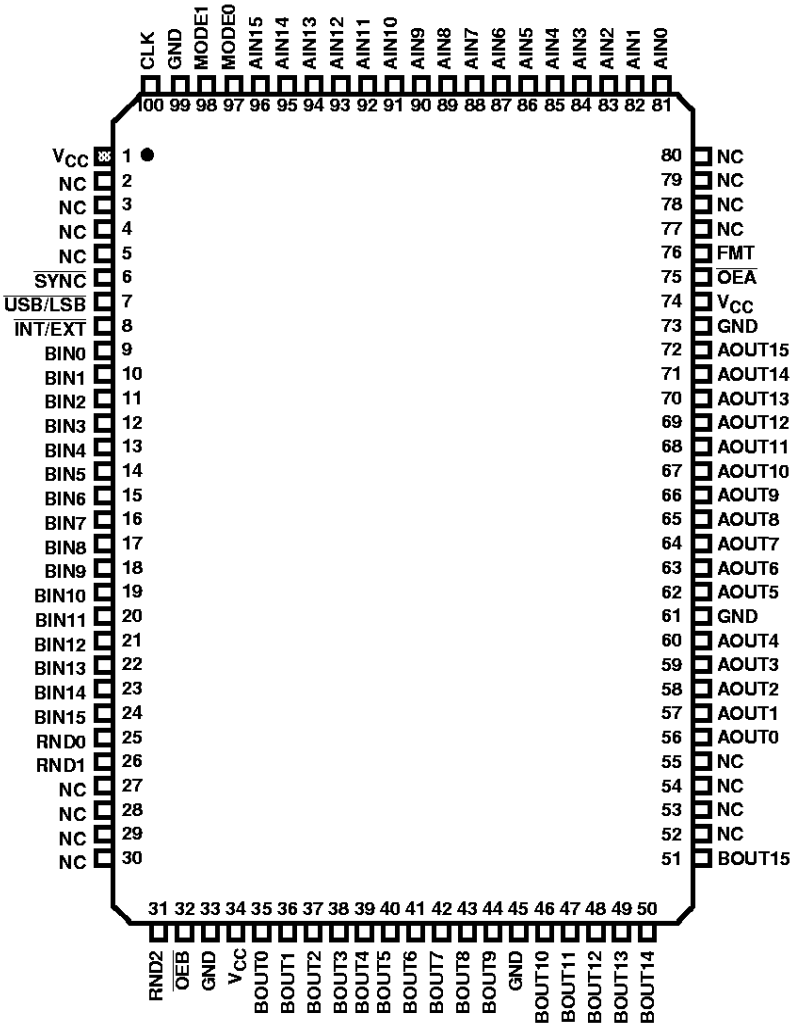


85 PIN PGA
BOTTOM VIEW



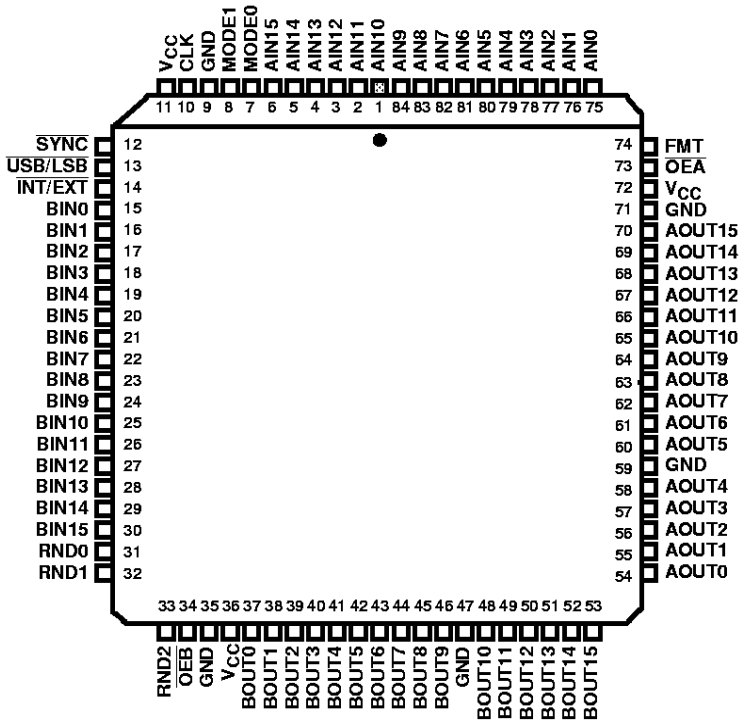
Pinouts (Continued)

100 LEAD MQFP
TOP VIEW



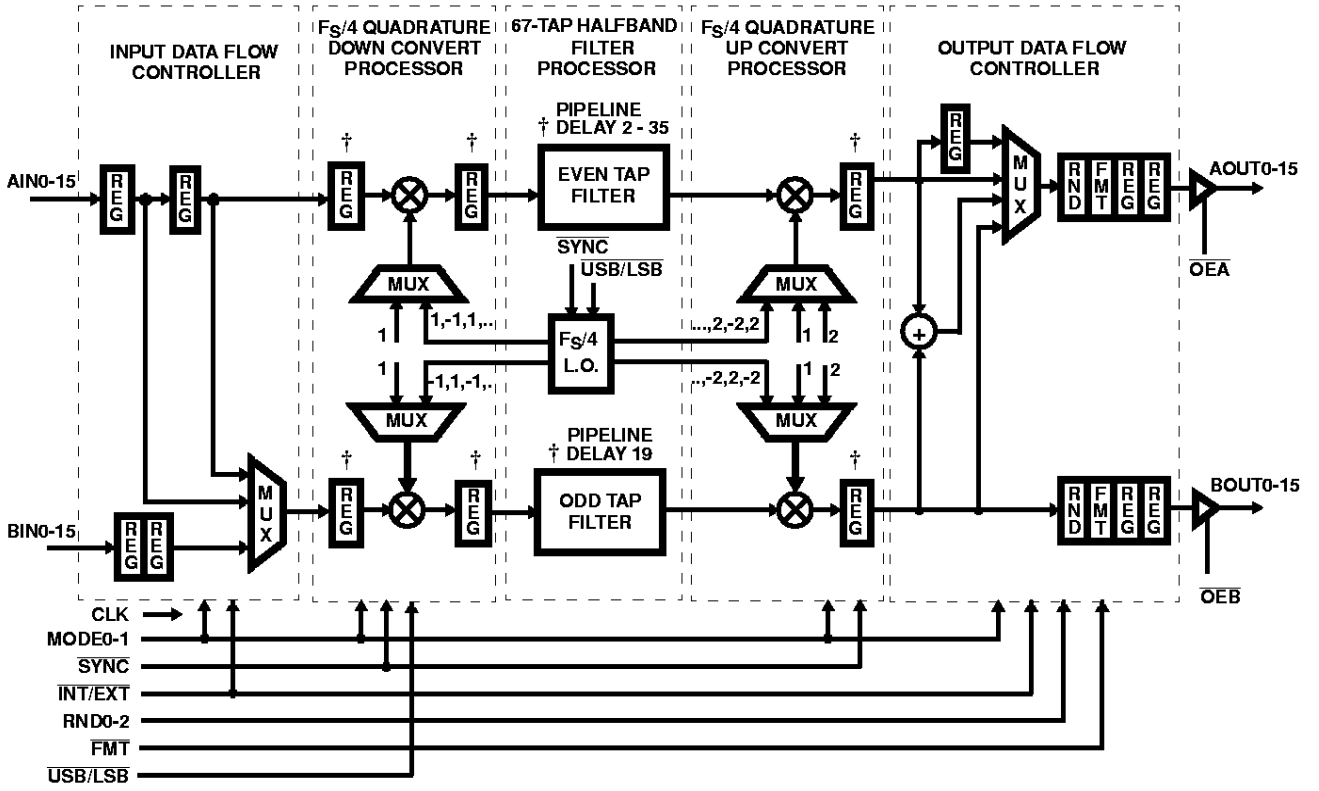
Pinouts (Continued)

84 LEAD PLCC
TOP VIEW



Pin Description

NAME	TYPE	DESCRIPTION
V_{CC}	-	+5V Power
GND	-	Ground
CLK	I	Clock Input. (CMOS LEVEL)
AIN0-15	I	Input Data Bus A. AIN0 is the LSB. Input data format is 16-bit Two's Complement.
BIN0-15	I	Input Data Bus B. BIN0 is the LSB. Input data format is 16-bit Two's Complement.
MODE0-1	I	The Mode Select Inputs set one of four operational modes as highlighted in Table 1.
$\overline{INT}$/EXT	I	The Internal\External multiplexer select inputs set whether the data multiplex/demultiplex function required in the various operational modes is performed internally (High State) or externally to the chip (Low State).
$\overline{SYNC}$	I	This input is used to synchronize the input sample stream with the zero degree phase of the up or down convert Local Oscillators. In the straight decimate modes, this input can be use to synchronize the input sample stream with a particular phase of the halfband filter. (See the Operational Modes Section for additional information)
$\overline{USB}$/LSB	I	The Upper and Lower Sideband select line is used to specify the direction of frequency translation imparted on the data stream in the Down Convert and Decimate Mode and in the Quadrature to Real Convert Mode. (See Operational Modes Section for additional information)
RND0-2	I	The Round Select inputs set the number of output bits from eight (RND = 000) to sixteen (RND = 110). Least significant output bits are zeroed. See Table 4.
$\overline{OEA}$	I	Three-State Control Output Bus A, OUTA0-15. Active Low.
$\overline{OEB}$	I	Three-State Control Output Bus B, OUTB0-15. Active Low.
$\overline{FMT}$	I	The Format select input is used to convert the two's complement output to offset binary (unsigned). When asserted high, the AOUT15 and BOUT15 bits are inverted from the normal two's complement representation.
AOUT0-15	O	Output Bus A. AOUT0 is the LSB.
BOUT0-15	O	Output Bus B. BOUT0 is the LSB.



† Indicates elements which operate at CLK/2 when the $\overline{\text{INT/EXT}}$ control input is high.

FIGURE 1. HALFBAND BLOCK DIAGRAM

Functional Description

The operation of the HSP43216 centers around a fixed coefficient, 67-Tap, Halfband Filter Processor as shown in Figure 1. The Halfband Filter Processor operates stand alone to provide two fundamental modes of operation: interpolate or decimate by two filtering of a real signal. In two other modes, the Quadrature Up/Down Convert circuitry operates together with the Filter Processor block to provide $F_S/4$ Down Conversion with decimate by 2 filtering or Quadrature to Real Conversion.

In Down Convert and Decimate mode, a real input sample stream is spectrally shifted by $F_S/4$. Each component of the resulting complex signal is then halfband filtered and decimated by 2 to produce real and imaginary output samples at half of the input data rate.

In Quadrature to Real Conversion mode, the real and imaginary components of a quadrature input are interpolated by two and halfband filtered. The filtered result is then spectrally shifted by $F_S/4$ and the real component of this operation is output at twice the input sample rate.The HSP43216 is configured for different operational modes by setting the state of the mode control pins, MODE1-0 as shown in Table 1.

TABLE 1. MODE SELECT TABLE

MODE1-0	MODE
00	Decimate by Two
01	Interpolate by Two
10	Down Convert and Decimate
11	Quadrature to Real Conversion

Input Data Flow Controller

The Input Data Flow Controller routes data samples from the AIN0-15 and BIN0-15 inputs to the internal processing elements of the Halfband. The data routing paths are based on mode of operation and are more fully discussed in the Operational Modes section.

$F_S/4$ Quadrature Down Convert Processor

The $F_S/4$ Quadrature Down Convert Processor operates as a Quadrature LO which provides the negative $F_S/4$ spectral shift required to center the upper sideband of a real input signal at DC. This operation is equivalent to multiplying the

real sample stream, x(n), by the quadrature components of the complex exponential $e^{-j(\pi/2)n}$ as given below:

$$x(n)e^{-j(\pi n/2)} = x(n)\cos(\pi n/2) + jx(n)\sin(-\pi n/2) \quad \text{(EQ. 1)}$$

For added flexibility, a spectrally reversed version of the above process may be realized by configuring the Down Convert processor to impart a positive $F_S/4$ spectral shift on the input signal. This has the effect of centering the lower sideband of the input signal at DC and is achieved by reversing the sign of the sine term in the quadrature mix as shown below:

$$x(n)e^{j(\pi n/2)} = x(n)\cos(\pi n/2) + jx(n)\sin(\pi n/2) \quad \text{(EQ. 2)}$$

The direction of the spectral shift imparted by the Down Convert Processor is set by the Upper Sideband/ Lower Sideband control input, $\overline{USB}/LSB$. When this input is high, a $-F_S/4$ spectral shift is used to center the input signal's upper sideband at DC. When asserted low, a spectral shift of $F_S/4$ is used to center the lower sideband at DC. The $\overline{SYNC}$ control input may be used to synchronize the incoming data stream with the zero degree phase of the complex exponential as described in the Operational Modes section.

The real and imaginary sample streams generated by the down convert operation are passed to the Halfband Filter block on the upper and lower processing legs respectively.

The Down Convert Processor is only active in Down Convert and Decimate Mode, MODE1-0 = 10. In the other modes, the data on the upper and lower processing legs pass unaltered.

67-Tap Halfband Filter Processor

The processing required to implement the 67-Tap Halfband filter is distributed across two polyphase branches comprised of even and odd tap filters as shown in Figure 1. The Even Tap Filter performs a filtering operation using the even indexed coefficients (even phase) of the halfband filter. The Odd Tap Filter uses the odd indexed coefficients (odd phase) of the halfband filter. ***NOTE: the odd tap filter's processing reduces to a delay and scale operation since the center tap is the only non-zero odd tap for a halfband filter.*** Together the polyphase filters perform the sum of-products required to implement the 67-tap halfband filter in an architecture capable of supporting a variety of operational modes. The frequency response of the halfband filter is given graphically in Figure 2 and in tabular form in Table 3. Table 2 shows the different modes and the related frequency with which the spectra in Figure 2 is normalized.

TABLE 2. NORMALIZED FREQRUENCY vs MODE

MODE	F_S
Decimate by Two	CLK
Interpolate by Two	CLK/2
Down Convert and Decimate	CLK
Quadrature to Real	CLK/2

The polyphase implementation of the halfband filter provides the flexibility to realize a variety of filter configurations. In Decimate by Two Mode, the outputs of the each polyphase branch are summed to yield the filter output. In Interpolate by Two mode, the polyphase filters produce independent outputs which are multiplexed into a single sample stream at the interpolated data rate. In the Up Convert and Down Convert Modes, the polyphase branches filter the real and imaginary components of a complex sample stream with the equivalent of identical 67-Tap Halfband Filters. For these modes, the real component is processed by the Even Tap filter and the imaginary component is processed by the Odd Tap filter. The Operational Modes Section provides further details regarding the data flow and operation of the Filter Processor for the various modes.

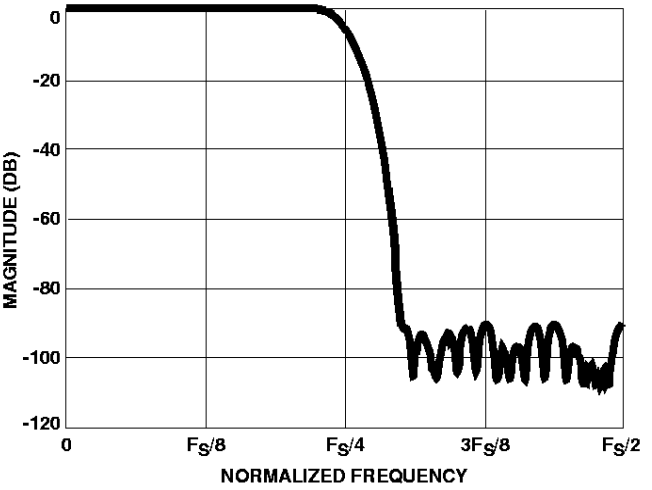


FIGURE 2. FREQUENCY RESPONSE OF 67-TAP HALFBAND FILTER

As a standard DSP term, group delay is defined as the time it takes to obtain valid filtered data given a certain input pattern. Both the Even Tap and Odd Tap filters have an identical group delay of 19 clocks relative to the operating mode of the halfband. The group delay has been specified in the data flow diagrams following this section. The delay clocks equal CLK when $\overline{INT}/EXT$ = 0 and CLK/2 when $\overline{INT}/EXT$ = 1.

NOTE: Pipeline delay specifies the time it takes for bits to toggle at the output given a certain input pattern. The Odd tap filter has a pipeline delay of 19 CLKs with respect to the operating mode because it consists of only the center tap of the 67-tap halfband. The Even tap filter has a pipeline delay of 2-35 CLKs with respect to the operating mode.

$F_S/4$ Quadrature Up Convert Processor

The $F_S/4$ Quadrature Up Convert Processor provides the $F_S/4$ spectral shift used to construct a real signal from a complex sample stream. The operation performed is equivalent to multiplying a quadrature data stream, i(n)+jq(n), by samples of a complex exponential, $e^{-j(\pi/2)n}$,

TABLE 3. FREQUENCY RESPONSE OF THE 67-TAP HALFBAND FILTER NORMALIZED TO THE MODE SPECIFIC SAMPLE RATE

FREQUENCY (NORMALIZED)	MAGNITUDE (dB)	FREQUENCY (NORMALIZED)	MAGNITUDE (dB)	FREQUENCY (NORMALIZED)	MAGNITUDE (dB)	FREQUENCY (NORMALIZED)	MAGNITUDE (dB)
0.000000	-0.000256	0.125000	-0.000278	0.250000	-6.020594	0.375000	-90.469534
0.003906	-0.000143	0.128906	-0.000098	0.253906	-7.989334	0.378906	-91.528735
0.007812	-0.000071	0.132812	0.000001	0.257812	-10.364986	0.382812	-98.960202
0.011719	-0.000013	0.136719	0.000077	0.261719	-13.194719	0.386719	-105.235066
0.015625	-0.000004	0.140625	0.000166	0.265625	-16.533196	0.390625	-97.073218
0.019531	-0.000001	0.144531	0.000106	0.269531	-20.447622	0.394531	-101.790858
0.023438	0.000032	0.148438	0.000015	0.273438	-25.024382	0.398438	-103.660592
0.027344	-0.000000	0.152344	-0.000022	0.277344	-30.379687	0.402344	-96.903272
0.031250	-0.000026	0.156250	-0.000048	0.281250	-36.679477	0.406250	-97.160860
0.035156	0.000002	0.160156	-0.000074	0.285156	-44.169450	0.410156	-106.804655
0.039062	0.000036	0.164062	-0.000022	0.289062	-53.259353	0.414062	-96.213761
0.042969	0.000050	0.167969	0.000005	0.292969	-64.619008	0.417969	-91.368358
0.046875	0.000021	0.171875	0.000009	0.296875	-79.291213	0.421875	-91.202963
0.050781	0.000008	0.175781	0.000041	0.300781	-90.247748	0.425781	-96.903271
0.054688	-0.000012	0.179688	0.000095	0.304688	-91.540418	0.429688	-103.058722
0.058594	-0.000140	0.183594	0.000090	0.308594	-96.987389	0.433594	-92.156508
0.062500	-0.000226	0.187500	-0.000012	0.312500	-97.990997	0.437500	-90.247741
0.066406	-0.000138	0.191406	-0.000037	0.316406	-94.450644	0.441406	-91.623161
0.070312	0.000010	0.195312	-0.000145	0.320312	-94.268681	0.445312	-98.760392
0.074219	0.000036	0.199219	-0.000208	0.324219	-97.250387	0.449219	-103.883238
0.078125	0.000179	0.203125	-0.000927	0.328125	-103.660592	0.453125	-96.861830
0.082031	0.000190	0.207031	-0.005089	0.332031	-105.940671	0.457031	-96.987388
0.085938	0.000064	0.210938	-0.018871	0.335938	-98.212931	0.460938	-100.046559
0.089844	0.000011	0.214844	-0.053894	0.339844	-94.313447	0.464844	-106.804655
0.093750	-0.000064	0.218750	-0.128250	0.343750	-95.354251	0.468750	-104.119091
0.097656	-0.000018	0.222656	-0.266964	0.347656	-98.447393	0.472656	-105.235066
0.101562	-0.000000	0.226562	-0.501238	0.351562	-103.249457	0.476562	-104.637666
0.105469	0.000020	0.230469	-0.866791	0.355469	-93.387604	0.480469	-105.940673
0.109375	0.000053	0.234375	-1.401949	0.359375	-91.390894	0.484375	-107.323099
0.113281	0.000012	0.238281	-2.145948	0.363281	-94.404415	0.488281	-102.375213
0.117188	-0.000022	0.242188	-3.137997	0.367188	-103.883234	0.492188	-94.009640
0.121094	-0.000149	0.246094	-4.416657	0.371094	-93.245384	0.496094	-91.312516

and outputting the real part of that mathematical operation as given below:

$$\text{Real}\{(i(n) + jq(n))\, e^{j(\pi n/2)}\}$$
$$= \text{Real}\{[i(n)\cos(\pi n/2) - q(n)\sin(\pi n/2)] + j[i(n)\sin(\pi n/2) + q(n)\cos(\pi n/2)]\}$$
$$= i(n)\cos(\pi n/2) - q(n)\sin(\pi n/2)$$
$$= i(n)\cos(\pi n/2) + q(n)\sin(-\pi n/2) \quad \text{(EQ. 3)}$$

In the above operation, a positive $F_S/4$ spectral shift is imparted on the quadrature input which causes the upper sideband of the resulting real output to be defined by the spectral content of the input signal as shown in Figure 3. For added flexibility, the Up Convert processor may be configured to impart a negative $F_S/4$ shift on the quadrature input which generates a real output whose lower sideband is defined the spectrum of the quadrature input as shown in Figure 4. The state of the $\overline{\text{USB/LSB}}$ control input determines the direction of the spectral shift. If this input is set "High", a positive $F_S/4$ shift is introduced by the Up Convert Processor. If $\overline{\text{USB/LSB}}$ is asserted "Low", a negative $F_S/4$ spectral shift is introduced.

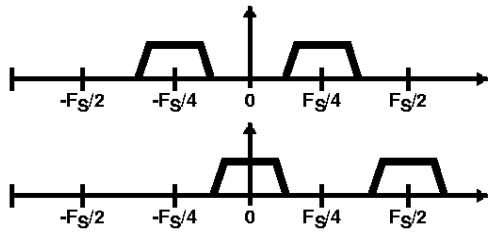


FIGURE 3. $F_S/4$ POSITIVE SHIFT: UP CONVERSION

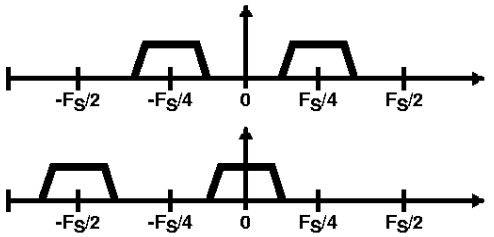


FIGURE 4. $F_S/4$ NEGATIVE SHIFT: DOWN CONVERSION

The Up Convert Processor implements the up convert operation by multiplying the in-phase and quadrature samples on the upper and lower processing legs by the nonzero sine and cosine terms in the above expression. The resulting data is then multiplexed together in the Output Flow Controller to yield the real output sample stream. The $\overline{\text{SYNC}}$ control input may be used to align the zero degree phase of the Up Convert LO with a particular input sample as described in the Operational Modes Section.

The Up Convert Processor also scales the data streams output from the Filter Processor as required by the operational mode. In the modes which employ interpolation, the Up Convert Processor scales the Filter Processor's output by two to compensate for the attenuation of one half caused by the interpolation process. In down convert and decimate mode, the filter processor output is also scaled by two to compensate for the attenuation introduced by the down covert process. The scaling operations performed are summarized in Table 4.

TABLE 4. SCALE FACTORS APPLIED BY UP CONVERT PROCESSOR vs MODE

MODE	SCALE FACTOR
Decimate by Two (MODE1-0 = 00)	1.0
Interpolate by Two (MODE1-0 = 01)	2.0
Down Convert and Decimate (MODE1-0 = 10)	2.0
Quadrature to Real (MODE1-0 = 11)	2.0

Output Data Flow Controller

The Output Flow Controller routes data to the AOUT0-15 and BOUT0-15 output depending on mode of operation. In decimate by two mode (MODE1-0 = 00), output from the filter processor's polyphase branches are summed and output through AOUT0-15. In Down Convert and Decimate mode (MODE1-0 = 10), real and imaginary data streams produced by the down convert process pass are output directly to AOUT0-15 and BOUT0-15 respectively. In the two modes using interpolation, MODE1-0 = 01 or 11, with internal multiplexing enabled, $\overline{\text{INT/EXT}}$ set high, data sam ples output from the polyphase branches are internally multiplexed into a single stream and output via AOUT0-15. If a mode using interpolation is specified together with external multiplexing, $\overline{\text{INT/EXT}}$ set low, the data stream multiplexing is performed off chip and the data on the upper and lower processing legs is output through AOUT0-15 and BOUT0-15.

The Output Data Flow Controller also sets the binary format and precision of the two 16-bit outputs. The data format is specified as either two's complement (FMT input low) or offset binary (FMT input high). The precision of the output data is set from 8 to 16 bits via the round control inputs, RND2-0. The RND2-0 inputs round the output data to a precision ranging from 8 to 16 bits as specified in Table 5. Saturation logic is incorporated in the output flow controller to insure that numerical growth associated with a worst case signal input or rounding condition saturates to a 16-bit value.

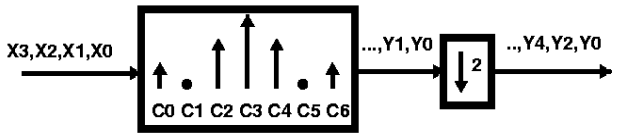
TABLE 5. OUTPUT ROUNDING CONTROL

RND 2-0	ROUND FUNCTION
000	Round output to 8 bits, AOUT15-8 and BOUT15-8, zero lower bits.
001	Round output to 9 bits, AOUT15-7 and BOUT15-7, zero lower bits.
010	Round output to 10 bits, AOUT15-6 and BOUT15-6, zero lower bits.
011	Round output to 11 bits, AOUT15-5 and BOUT15-5, zero lower bits.
100	Round output to 12 bits, AOUT15-4 and BOUT15-4, zero lower bits.
101	Round output to 14 bits, AOUT15-2 and BOUT15-2, zero lower bits.
110	Round output to 16 bits, AOUT15-0 and BOUT15-0.
111	Zero all outputs.

Operational Modes

Decimate By 2 Filter Mode (Mode1-0 = 00)

The concept of operation for Decimate by Two Filter mode is most easily understood by comparing the 7 tap transversal filter implementation to the equivalent polyphase implementation. The transversal implementation is shown in Figure 5.



$Y(0) = X0(C0)+X1(C1)+X2(C2)+X3(C3)+X4(C4)+X5(C5)+X6(C6)$
† $Y(1) = X1(C0)+X2(C1)+X3(C2)+X4(C3)+X5(C4)+X6(C5)+X7(C6)$
$Y(2) = X2(C0)+X3(C1)+X4(C2)+X5(C3)+X6(C4)+X7(C5)+X8(C6)$
† $Y(3) = X3(C0)+X4(C1)+X5(C2)+X6(C3)+X7(C4)+X8(C5)+X9(C6)$

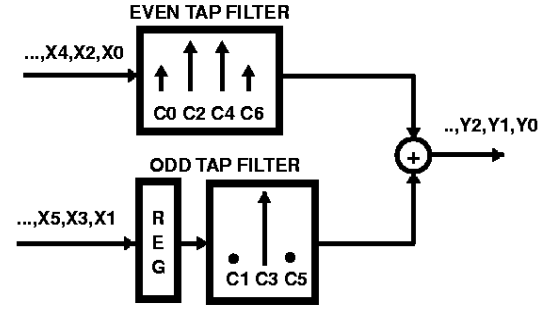
† Indicates samples discarded by decimation process

FIGURE 5. TRANSVERSAL IMPLEMENTATION OF DECIMATE BY 2 HALFBAND FILTER

By inspecting the sum-of-products for the decimated output in Figure 5, it is seen that even indexed input samples are always multiplied by the even filter coefficients and the odd samples are always multiplied by the odd coefficients. This computational partitioning is realized in the polyphase implementation shown in Figure 6.

In the polyphase implementation, the input data is broken into even and odd sample streams which are processed by a set of polyphase filters running at one half of the input data rate. These filters are designated as even or odd tap filters depending upon whether the coefficients were derived from the even or odd indexed coefficients of the original transversal filter. This architecture only produces the outputs which are not discarded by the decimation process. ***NOTE: Since the only non-zero tap for a halfband filter is the center tap, the Odd Tap Filter reduces to a delay and multiply operation.***

The operation of the HSP43216 in Decimate by Two mode is analogous to the polyphase implementation in Figure 6. In this mode, the internal data paths are routed as shown in Figure 7A and Figure 7B. The different data flows depend on whether internal or external multiplexing has been selected using the $\overline{INT/EXT}$ control input. In either case, an input data stream is decomposed into even and odd sample streams which are then routed to the even and odd tap polyphase filters. The output of each polyphase filter is summed and output via AOUT0-15.



$Y(0) = X0(C0)+X1(C1)+X2(C2)+X3(C3)+X4(C4)+X5(C5)+X6(C6)$
$Y(1) = X2(C0)+X3(C1)+X4(C2)+X5(C3)+X6(C4)+X7(C5)+X8(C6)$

FIGURE 6. POLYPHASE IMPLEMENTATION OF DECIMATE BY 2 HALFBAND FILTER

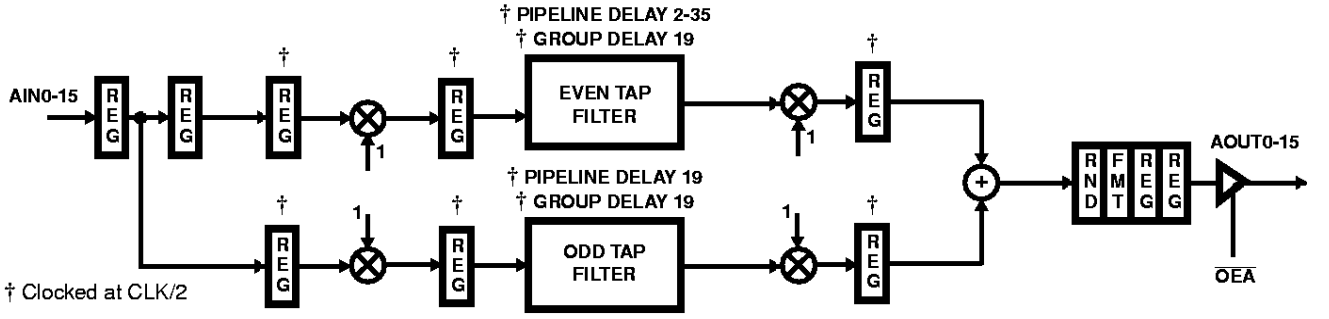


FIGURE 7A. DATA FLOW DIAGRAM FOR DECIMATE BY 2 FILTER MODE ($\overline{INT/EXT}$ = 1)

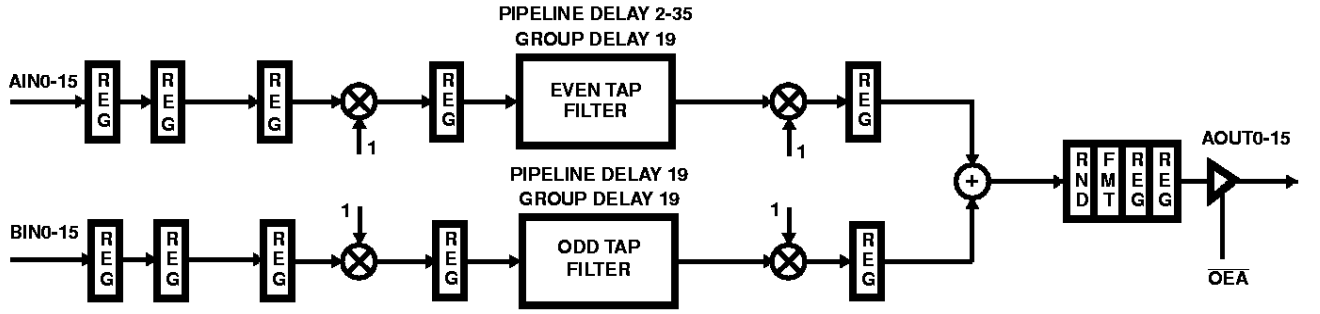
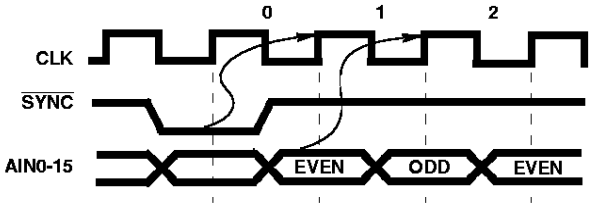


FIGURE 7B. DATA FLOW DIAGRAM FOR DECIMATE BY 2 FILTER MODE ($\overline{INT/EXT}$ = 0)

If internal multiplexing is selected ($\overline{INT/EXT}$ = 1), the input data stream is decomposed into even and odd samples internally by the processing elements operating at one half of the input CLK (see elements marked by "†" in Figure 7A). In this mode, the Data Flow Controller routes data samples input through AIN0-15 to upper and lower processing legs with a one sample relative delay. Since a new data sample is clocked into either of the processing legs at CLK/2, each leg processes a data stream comprised of every other input sample, and the one sample relative delay of each leg's input forces the even samples to be clocked into one leg while the odd samples are clocked into the other. The user may choose which sample gets routed to the upper (even) processing leg by asserting $\overline{SYNC}$. Specifically, a sample input on the CLK following the assertion of $\overline{SYNC}$ will be routed to the upper processing leg as shown in Figure 8. With internal multiplexing, the minimum pipeline delay on the upper processing leg is 14 CLK's and the pipeline delay on the bottom leg is 47 CLK's. The filtered and decimated data stream is held on AOUT0-15 for 2 CLK's.

If external multiplexing is selected ($\overline{INT/EXT}$ = 0), a demultiplex function is required off chip to break the input data into even and odd sample streams for input through AIN0-15 and BIN0-15. In this mode, the Data Flow Controller routes the even and odd sample streams directly to the following processing elements which are all running at the input CLK rate. This allows the device to perform decimate by two filtering on signals sampled at up to twice the maximum CLK rate of the device (104 MSPS). With external multiplexing, the minimum pipeline delay through the upper processing leg is 9 CLK's and the pipeline delay through the lower processing leg is 26 CLK's as shown in Figure 7B. In this mode, $\overline{SYNC}$ has no effect on part operation. ***NOTE: For proper operation, the samples demultiplexed to the AIN0-15 input must precede those input to the BIN0-15 input in sample order.*** For example, given a data sequence x0, x1, x2 and x3, the demultiplex function would route x0 and x2 to AIN0-15 and x1 and x3 to BIN0-15.



INPUTS DESIGNATED AS EVEN ARE PROCESSED ON THE UPPER LEG, INPUTS DESIGNATED AS ODD ARE PROCESSED ON THE LOWER LEG.

FIGURE 8. DATA SYNCHRONIZATION WITH PROCESSING LEGS ($\overline{INT/EXT}$ = 1)

Interpolate By 2 Filter Mode (Mode1-0 = 01)

As with the Decimate by Two mode the concept of operation for the Interpolate by Two Filter mode is more easily understood by comparing a 7 tap transversal filter implementation to the equivalent polyphase implementation. The transversal implementation is shown in Figure 9.

By inspecting filter outputs in Figure 9, it is seen that the even indexed outputs are the result of the sum-of-products for the odd coefficients, and the odd indexed outputs are the result of the sum-of-products for the even coefficients. This computational partitioning is evident in the polyphase implementation shown in Figure 10.

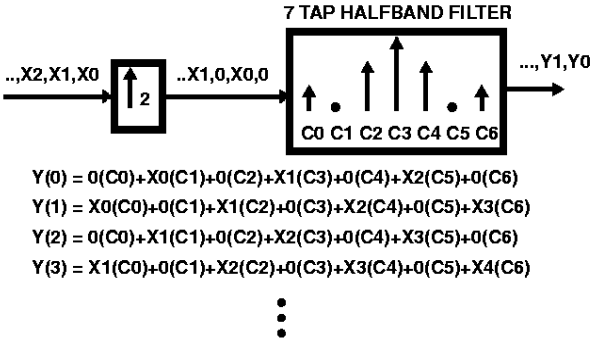


FIGURE 9. TRANSVERSAL IMPLEMENTATION OF INTERPOLATE BY TWO HALFBAND FILTER

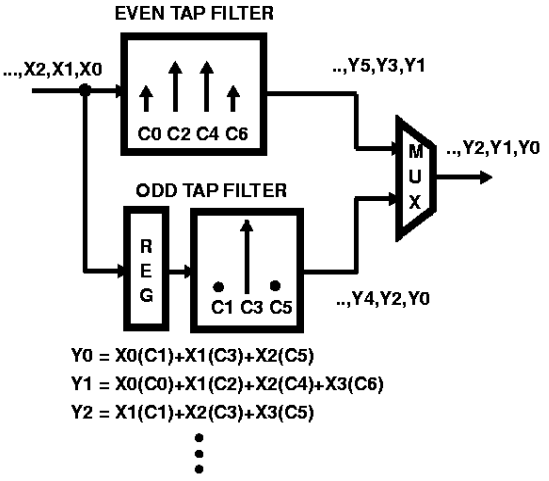


FIGURE 10. POLYPHASE IMPLEMENTATION OF INTERPOLATE BY TWO HALFBAND FILTER

In the polyphase implementation, the input data stream feeds even and odd tap filters running at the input sample rate. The interpolated sample stream is derived by multiplexing the output of each polyphase branch into a single data stream at twice the input sample rate. As in the Decimate by Two example, the even or odd tap filters are comprised of the even or odd indexed coefficients from the original transversal filter.

The operation of the HSP43216 in Interpolate by Two mode is analogous to the polyphase example above. In this mode the internal data flow is routed as shown in Figure 11A and Figure 11B. The different data flows depend on the selection of internal or external multiplexing via $\overline{INT/EXT}$. In this mode, data input through AIN0-15 is fed to the even and odd polyphase branches of the filter processor. The output of each branch is multiplexed together to generate the output data stream at the interpolated rate. ***NOTE: The output of each polyphase branch is scaled by two to compensate for the attenuation of one half caused by interpolation.***

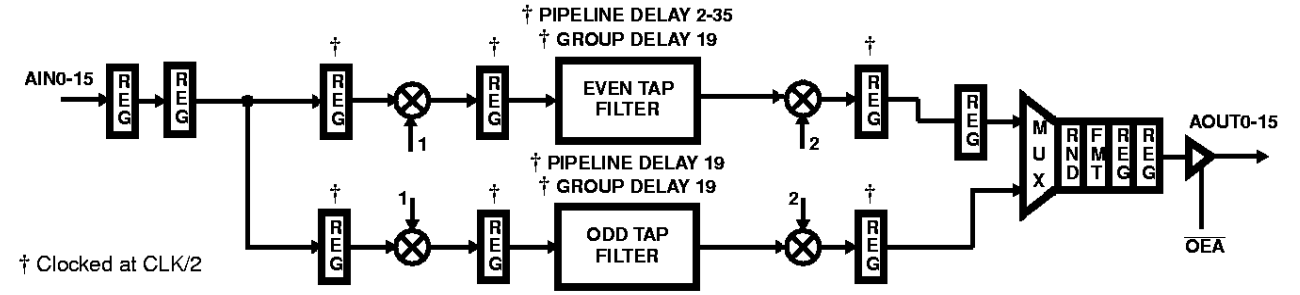


FIGURE 11A. DATA FLOW DIAGRAM FOR INTERPOLATE BY 2 FILTER MODE ($\overline{INT/EXT}$ = 1)

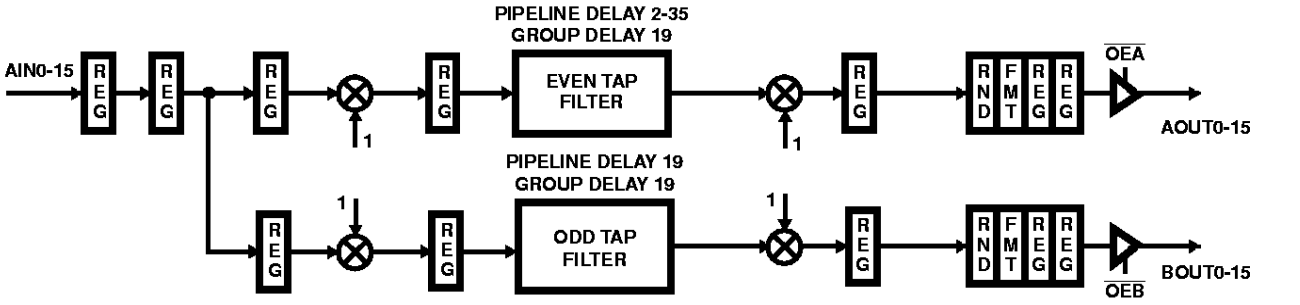


FIGURE 11B. DATA FLOW DIAGRAM FOR INTERPOLATE BY 2 FILTER MODE ($\overline{INT/EXT}$ = 0)

If internal multiplexing is selected (INT/EXT = 1), the data stream input through AIN0-15 is fed to both the upper and lower processing legs as shown in Figure 11A. The output of each processing leg is then multiplexed together to produce the interpolated sample stream at twice the input sample rate. In this mode the device is clocked at the interpolated data rate to support the multiplexing of each processing leg's output into a single data stream. The upper and lower processing legs each run at the input data rate of CLK/2 as indicated by the "†" marking the various registers and processing elements in Figure 11A. In this mode, data samples are clocked into the part on every other **rising edge** of CLK. The SYNC signal is used to specify which set of CLK cycles are used to register data at the part's input. Specifically, every other rising edge of CLK starting one CLK after the assertion of SYNC will be used to clock data into the part. With internal multiplexing the minimum pipeline delay through the upper processing leg is 15 CLK's and the pipeline delay through the lower processing leg is 48 CLK's.

If external multiplexing is selected ($\overline{INT/EXT}$ = 0), the upper and lower processing legs are output through AOUT0-15 and BOUT0-15 for multiplexing into a single data stream off chip.This allows the processing legs to run at the maximum clock rate which coincides with an interpolated output data rate of 104 MSPS. ***NOTE: The samples output on BOUT0-15 precede those on AOUT0-15 in sample order.*** This requires a multiplexing scenario in which BOUT0-15 is selected before AOUT0-15. With external multiplexing, the minimum pipeline delay through the upper processing leg is 9 CLK's and the pipeline delay through the lower processing leg is 26 CLK's as shown in Figure 11B. In this mode $\overline{SYNC}$ has no effect on part operation.

Down Convert and Decimate Mode (MODE1-0 = 10)

In Down Convert and Decimate Mode a real input signal is spectrally shifted -F_S/4 which centers the upper sideband at DC. This operation produces real and imaginary components which are each filtered and decimated by identical 67-tap halfband filters. For added flexibility, a positive F_S/4 spectral shift may be selected which centers the lower sideband at DC. The direction of the spectral shift is selected via USB/LSB as described in the Quadrature Down Convert section. A spectral representation of the down convert and decimate operation is shown in Figure 12 (USB/LSB = 1). ***NOTE: Each of the complex terms output by the Filter Processor are scaled by two to compensate for the attenuation of one half introduced by the down conversion process.***

The Down Convert and Decimate mode is most easily understood by first considering the transversal implementation using a 7 tap filter as shown in Figure 13.

By examining the combination of down conversion, filtering and decimation, it is seen that the real outputs are only dependent on the sum-of-products for the even indexed samples and filter coefficients, and the imaginary outputs are only a function of the sum-of-products for the odd indexed samples and filter coefficients. This computational partitioning allows the quadrature filters required after down conversion to be realized using the same poly-phase processing elements used in the previous two modes.

A functional block diagram of the polyphase implementation is shown in Figure 14. In this implementation, the input data stream is broken into even and odd sample streams and processed independently by the even and odd tap filters. By decomposing the sample stream into even and odd samples, the zero mix terms produced by the down convert LO drop out of the data streams, and the output of each of the filters represent the decimated data streams for both the real and imaginary outputs.

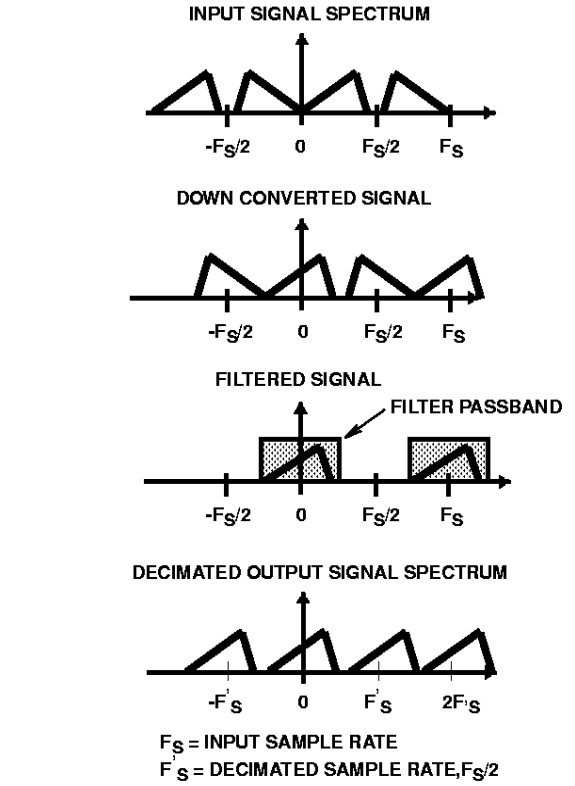
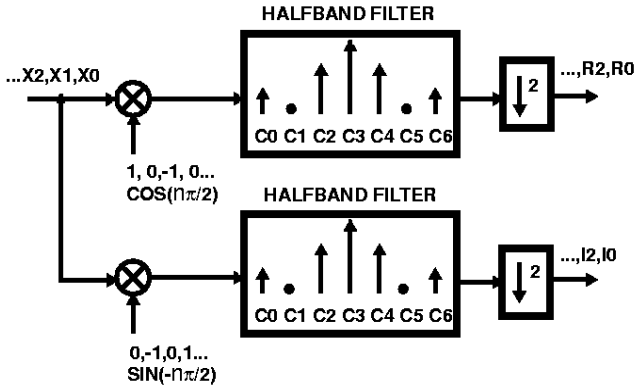


FIGURE 12. DOWN CONVERT AND DECIMATE OPERATION



REAL OUTPUTS

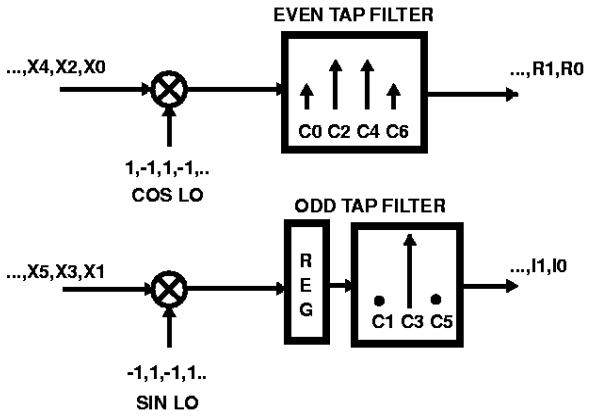
R0 = X0(C0)+0(C1)-X2(C2)+0(C3)+X4(C4)+0(C5)-X6(C6)
† R1 = 0(C0)-X2(C1)+0(C2)+X4(C3)+0(C4)-X6(C5)+0(C6)
R2 = -X2(C0)+0(C1)+X4(C2)+0(C3)-X6(C4)+0(C5)+X4(C6)
† R3 = 0(C0)+X4(C1)+0(C2)-X6(C3)+0(C4)+X4(C5)+0(C6)

IMAGINARY OUTPUTS

I0 = 0(C0)-X1(C1)+0(C2)+X3(C3)+0(C4)-X5(C5)+0(C6)
† I1 = -X1(C0)+0(C1)+X3(C2)+0(C3)-X5(C4)+0(C5)+X7(C6)
I2 = 0(C0)+X3(C1)+0(C2)-X5(C3)+0(C4)+X7(C5)+0(C6)
† I3 = X3(C0)+0(C1)-X5(C2)+0(C3)+X7(C4)+0(C5)-X9(C6)

† Indicates samples discarded by decimation process

FIGURE 13. DOWN CONVERT AND DECIMATE FUNCTION USING TRANSVERSAL FILTERS



REAL OUTPUTS

R0 = X0(C0)-X2(C2)+X4(C4)-X6(C6)
R1 = -X2(C0)+X4(C2)-X6(C4)+X8(C6)
R2 = X4(C0)-X6(C2)+X8(C4)-X10(C6)

IMAGINARY OUTPUTS

I0 = -X1(C1)+X3(C3)-X5(C5)
I1 = X3(C1)-X5(C3)+X7(C5)
I2 = -X5(C1)+X7(C3)-X9(C5)

FIGURE 14. DOWN CONVERT AND DECIMATE FUNCTION USING POLYPHASE FILTERS

The HSP43216's implementation of Down Convert and Decimate mode is analogous to the polyphase solution shown in Figure 14. The part's data flow diagram for this mode is shown in Figure 15A and Figure 15B. As seen in the figures, the input sample data is broken into even and odd sample streams which feed the upper and lower processing legs as described in the Decimate By 2 Mode section. The data on each processing leg is then modulated with the nonzero quadrature components of the complex exponent (see Quadrature Down Convert Section). Following this operation, the upper leg becomes the processing chain for the real (In-phase) component of the quadrature down conversion and the lower leg processes the complex (Quadrature) component of the down conversion. The filter processing block implements the equivalent of a decimate by two Halfband filter on each of the quadrature legs.

If internal multiplexing is specified (INT/EXT = 1), the upper and lower processing legs are fed with even and odd sample streams which are derived from data input through AIN0-15. The input sample stream may be synchronized with the zero degree phase term of the down converter LO by using the SYNC control input. For example, an input data sample will be fed into the real (upper) processing leg and mixed with the zero degree cosine term of the quadrature LO if it is input on the 4th CLK following the assertion of SYNC as shown in Figure 16. The pipeline delay through the real processing leg (upper leg) is 14 CLK's and the delay through the imaginary processing leg (lower leg) is 47 CLK's. The complex samples output through AOUT0-15 and BOUT0-15 are present for 2 CLK's since the quadrature streams have been decimated by two in the filter processor.

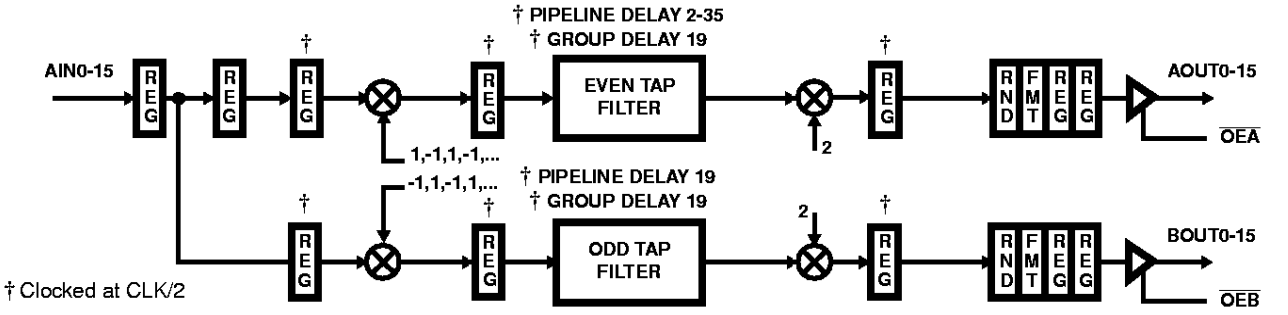


FIGURE 15A. DATA FLOW DIAGRAM FOR DOWN CONVERT AND DECIMATE MODE ($\overline{INT/EXT}$ = 1)

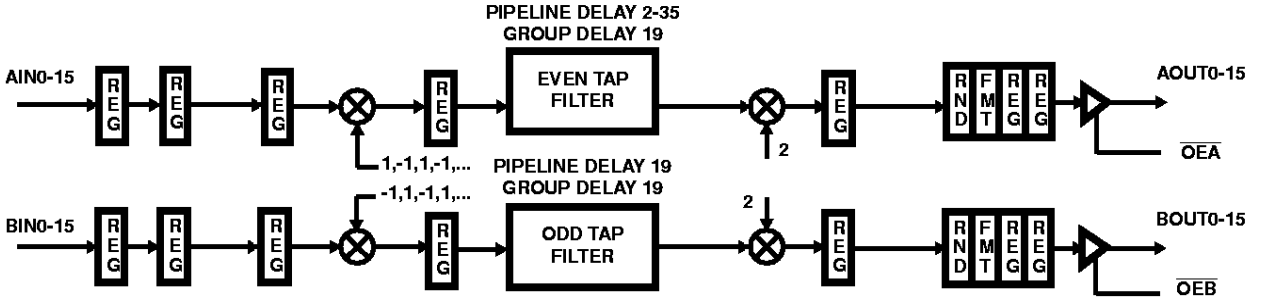
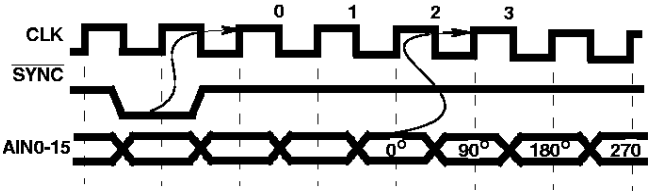
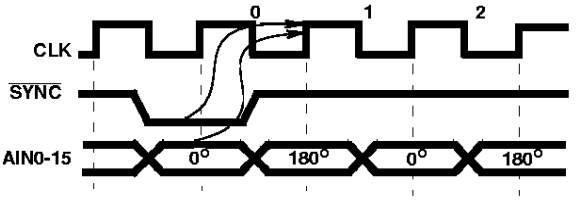


FIGURE 15B. DATA FLOW DIAGRAM FOR DOWN CONVERT AND DECIMATE MODE ($\overline{INT/EXT}$ = 0)



THE SAMPLE DESIGNATED BY THE 0° AND 180° LABELS ARE MIXED WITH THE RESPECTIVE COSINE TERMS ON THE UPPER PROCESSING LEG, AND THE OTHER SAMPLES, THOSE LABELED BY 90° AND 270°, ARE MIXED WITH THE RESPECTIVE SINE TERMS ON THE LOWER LEG.

FIGURE 16. DATA SYNCHRONIZATION TO 0° PHASE OF QUADRATURE LO



THE 0° AND 180° LABELS INDICATE THE PHASE ALIGNMENT OF THE SAMPLES INPUT THROUGH AIN0-15 WITH THE COSINE TERM OF THE QUADRATURE DOWN CONVERT LO.

FIGURE 17. DATA SYNCHRONIZATION WITH PHASE OF DOWN CONVERT LO

If external multiplexing is selected ($\overline{INT/EXT}$ = 0), a demultiplex function is required off chip to break the input data stream into even and odd samples for input through AIN0-15 and BIN0-15. In this mode, the real and imaginary processing legs run at the input clock rate which allows the device to perform the down convert and decimate function on real signals sampled at up to twice the maximum speed grade of the device (104 MSPS). With external multiplexing, the minimum pipeline delay through the upper processing leg is 9 CLK's and the pipeline delay through the lower processing leg is 26 CLK's as shown in Figure 15B. To synchronize the even samples input through AIN0-15 with the zero degree cosine term of the quadrature LO, $\overline{SYNC}$ should be asserted on the same clock that the target sample is present at the input of the part as shown in Figure 17. ***NOTE: For proper operation, the samples demultiplexed to the AIN0-15 input must precede those input to the BIN0-15 input in sample order. For example, given a data sequence x0, x1, x2, and x3, the demultiplex function would route x0 and x2 to AIN0-15 and x1 and x3 to BIN0-15.***

Quadrature to Real Conversion Mode (MODE1-0 = 11)

The Quadrature to Real Conversion mode is used to construct a real output from a quadrature input. To accomplish this, the Halfband Filter Processor interpolates the quadrature components of the complex input signal by a factor of two. Next, the Quadrature Up-Convert Processor spectrally shifts the signal by $F_S/4$ and derives the real output as described in the $F_S/4$ Quadrature Up-Convert Processor Section. The direction of the spectral shift is controlled via the $\overline{USB/LSB}$ input and is used to designate the frequency content of the complex input as either the upper or lower sideband of the resulting real output signal. A spectral representation of quadrature to real conversion is shown in Figure 18 for $\overline{USB/LSB}$ = 1. ***NOTE: The $F_S/4$ Up-Convert Processor uses quadrature mix factors scaled by two to compensate for the attenuation introduced by the interpolation process.***

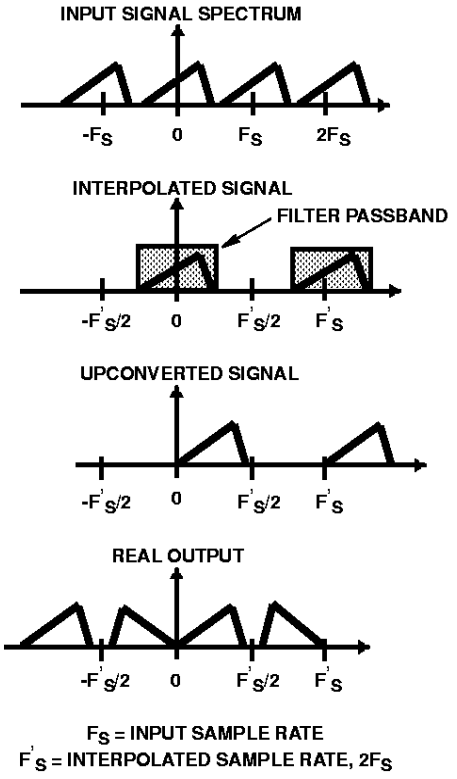
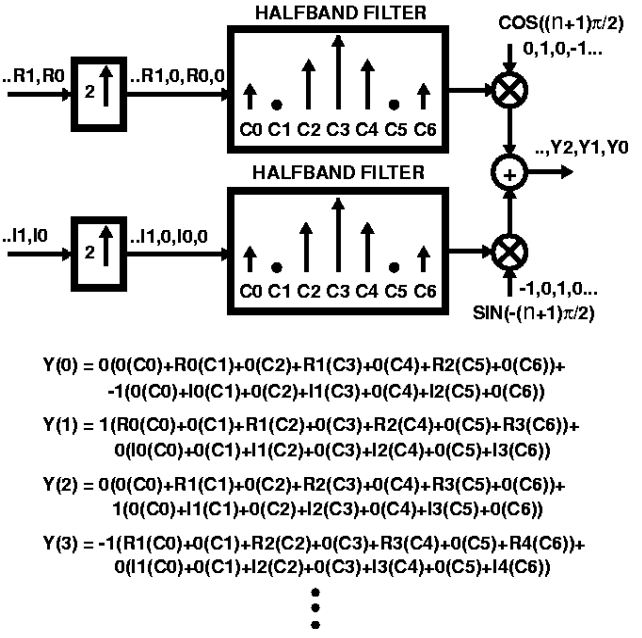


FIGURE 18. QUADRATURE TO REAL CONVERSION

The Quadrature to Real Conversion mode is most easily understood by first considering an implementation using a 7 tap transversal filter as shown in Figure 19. By examining the combination of interpolation, filtering, and up conversion it is seen that a particular output is only dependent on the sum-of-products for the even indexed samples and coefficients or the sum-of-products for the odd indexed samples and coefficients. This computational partitioning allows the dual interpolation filters required in this mode to be realized using the same polyphase filter structure used in the other modes. A functional block diagram of the polyphase implementation for Quadrature to Real Conversion mode is shown in Figure 20. In this implementation, the real and imaginary components of a complex input stream drive the even and odd tap filters. The output of each filter is then modulated by the non-zero mix factors and multiplexed into a single real output stream.



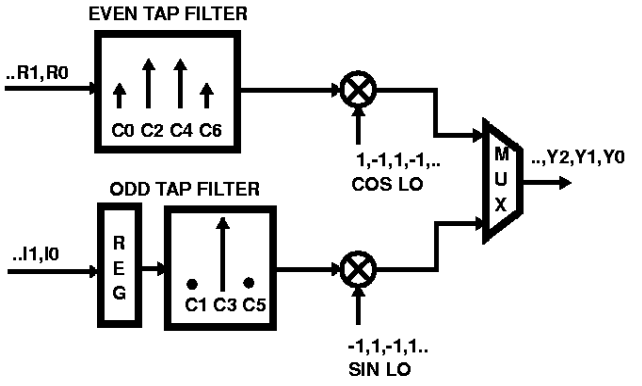
$Y(0) = 0(0(C0)+R0(C1)+0(C2)+R1(C3)+0(C4)+R2(C5)+0(C6))+ -1(0(C0)+I0(C1)+0(C2)+I1(C3)+0(C4)+I2(C5)+0(C6))$

$Y(1) = 1(R0(C0)+0(C1)+R1(C2)+0(C3)+R2(C4)+0(C5)+R3(C6))+ 0(I0(C0)+0(C1)+I1(C2)+0(C3)+I2(C4)+0(C5)+I3(C6))$

$Y(2) = 0(0(C0)+R1(C1)+0(C2)+R2(C3)+0(C4)+R3(C5)+0(C6))+ 1(0(C0)+I1(C1)+0(C2)+I2(C3)+0(C4)+I3(C5)+0(C6))$

$Y(3) = -1(R1(C0)+0(C1)+R2(C2)+0(C3)+R3(C4)+0(C5)+R4(C6))+ 0(I1(C0)+0(C1)+I2(C2)+0(C3)+I3(C4)+0(C5)+I4(C6))$

FIGURE 19. QUADRATURE TO REAL CONVERTER USING TRANSVERSAL FILTERS



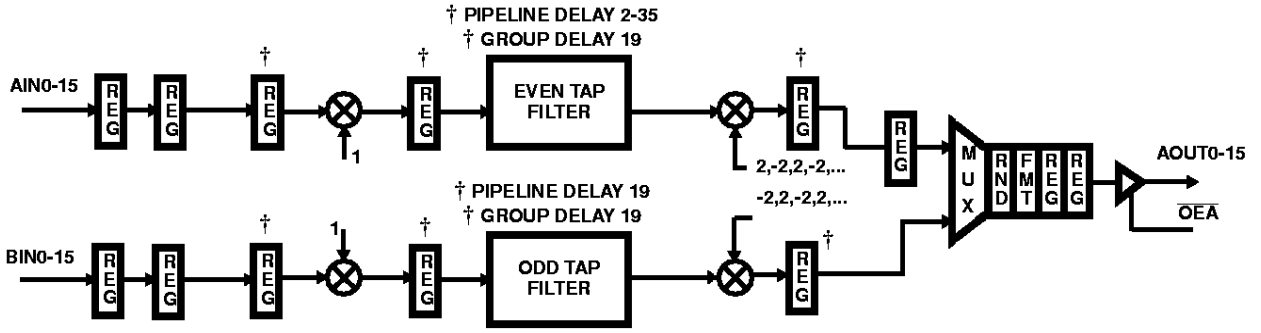
$Y(0) = -1(I0(C1)+I1(C3))+I2(C5))$

$Y(1) = 1(R0(C0)+R1(C2)+R2(C4))+R3(C6))$

$Y(2) = 1(I1(C1)+I2(C3)+I3(C5))$

$Y(3) = -1(R1(C0)+R2(C2)+R3(C4)+R4(C6))$

FIGURE 20. POLYPHASE IMPLEMENTATION OF QUADRATURE TO REAL CONVERTER



† Clock at Input data rate, CLK/2

FIGURE 21A. DATA FLOW DIAGRAM FOR QUADRATURE TO REAL CONVERSION MODE ($\overline{INT/EXT}$ = 1)

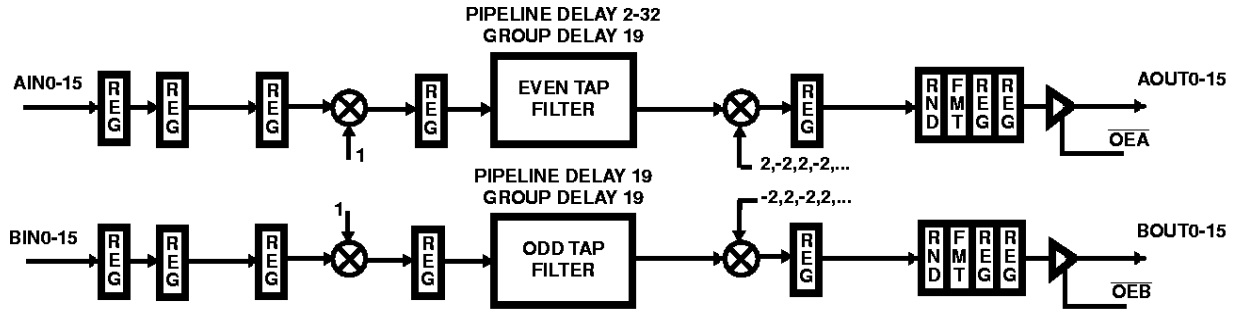


FIGURE 21B. DATA FLOW DIAGRAM FOR QUADRATURE TO REAL CONVERSION MODE ($\overline{INT/EXT}$ = 0)

As in the other modes, the operation of the HSP43216 in Quadrature to real Conversion mode is analogous to that of the polyphase solution described above. The data flow diagrams for this particular mode are shown in Figures 21A and 21B.

If Internal Multiplexing is specified ($\overline{INT/EXT}$ = 1), the real and imaginary components of the quadrature input are fed through AIN0-15 and BIN0-15 and processed on the upper and lower legs respectively (see Figure 21A). Each component of the complex input is interpolated, mixed with the non-zero sine and cosine terms of the quadrature LO, and multiplexed together into a real output sample stream through AOUT0-15. Prior to the output multiplexer, the upper and lower processing legs each run at the input data rate of CLK/2 as indicated by the "†" marking the various registers and processing elements in Figure 21A. The complex input sample stream may be synchronized with the zero degree phase of the up converters quadrature LO by asserting the $\overline{SYNC}$ control input one cycle prior to the targeted data sample as shown in Figure 22. This ensures that the real sample input on the upper processing leg will be mixed with the zero degree cosine term. The minimum pipeline delay through the real processing leg (upper leg) is 15 CLK's and the delay through the imaginary processing leg (lower leg) is 48 CLK's.

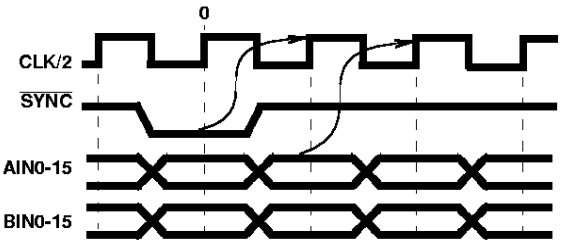


FIGURE 22. DATA SYNCHRONIZATION WITH PROCESSING LEGS ($\overline{INT/EXT}$ = 1)

If external multiplexing is selected ($\overline{INT/EXT}$ = 0), output from the upper and lower processing legs exit through AOUT0-15 and BOUT0-15 for multiplexing into a single data stream off chip (see Figure 21B).This allows the processing legs to run at the maximum CLK rate which coincides with an interpolated output data rate of up to 104 MSPS. ***NOTE: The output on BOUT0-15 precedes that on AOUT0-15 in sample order.*** This requires a multiplexing scenario which selects BOUT0-15 then AOUT0-15 on each CLK of the HSP43216. With external multiplexing, the minimum pipeline delay through the upper processing leg is 9 CLK's and the pipeline delay through the lower processing leg is 26 CLK's as shown in Figure 21B. The $\overline{SYNC}$ control input is used as described in the preceding paragraph.

Absolute Maximum Ratings

Supply Voltage . . . . . +7.0V
Input, Output or I/O Voltage . . . . . GND -0.5V to V_{CC} +0.5V
ESD Classification . . . . . Class 1

Operating Conditions

Voltage Range . . . . . +4.75V to +5.25V
Temperature Range . . . . . 0°C to 70°C

Thermal Information

Thermal Resistance (Typical, Note 1)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
CPGA Package	40	8
PLCC Package	23.0	N/A
MQFP Package	35.0	N/A

Maximum Junction Temperature
PLCC and MQFP Packages . . . . . 150°C
CPGA Package . . . . . 175°C
Maximum Storage Temperature Range . . . . . -65°C to 150°C
Maximum Lead Temperature (Soldering 10s) . . . . . 300°C
(PLCC and MQFP Lead Tips Only)

Die Characteristics

Gate Count . . . . . 35469 Gates

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

1. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

DC Electrical Specifications V_{CC} = 5.0V ± 5%, T_A = 0° to 70°C

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	MAX	UNITS
Power Supply Current	I_{CCOP}	V_{CC} = Max, CLK Frequency 52MHz $\overline{INT/EXT}$ = '1', Notes 2, 4	-	468	mA
		V_{CC} = Max, CLK Frequency 52MHz $\overline{INT/EXT}$ = '0', Notes 3, 4	-	572	mA
Standby Power Supply Current	I_{CCSB}	V_{CC} = Max, Outputs Not Loaded	-	500	µA
Input Leakage Current	I_I	V_{CC} = Max, Input = 0V or V_{CC}	-10	10	µA
Output Leakage Current	I_O	V_{CC} = Max, Input = 0V or V_{CC}	-10	10	µA
Clock Input High	V_{IHC}	V_{CC} = Max	3.0	-	V
Clock Input Low	V_{ILC}	V_{CC} = Min	-	0.8	V
Logical One Input Voltage	V_{IH}	V_{CC} = Max	2.0	-	V
Logical Zero Input Voltage	V_{IL}	V_{CC} = Min	-	0.8	V
Logical One Output Voltage	V_{OH}	I_{OH} = -3mA, V_{CC} = Min	2.6	-	V
Logical Zero Output Voltage	V_{OL}	I_{OL} = 5mA, V_{CC} = Min	-	0.4	V
Input Capacitance	C_{IN}	CLK Frequency 1MHz, All measurements referenced to GND. T_A = 25°C, Note 5	-	12	pF
Output Capacitance	C_{OUT}		-	12	pF

NOTES:

2. Power supply current is proportional to frequency. Typical rating is 9mA/MHz when Internal Multiplexing is selected, $\overline{INT/EXT}$ = 1.
3. Power supply current is proportional to frequency. Typical rating is 11mA/MHz when External Multiplexing is selected, $\overline{INT/EXT}$ = 0.
4. Output load per test circuit and C_L = 40pF.
5. Not tested, but characterized at initial design and at major process/design changes.
6. Maximum junction temperature must be considered when operating part at high clock frequencies.

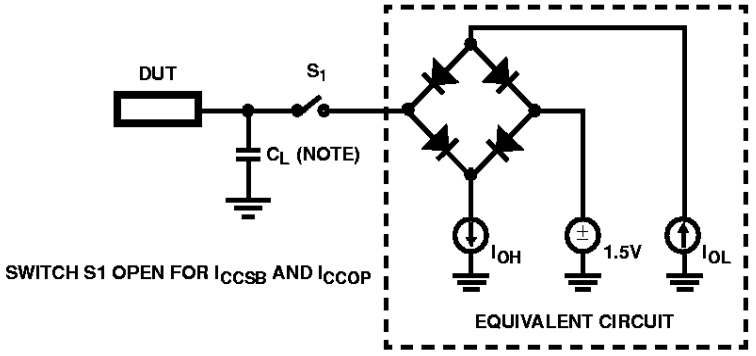
AC Electrical Specifications (Note 7)

PARAMETER	SYMBOL	NOTES	52MHz		UNITS
			MIN	MAX	
CLK Period	t_{CP}		19	-	ns
CLK High	t_{CH}		7	-	ns
CLK Low	t_{CL}		7	-	ns
Setup Time AIN0-15, BIN0-15 to CLK	t_{DS}		7	-	ns
Hold Time AIN0-15, BIN0-15 from CLK	t_{DH}		0	-	ns
MODE0-1, RND0-2, $\overline{\text{INT/EXT}}$, $\overline{\text{SYNC}}$, $\overline{\text{USB/LSB}}$ Setup Time to CLK	t_{RS}		7	-	ns
MODE0-1, RND0-2, $\overline{\text{INT/EXT}}$, $\overline{\text{SYNC}}$, $\overline{\text{USB/LSB}}$ Hold Time to CLK	t_{RH}		0	-	ns
CLK to AOUT0-15, BOUT0-15 Delay	t_{DO}		-	9	ns
Output Enable Time	t_{OE}		-	9	ns
Output Disable Time	t_{OD}	Note 8	-	9	ns
Output Rise, Output Fall Times	t_r, t_f	Note 8	-	5	ns

NOTES:

7. AC tests performed with C_L = 40pF, I_{OL} = 5mA, and I_{OH} = -3mA. Input reference level for CLK is 2.0V, all other inputs 1.5V. Test V_{IH} = 3.0V, V_{IHC} = 4.0V, V_{IL} = 0V.
8. Controlled via design or process parameters and not directly tested. Characterized upon initial design and after major process and/or changes.

AC Test Load Circuit



NOTE: Test head capacitance.

Waveforms

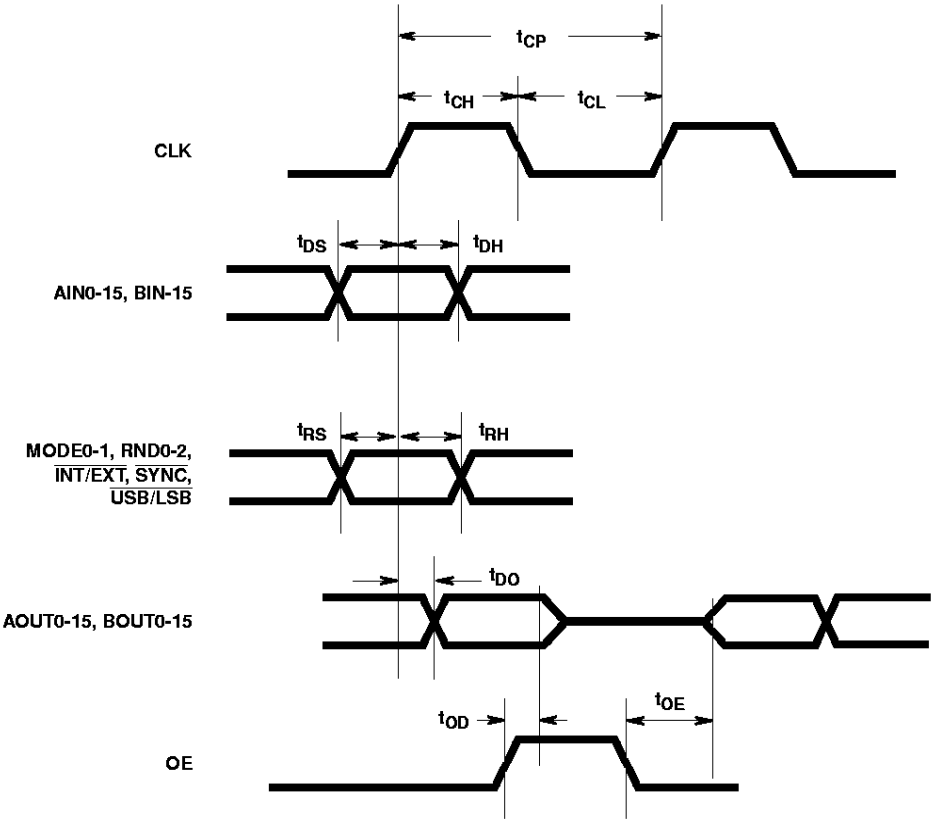


FIGURE 23. TIMING RELATIVE TO CLK

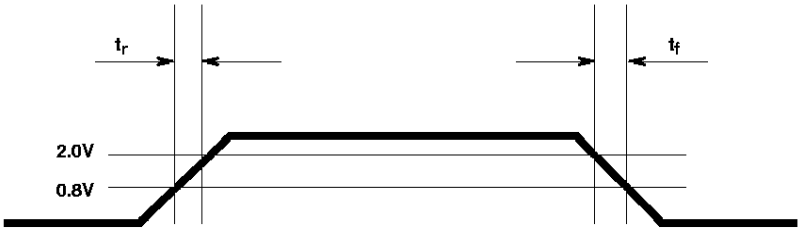
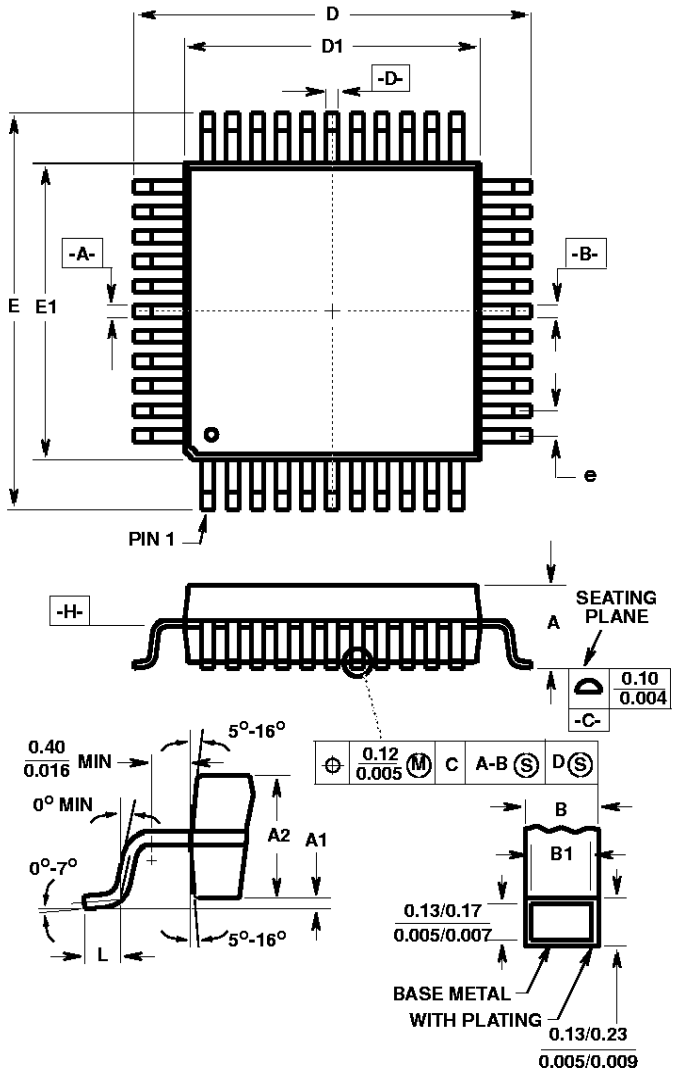


FIGURE 24. OUTPUT RISE AND FALL TIMES

Metric Plastic Quad Flatpack Packages (MQFP)



Q100.14x20 (JEDEC MO-108CC-1 ISSUE A)
100 LEAD METRIC PLASTIC QUAD FLATPACK PACKAGE

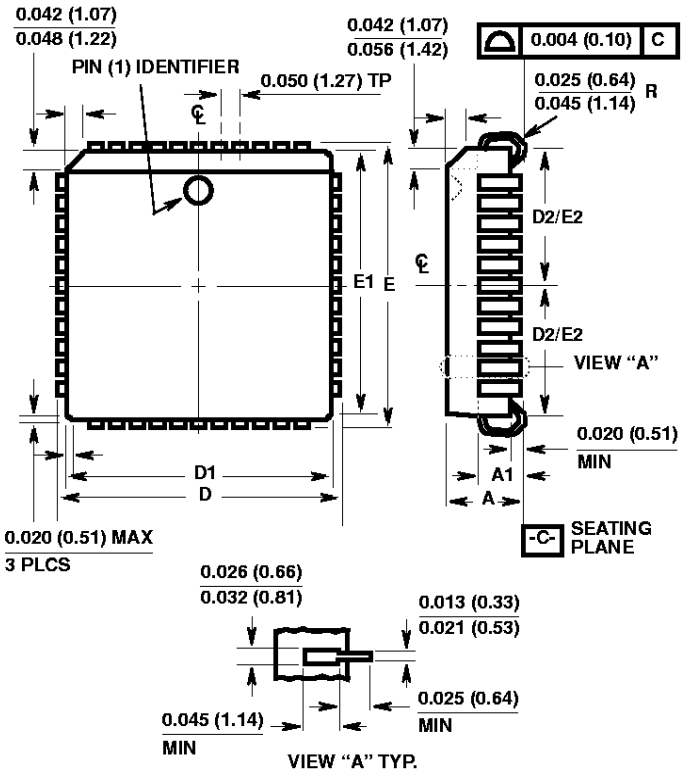
SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.134	-	3.40	-
A1	0.010	-	0.25	-	-
A2	0.100	0.120	2.55	3.05	-
B	0.009	0.015	0.22	0.38	6
B1	0.009	0.013	0.22	0.33	-
D	0.904	0.923	22.95	23.45	3
D1	0.783	0.791	19.90	20.10	4, 5
E	0.667	0.687	16.95	17.45	3
E1	0.547	0.555	13.90	14.10	4, 5
L	0.026	0.037	0.65	0.95	-
N	100		100		7
e	0.026 BSC		0.65 BSC		-
ND	30		30		-
NE	20		20		-

Rev. 0 1/94

NOTES:

1. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact.
2. All dimensions and tolerances per ANSI Y14.5M-1982.
3. Dimensions D and E to be determined at seating plane -C-.
4. Dimensions D1 and E1 to be determined at datum plane -H-.
5. Dimensions D1 and E1 do not include mold protrusion. Allowable protrusion is 0.25mm (0.010 inch) per side.
6. Dimension B does not include dambar protrusion. Allowable dambar protrusion shall be 0.08mm (0.003 inch) total.
7. "N" is the number of terminal positions.

Plastic Leaded Chip Carrier Packages (PLCC)



N84.1.15 (JEDEC MS-018AF ISSUE A)
84 LEAD PLASTIC LEADED CHIP CARRIER PACKAGE

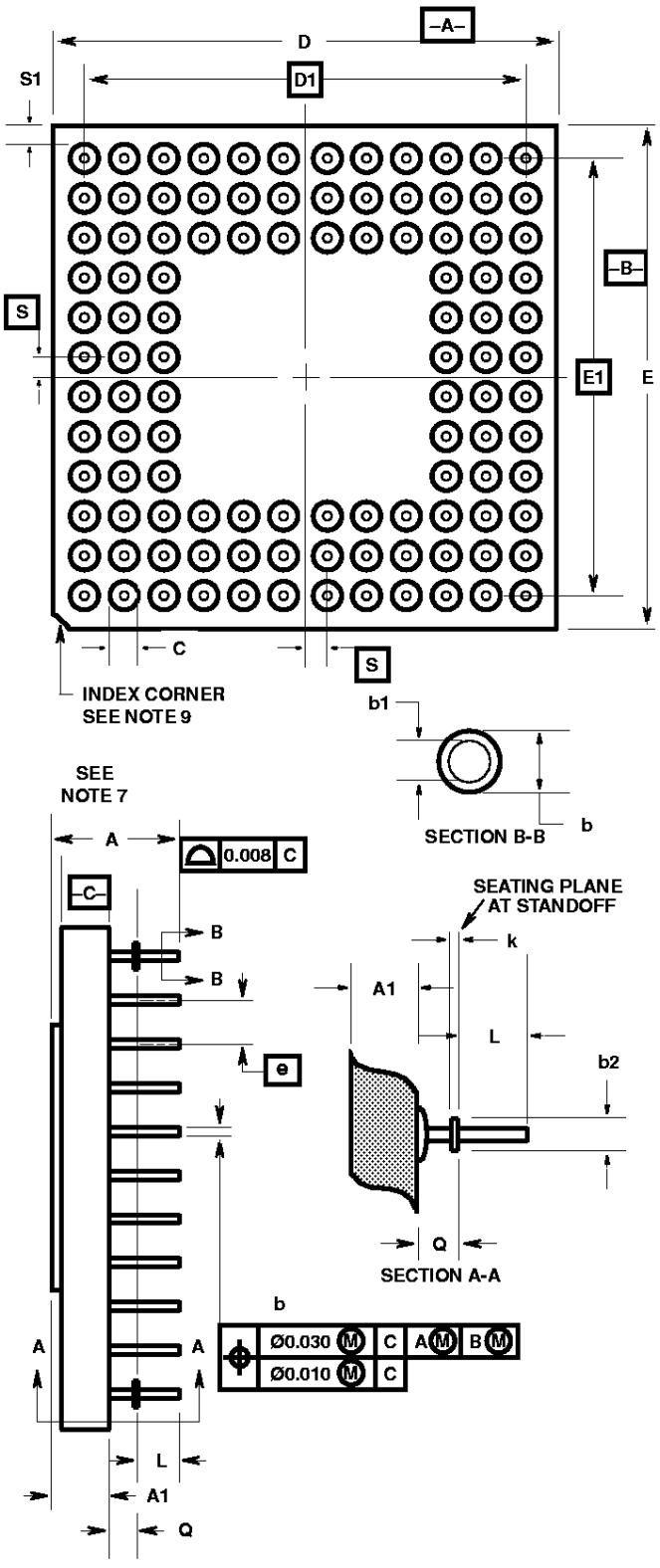
SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.165	0.180	4.20	4.57	-
A1	0.090	0.120	2.29	3.04	-
D	1.185	1.195	30.10	30.35	-
D1	1.150	1.158	29.21	29.41	3
D2	0.541	0.569	13.75	14.45	4, 5
E	1.185	1.195	30.10	30.35	-
E1	1.150	1.158	29.21	29.41	3
E2	0.541	0.569	13.75	14.45	4, 5
N	84		84		6

Rev. 1 3/95

NOTES:

1. Controlling dimension: INCH. Converted millimeter dimensions are not necessarily exact.
2. Dimensions and tolerancing per ANSI Y14.5M-1982.
3. Dimensions D1 and E1 do not include mold protrusions. Allowable mold protrusion is 0.010 inch (0.25mm) per side.
4. To be measured at seating plane -C- contact point.
5. Centerline to be determined where center leads exit plastic body.
6. "N" is the number of terminal positions.

Ceramic Pin Grid Array Packages (CPGA)



G85.A MIL-STD-1835 CMGA3-P85C (P-AC)
85 LEAD CERAMIC PIN GRID ARRAY PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.215	0.345	5.46	8.76	-
A1	0.070	0.145	1.78	3.68	3
b	0.016	0.0215	0.41	0.55	8
b1	0.016	0.020	0.41	0.51	-
b2	0.042	0.058	1.07	1.47	4
C	-	0.080	-	2.03	-
D	1.140	1.180	28.96	29.97	-
D1	1.000 BSC		25.4 BSC		-
E	1.140	1.180	28.96	29.97	-
E1	1.000 BSC		25.4 BSC		-
e	0.100 BSC		2.54 BSC		6
k	0.008 REF		0.20 REF		-
L	0.120	0.140	3.05	3.56	-
Q	0.040	0.060	1.02	1.52	5
S	0.000 BSC		0.00 BSC		10
S1	0.003	-	0.08	-	-
M	11		11		1
N	-	121	-	121	2

Rev. 1 6/21/95

NOTES:

1. "M" represents the maximum pin matrix size.
2. "N" represents the maximum allowable number of pins. Number of pins and location of pins within the matrix is shown on the pinout listing in this data sheet.
3. Dimension "A1" includes the package body and Lid for both cavity-up and cavity-down configurations. This package is cavity up. Dimension "A1" does not include heatsinks or other attached features.
4. Standoffs are intrinsic and shall be located on the pin matrix diagonals. The seating plane is defined by the standoffs at dimensions Q.
5. Dimension "Q" applies to cavity-up configurations only.
6. All pins shall be on the 0.100 inch grid.
7. Datum C is the plane of pin to package interface for both cavity up and down configurations.
8. Pin diameter includes solder dip or custom finishes. Pin tips shall have a radius or chamfer.
9. Corner shape (chamfer, notch, radius, etc.) may vary from that shown on the drawing. The index corner shall be clearly unique.
10. Dimension "S" is measured with respect to datums A and B.
11. Dimensioning and tolerancing per ANSI Y14.5M-1982.
12. Controlling dimension: INCH.