FAIRCHILD SEMICONDUCTOR®

November 2006

FXL2TD245

Low Voltage Dual Supply 2-Bit Signal Translator with Configurable Voltage Supplies and Signal Levels and 3-STATE Outputs and Independent Direction Controls

General Description

The FXL2TD245 is a configurable dual-voltage-supply translator designed for both uni-directional and bi-directional voltage translation between two logic levels. The device allows translation between voltages as high as 3.6V to as low as 1.1V. The A Port tracks the V_{CCA} level, and the B Port tracks the V_{CCB} level. This allows for bi-directional voltage translation over a variety of voltage levels: 1.2V, 1.5V, 1.8V, 2.5V, and 3.3V.

The device remains in 3-STATE until both V_{CC}s reach active levels allowing either V_{CC} to be powered-up first. Internal power down control circuits place the device in 3-STATE if either V_{CC} is removed.

The Transmit/Receive inputs independently determine the direction of data through each of the two bits. The $\overline{OE}$ input, when HIGH, disables both the A and B Ports by placing them in a 3-STATE condition. The FXL2TD245 is designed so that the control pins ($T/\overline{R}$ and $\overline{OE}$) are supplied by V_{CCA}.

Features

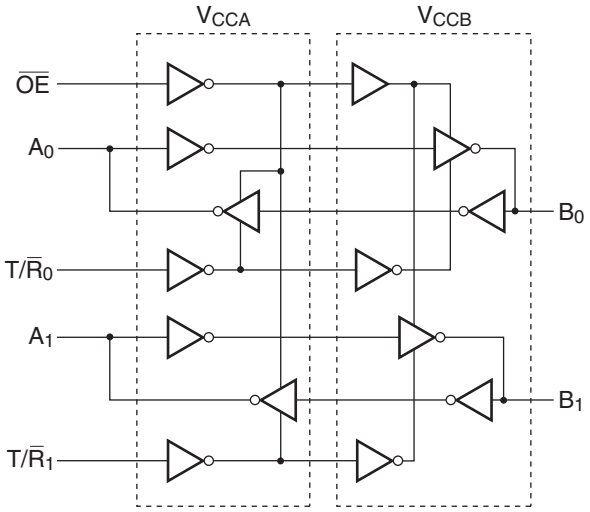
- Bi-directional interface between any 2 levels from 1.1V to 3.6V
- Fully configurable: Inputs track V_{CC} level
- Non-preferential power-up sequencing; either V_{CC} may be powered-up first
- Outputs remain in 3-STATE until active V_{CC} level is reached
- Outputs switch to 3-STATE if either V_{CC} is at GND
- Power-off protection
- Control inputs ($T/\overline{R}_n$, $\overline{OE}$) levels are referenced to V_{CCA} voltage
- Packaged in the Chipscale MicroPak10 (1.6mm x 2.1mm)
- ESD protections exceeds:
  - 4kV HBM ESD (per JESD22-A114 & Mil Std 883e 3015.7)
  - 8kV HBM I/O to GND ESD (per JESD22-A114 & Mil Std 883e 3015.7)
  - 1kV CDM ESD (per ESD STM 5.3)
  - 200V MM ESD (per JESD22-A115 & ESD STM5.2)

Ordering Information

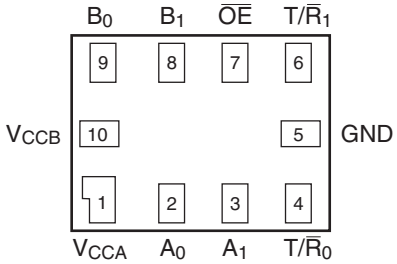
Order Number	Package Number	Pb-Free	Package Description
FXL2TD245L10X	MAC010A	Yes	10-Lead MicroPak, 1.6mm x 2.1mm

Pb-Free package per JEDEC J-STD-020B.

Functional Diagram



Connection Diagram



(Top View)

Pin Assignment

Pin Number	Terminal Name
1	V_{CCA}
2	A_0
3	A_1
4	T/R_0
5	GND
6	T/R_1
7	$\overline{OE}$
8	B_1
9	B_0
10	V_{CCB}

Pin Descriptions

Pin Names	Description
$\overline{OE}$	Output Enable Input
$T/\overline{R}_n$	Transmit/Receive Inputs
A_n	Side A Inputs or 3-STATE Outputs
B_n	Side B Inputs or 3-STATE Outputs
V_{CCA}	Side A Power Supply
V_{CCB}	Side B Power Supply

Truth Table

Inputs			Outputs
$\overline{OE}$	$T/\overline{R}_0$	$T/\overline{R}_1$	
L	L	X	B_0 Data to A_0 Output
L	H	X	A_0 Data to B_0 Output
L	X	L	B_1 Data to A_1 Output
L	X	H	A_1 Data to B_1 Output
H	X	X	3-STATE

H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care

Power-Up/Power-Down Sequencing

FXL translators offer an advantage in that either V_{CC} may be powered up first. This benefit derives from the chip design. When either V_{CC} is at 0 volts, outputs are in a HIGH-Impedance state. The control inputs ($T/\overline{R}_n$ and $\overline{OE}$) are designed to track the V_{CCA} supply. A pull-up resistor tying $\overline{OE}$ to V_{CCA} should be used to ensure that bus contention, excessive currents, or oscillations do not occur during power-up/power-down. The size of the pull-up resistor is based upon the current-sinking capability of the $\overline{OE}$ driver.

The recommended power-up sequence is the following:

1. Apply power to either V_{CC}.
2. Apply power to the $T/\overline{R}_n$ inputs (Logic HIGH for A-to-B operation; Logic LOW for B-to-A operation) and to the respective data inputs (A Port or B Port). This may occur at the same time as Step 1.
3. Apply power to other V_{CC}.
4. Drive the $\overline{OE}$ input LOW to enable the device.

The recommended power-down sequence is the following:

1. Drive $\overline{OE}$ input HIGH to disable the device.
2. Remove power from either V_{CC}.
3. Remove power from other V_{CC}.

Absolute Maximum Ratings

The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the Electrical Characteristics tables are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Symbol	Parameter	Rating
V_{CCA}, V_{CCB}	Supply Voltage	-0.5V to +4.6V
V_I	DC Input Voltage	
	I/O Port A	-0.5V to +4.6V
	I/O Port B	-0.5V to +4.6V
	Control Inputs ($T/\overline{R}_n$, $\overline{OE}$)	-0.5V to +4.6V
V_O	Output Voltage(1)	
	Outputs 3-STATE	-0.5V to +4.6V
	Outputs Active (A_n)	-0.5V to V_{CCA} + 0.5V
	Outputs Active (B_n)	-0.5V to V_{CCB} + 0.5V
I_{IK}	DC Input Diode Current @ V_I < 0V	-50mA
I_{OK}	DC Output Diode Current @	
	V_O < 0V	-50mA
	V_O > V_{CC}	+50mA
I_{OH} / I_{OL}	DC Output Source/Sink Current	-50mA / +50mA
I_{CC}	DC V_{CC} or Ground Current per Supply Pin	±100mA
T_{STG}	Storage Temperature Range	-65°C to +150°C

Recommended Operating Conditions(2)

Symbol	Parameter	Rating
V_{CCA} or V_{CCB}	Power Supply Operating	1.1V to 3.6V
	Input Voltage	
	Port A	0.0V to 3.6V
	Port B	0.0V to 3.6V
	Control Inputs ($T/\overline{R}_n$, $\overline{OE}$)	0.0V to V_{CCA}
	Output Current in I_{OH}/I_{OL} with V_{CC} @	
	3.0V to 3.6V	±24mA
	2.3V to 2.7V	±18mA
	1.65V to 1.95V	±6mA
	1.4V to 1.65V	±2mA
	1.1V to 1.4V	±0.5mA
T_A	Free Air Operating Temperature	-40°C to +85°C
$\Delta t/\Delta V$	Maximum Input Edge Rate $V_{CCA/B}$ = 1.1V to 3.6V	10ns/V

Notes:

1. I_O Absolute Maximum Rating must be observed.
2. All unused inputs and input/output pins must be held at V_{CCI} or GND.

DC Electrical Characteristics

Symbol	Parameter	Conditions	V_{CCI} (V)	V_{CCO} (V)	Min.	Max.	Units
V_{IH}	High Level Input Voltage[3]	Data Inputs A_n, B_n	2.7–3.6	1.1–3.6	2.0		V
			2.3–2.7		1.6		
			1.65–2.3		0.65 x V_{CCI}		
			1.4–1.65		0.65 x V_{CCI}		
			1.1–1.4		0.9 x V_{CCI}		
		Control Pins $\overline{OE}$, T/$\overline{R}_n$ (Referenced to V_{CCA})	2.7–3.6	1.1–3.6	2.0		
			2.3–2.7		1.6		
			1.65–2.3		0.65 x V_{CCA}		
			1.4–1.65		0.65 x V_{CCA}		
			1.1–1.4		0.9 x V_{CCA}		
V_{IL}	Low Level Input Voltage[3]	Data Inputs A_n, B_n	2.7–3.6	1.1–3.6		0.8	V
			2.3–2.7			0.7	
			1.65–2.3			0.35 x V_{CCI}	
			1.4–1.65			0.35 x V_{CCI}	
			1.1–1.4			0.1 x V_{CCI}	
		Control Pins $\overline{OE}$, T/$\overline{R}_n$ (Referenced to V_{CCA})	2.7–3.6	1.1–3.6		0.8	
			2.3–2.7			0.7	
			1.65–2.3			0.35 x V_{CCA}	
			1.4–1.65			0.35 x V_{CCA}	
			1.1–1.4			0.1 x V_{CCA}	
V_{OH}	High Level Output Voltage[4]	I_{OH} = -100µA	1.1–3.6	1.1–3.6	V_{CC0}–0.2		V
		I_{OH} = -12mA	2.7	2.7	2.2		
		I_{OH} = -18mA	3.0	3.0	2.4		
		I_{OH} = -24mA	3.0	3.0	2.2		
		I_{OH} = -6mA	2.3	2.3	2.0		
		I_{OH} = -12mA	2.3	2.3	1.8		
		I_{OH} = -18mA	2.3	2.3	1.7		
		I_{OH} = -6mA	1.65	1.65	1.25		
		I_{OH} = -2mA	1.4	1.4	1.05		
		I_{OH} = -0.5mA	1.1	1.1	0.75 x V_{CC0}		
V_{OL}	Low Level Output Voltage[4]	I_{OL} = 100µA	1.1–3.6	1.1- 3.6		0.2	V
		I_{OL} = 12mA	2.7	2.7		0.4	
		I_{OL} = 18mA	3.0	3.0		0.4	
		I_{OL} = 24mA	3.0	3.0		0.55	
		I_{OL} =12mA	2.3	2.3		0.4	
		I_{OL} = 18mA	2.3	2.3		0.6	
		I_{OL} = 6mA	1.65	1.65		0.3	
		I_{OL} = 2mA	1.4	1.4		0.35	
		I_{OL} = 0.5mA	1.1	1.1		0.3 x V_{CC0}	
I_I	Input Leakage Current Control Pins	V_I = V_{CCA} or GND	1.1–3.6	3.6		±1.0	µA

DC Electrical Characteristics (Continued)

Symbol	Parameter	Conditions	V_{CCI} (V)	V_{CCO} (V)	Min.	Max.	Units
I_{OFF}	Power Off Leakage Current	A_n, V_I or V_O = 0V to 3.6V	0	3.6		±10.0	µA
		B_n, V_I or V_O = 0V to 3.6V	3.6	0		±10.0	
I_{OZ}	3-STATE Output Leakage(5) $0 \le V_O \le 3.6V$ $V_I = V_{IH}$ or V_{IL}	A_n, B_n $\overline{OE} = V_{IH}$	3.6	3.6		±10.0	µA
		B_n, $\overline{OE}$ = Don't Care	0	3.6		+10.0	
		A_n, $\overline{OE}$ = Don't Care	3.6	0		+10.0	
$I_{CCA/B}$	Quiescent Supply Current(6)	$V_I = V_{CCI}$ or GND; $I_O = 0$	1.1–3.6	1.1–3.6		20.0	µA
I_{CCZ}	Quiescent Supply Current(6)	$V_I = V_{CCI}$ or GND; $I_O = 0$	1.1–3.6	1.1–3.6		20.0	µA
I_{CCA}	Quiescent Supply Current	$V_I = V_{CCA}$ or GND; $I_O = 0$	0	1.1–3.6		-10.0	µA
		$V_I = V_{CCA}$ or GND; $I_O = 0$	1.1–3.6	0		10.0	µA
I_{CCB}	Quiescent Supply Current	$V_I = V_{CCB}$ or GND; $I_O = 0$	1.1–3.6	0		-10.0	µA
		$V_I = V_{CCB}$ or GND; $I_O = 0$	0	1.1–3.6		10.0	µA
$\Delta I_{CCA/B}$	Increase in I_{CC} per Input; Other Inputs at V_{CC} or GND	V_{IH} = 3.0	3.6	3.6		500	µA

Notes:

3. V_{CCI} = the V_{CC} associated with the data input under test.
4. V_{CCO} = the V_{CC} associated with the output under test.
5. Don't Care = Any valid logic level.
6. Reflects current per supply, V_{CCA} or V_{CCB}.

AC Electrical Characteristics

V_{CCA} = 3.0V to 3.6V

Symbol	Parameter	T_A = -40°C to +85°C										Units
		V_{CCB} = 3.0V to 3.6V		V_{CCB} = 2.3V to 2.7V		V_{CCB} = 1.65V to 1.95V		V_{CCB} = 1.4V to 1.6V		V_{CCB} = 1.1V to 1.3V		
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t_{PLH}, t_{PHL}	Propagation Delay A to B	0.2	3.5	0.3	3.9	0.5	5.4	0.6	6.8	1.4	22.0	ns
	Propagation Delay B to A	0.2	3.5	0.2	3.8	0.3	4.0	0.5	4.3	0.8	13.0	
t_{PZH}, t_{PZL}	Output Enable $\overline{OE}$ to B	0.5	4.0	0.7	4.4	1.0	5.9	1.0	6.4	1.5	17.0	ns
	Output Enable $\overline{OE}$ to A	0.5	4.0	0.5	4.0	0.5	4.0	0.5	4.0	0.5	4.0	
t_{PHZ}, t_{PLZ}	Output Disable $\overline{OE}$ to B	0.2	3.8	0.2	4.0	0.7	4.8	1.5	6.2	2.0	17.0	ns
	Output Disable $\overline{OE}$ to A	0.2	3.7	0.2	3.7	0.2	3.7	0.2	3.7	0.2	3.7	

V_{CCA} = 2.3V to 2.7V

Symbol	Parameter	T_A = -40°C to +85°C										Units
		V_{CCB} = 3.0V to 3.6V		V_{CCB} = 2.3V to 2.7V		V_{CCB} = 1.65V to 1.95V		V_{CCB} = 1.4V to 1.6V		V_{CCB} = 1.1V to 1.3V		
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t_{PLH}, t_{PHL}	Propagation Delay A to B	0.2	3.8	0.4	4.2	0.5	5.6	0.8	6.9	1.4	22.0	ns
	Propagation Delay B to A	0.3	3.9	0.4	4.2	0.5	4.5	0.5	4.8	1.0	7.0	
t_{PZH}, t_{PZL}	Output Enable $\overline{OE}$ to B	0.6	4.2	0.8	4.6	1.0	6.0	1.0	6.8	1.5	17.0	ns
	Output Enable $\overline{OE}$ to A	0.6	4.5	0.6	4.5	0.6	4.5	0.6	4.5	0.6	4.5	
t_{PHZ}, t_{PLZ}	Output Disable $\overline{OE}$ to B	0.2	4.1	0.2	4.3	0.7	4.8	1.5	6.7	2.0	17.0	ns
	Output Disable $\overline{OE}$ to A	0.2	4.0	0.2	4.0	0.2	4.0	0.2	4.0	0.2	4.0	

V_{CCA} = 1.65V to 1.95V

Symbol	Parameter	T_A = -40°C to +85°C										Units
		V_{CCB} = 3.0V to 3.6V		V_{CCB} = 2.3V to 2.7V		V_{CCB} = 1.65V to 1.95V		V_{CCB} = 1.4V to 1.6V		V_{CCB} = 1.1V to 1.3V		
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t_{PLH}, t_{PHL}	Propagation Delay A to B	0.3	4.0	0.5	4.5	0.8	5.7	0.9	7.1	1.5	22.0	ns
	Propagation Delay B to A	0.5	5.4	0.5	5.6	0.8	5.7	1.0	6.0	1.2	8.0	
t_{PZH}, t_{PZL}	Output Enable $\overline{OE}$ to B	0.6	5.2	0.8	5.4	1.2	6.9	1.2	7.2	1.5	18.0	ns
	Output Enable $\overline{OE}$ to A	1.0	6.7	1.0	6.7	1.0	6.7	1.0	6.7	1.0	6.7	
t_{PHZ}, t_{PLZ}	Output Disable $\overline{OE}$ to B	0.2	5.1	0.2	5.2	0.8	5.2	1.5	7.0	2.0	17.0	ns
	Output Disable $\overline{OE}$ to A	0.5	5.0	0.5	5.0	0.5	5.0	0.5	5.0	0.5	5.0	

AC Electrical Characteristics (Continued)

V_{CCA} = 1.4V to 1.6V

Symbol	Parameter	T_A = -40°C to +85°C										Units
		V_{CCB} = 3.0V to 3.6V		V_{CCB} = 2.3V to 2.7V		V_{CCB} = 1.65V to 1.95V		V_{CCB} = 1.4V to 1.6V		V_{CCB} = 1.1V to 1.3V		
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t_{PLH}, t_{PHL}	Propagation Delay A to B	0.5	4.3	0.5	4.8	1.0	6.0	1.0	7.3	1.5	22.0	ns
	Propagation Delay B to A	0.6	6.8	0.8	6.9	0.9	7.1	1.0	7.3	1.3	9.5	
t_{PZH}, t_{PZL}	Output Enable $\overline{OE}$ to B	1.1	7.5	1.1	7.6	1.3	7.7	1.4	7.9	2.0	20.0	ns
	Output Enable $\overline{OE}$ to A	1.0	7.5	1.0	7.5	1.0	7.5	1.0	7.5	1.0	7.5	
t_{PHZ}, t_{PLZ}	Output Disable $\overline{OE}$ to B	0.4	6.1	0.4	6.2	0.9	6.2	1.5	7.5	2.0	18.0	ns
	Output Disable $\overline{OE}$ to A	1.0	6.0	1.0	6.0	1.0	6.0	1.0	6.0	1.0	6.0	

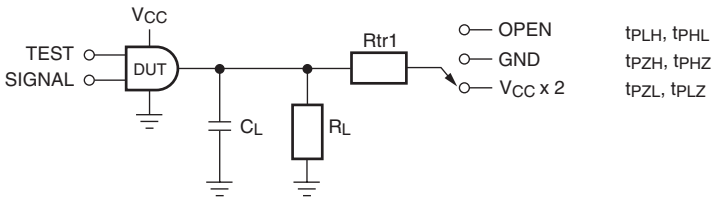
V_{CCA} = 1.1V to 1.3V

Symbol	Parameter	T_A = -40°C to +85°C										Units
		V_{CCB} = 3.0V to 3.6V		V_{CCB} = 2.3V to 2.7V		V_{CCB} = 1.65V to 1.95V		V_{CCB} = 1.4V to 1.6V		V_{CCB} = 1.1V to 1.3V		
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t_{PLH}, t_{PHL}	Propagation Delay A to B	0.8	13.0	1.0	7.0	1.2	8.0	1.3	9.5	2.0	24.0	ns
	Propagation Delay B to A	1.4	22.0	1.4	22.0	1.5	22.0	1.5	22.0	2.0	24.0	
t_{PZH}, t_{PZL}	Output Enable $\overline{OE}$ to B	1.0	12.0	1.0	9.0	2.0	10.0	2.0	11.0	2.0	24.0	ns
	Output Enable $\overline{OE}$ to A	2.0	22.0	2.0	22.0	2.0	22.0	2.0	22.0	2.0	22.0	
t_{PHZ}, t_{PLZ}	Output Disable $\overline{OE}$ to B	1.0	15.0	0.7	7.0	1.0	8.0	2.0	10.0	2.0	20.0	ns
	Output Disable $\overline{OE}$ to A	2.0	15.0	2.0	12.0	2.0	12.0	2.0	12.0	2.0	12.0	

Capacitance

Symbol	Parameter	Conditions	T_A = +25°C	Units
			Typical	
C_{IN}	Input Capacitance Control Pins ($\overline{OE}$, T/$\overline{R}$n)	V_{CCA} = V_{CCB} = 3.3V, V_I = 0V or $V_{CCA/B}$	4.0	pF
$C_{I/O}$	Input/Output Capacitance A_n, B_n Ports	V_{CCA} = V_{CCB} = 3.3V, V_I = 0V or $V_{CCA/B}$	5.0	pF
C_{PD}	Power Dissipation Capacitance	V_{CCA} = V_{CCB} = 3.3V, V_I = 0V or V_{CC}, F = 10MHz	20.0	pF

AC Loading and Waveforms

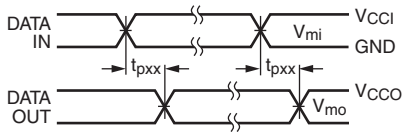


Test	Switch
t_{PLH}, t_{PHL}	OPEN
t_{PLZ}, t_{PZL}	V_{CCO} x 2 at V_{CCO} = 3.3 ± 0.3V, 2.5V ± 0.2V, 1.8V ± 0.15V, 1.5V ± 0.1V, 1.2V ± 0.1V
t_{PHZ}, t_{PZH}	GND

Figure 1. AC Test Circuit

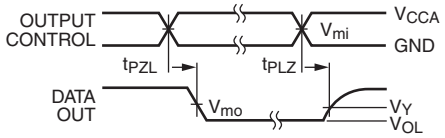
AC Load Table

V_{CCO}	C_L	R_L	Rtr1
1.2V ± 0.1V	15pF	2kΩ	2kΩ
1.5V ± 0.1V	15pF	2kΩ	2kΩ
1.8V ± 0.15V	15pF	2kΩ	2kΩ
2.5V ± 0.2V	15pF	2kΩ	2kΩ
3.3V ± 0.3V	15pF	2kΩ	2kΩ



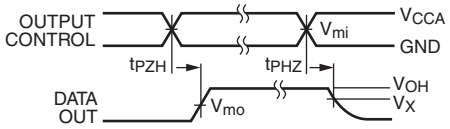
Input $t_R = t_F$ = 2.0 ns, 10% to 90%
Input $t_R = t_F$ = 2.5ns, 10% to 90%, @ V_I = 3.0V to 3.6V only

Figure 2. Waveform for Inverting and Non-Inverting Functions



Input $t_R = t_F$ = 2.0 ns, 10% to 90%
Input $t_R = t_F$ = 2.5ns, 10% to 90%, @ V_I = 3.0V to 3.6V only

Figure 3. 3-STATE Output Low Enable and Disable Times for Low Voltage Logic



Input $t_R = t_F$ = 2.0 ns, 10% to 90%
Input $t_R = t_F$ = 2.5ns, 10% to 90%, @ V_I = 3.0V to 3.6V only

Figure 4. 3-STATE Output High Enable and Disable Times for Low Voltage Logic

	V_{CC}				
Symbol	**3.3V ± 0.3V**	**2.5V ± 0.2V**	**1.8V ± 0.15V**	**1.5V ± 0.1V**	**1.2V ± 0.1V**
V_{mi}	$V_{CCI}/2$	$V_{CCI}/2$	$V_{CCI}/2$	$V_{CCI}/2$	$V_{CCI}/2$
V_{mo}	$V_{CCO}/2$	$V_{CCO}/2$	$V_{CCO}/2$	$V_{CCO}/2$	$V_{CCO}/2$
V_X	V_{OH}-0.3V	V_{OH}-0.15V	V_{OH}-0.15V	V_{OH}-0.1V	V_{OH}-0.1V
V_Y	V_{OL}+0.3V	V_{OL}+0.15V	V_{OL}+0.15V	V_{OL}+0.1V	V_{OL}+0.1V

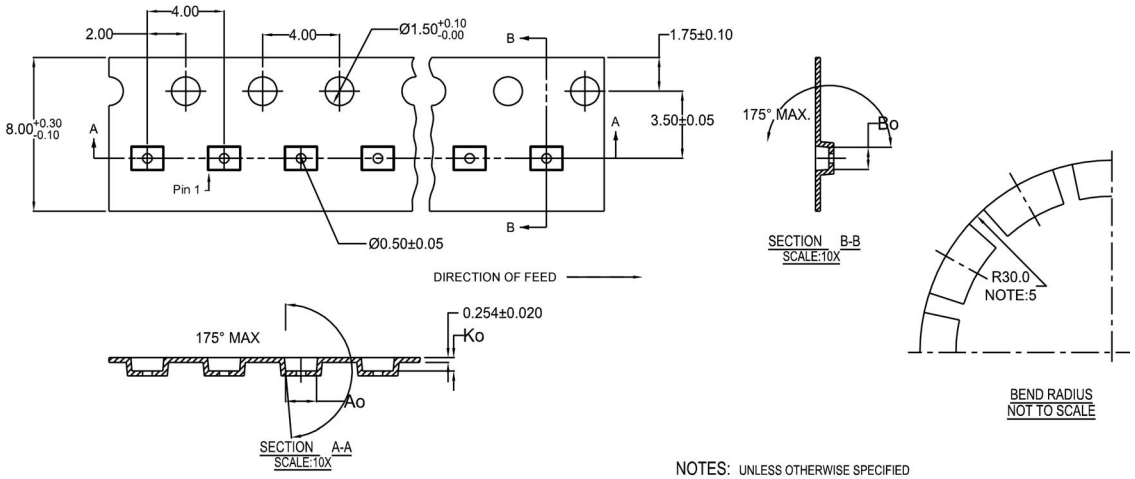
For V_{mi}: $V_{CCI} = V_{CCA}$ for Control Pins T/$\overline{R}$ and $\overline{OE}$, or $V_{CCA}/2$

Tape and Reel Specification

Tape Format for MicroPak 10

Package Designator	Tape Section	Number Cavities	Cavity Status	Cover Tape Status
L10X	Leader (Start End)	125 (typ)	Empty	Sealed
	Carrier	5000	Filled	Sealed
	Trailer (Hub End)	75 (typ)	Empty	Sealed

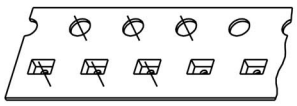
Tape Dimensions inches (millimeters)



10	300056	2.30±0.05	1.78±0.05	0.68±0.05
8	300038	1.78±0.05	1.78±0.05	0.68±0.05
6	300033	1.60±0.05	1.15±0.05	0.70±0.05

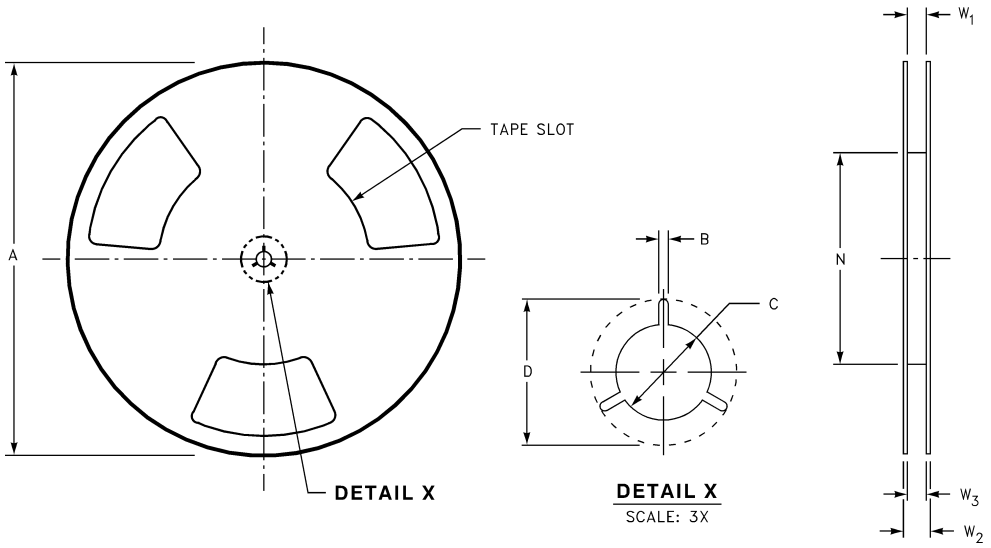
NOTES: UNLESS OTHERWISE SPECIFIED

1. ACCUMULATED 50 SPROCKETS, SPROCKET HOLE PITCH IS 200.00 ±0.30MM
2. NO INDICATED CORNER RADIUS IS 0.127MM
3. CAMBER NOT TO EXCEED 1MM IN 100MM
4. SMALLEST ALLOWABLE BENDING RADIUS
5. POCKET POSITION RELATIVE TO SPROCKET HOLE MEASURED AS TRUE POSITION OF POCKET, NOT POCKET HOLE



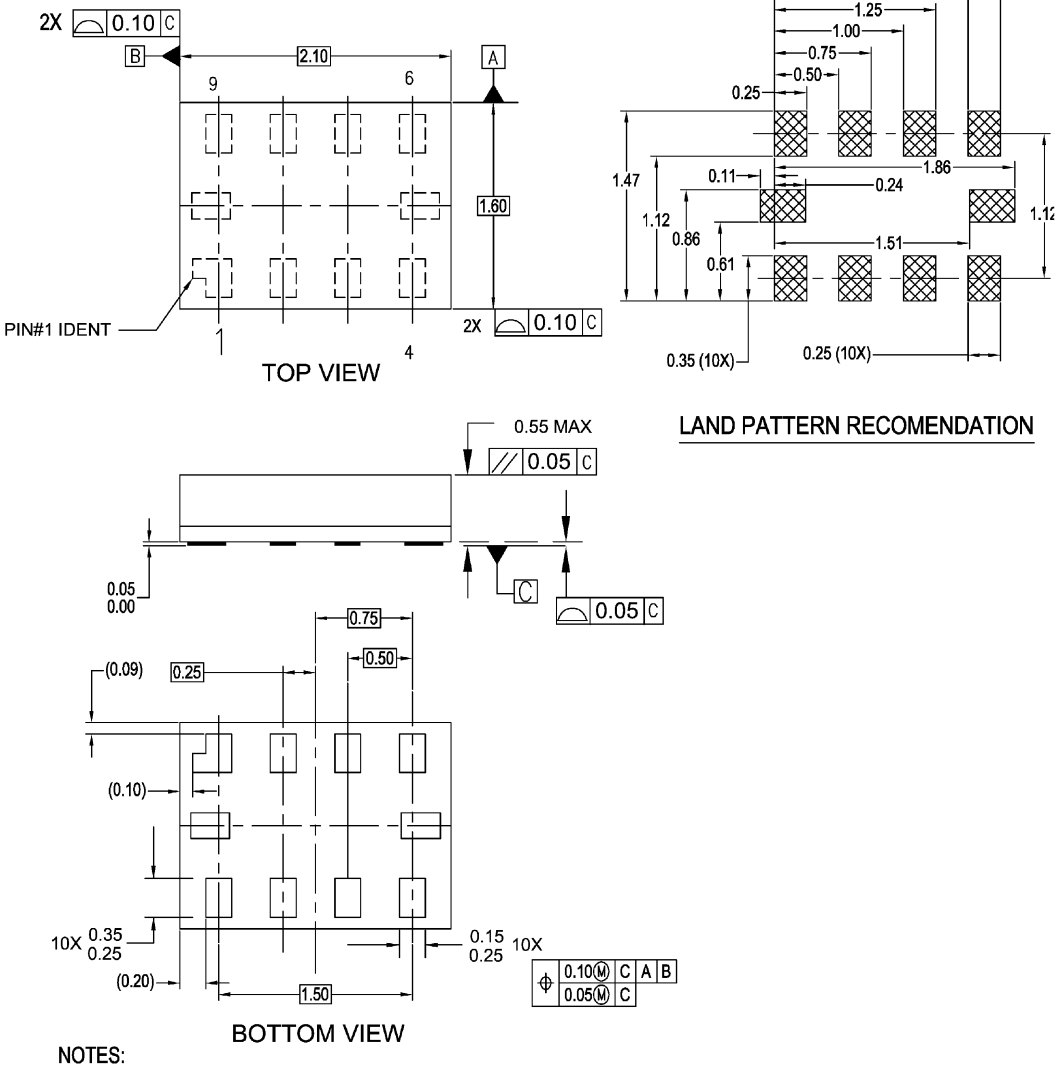
SCALE: 6X

MicroPak 10 Reel Dimensions inches (millimeters)



Tape Size	A	B	C	D	N	W1	W2	W3
8 mm	7.0 (177.8)	0.059 (1.50)	0.512 (13.00)	0.795 (20.20)	2.165 (55.00)	0.331 + 0.059/-0.000 (8.40 + 1.50/-0.00)	0.567 (14.40)	W1 + 0.078/-0.039W (W1 + 2.00/-1.00)

Physical Dimensions inches (millimeters) unless otherwise noted



NOTES:

A. PACKAGE CONFORMS TO JEDEC MO255, VARIATION UABD

B. DIMENSIONS ARE IN MILLIMETERS.

C. DIMENSIONS AND TOLERANCES CONFORMS TO ASME Y14.5M, 1994.

MAC010ARevC

Pb-Free 10-Lead MicroPak, 1.6mm x 2.1mm
Package Number MAC010A

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	MSXPro™	RapidConnect™	TINYOPTO™	
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The Power Franchise®		ScalarPump™	UHC®	
Programmable Active Droop™				

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PRODUCT STATUS DEFINITIONS

Definition of Terms

Datasheet Identification	Product Status	Definition
Advance Information	Formative or In Design	This datasheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	First Production	This datasheet contains preliminary data, and supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve design.
No Identification Needed	Full Production	This datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve design.
Obsolete	Not In Production	This datasheet contains specifications on a product that has been discontinued by Fairchild semiconductor. The datasheet is printed for reference information only.

FXL2TD245

Low Voltage Dual Supply 2-Bit Signal Translator with Configurable Voltage Supplies and Signal Levels and 3-STATE Outputs and Independent Direction Controls

Contents

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General description

The FXL2TD245 is a configurable dual-voltage-supply translator designed for both uni-directional and bi-directional voltage translation between two logic levels. The device allows translation between voltages as high as 3.6V to as low as 1.1V. The A Port tracks the V_{CCA} level, and the B Port tracks the V_{CCB} level. This allows for bi-directional voltage translation over a variety of voltage levels: 1.2V, 1.5V, 1.8V, 2.5V, and 3.3V.

The device remains in 3-STATE until both V_{CC}s reach active levels allowing either V_{CC} to be powered-up first. Internal power down control circuits place the device in 3-STATE if either V_{CC} is removed.

The Transmit/Receive ($T/\overline{R}$) input determines the direction of data flow through the device. The $\overline{OE}$ input, when HIGH, disables both the A and B Ports by placing them in a 3-STATE condition. The FXL2TD245 is designed so that the control pins ($T/\overline{R}$ and $\overline{OE}$) are supplied by V_{CCA}.

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Features

- Bi-directional interface between any 2 levels from 1.1V to 3.6V
- Fully configurable: Inputs track V_{CC} level
- Non-preferential power-up sequencing; either V_{CC} may be powered-up first
- Outputs remain in 3-STATE until active V_{CC} level is reached
- Outputs switch to 3-STATE if either V_{CC} is at GND
- Power-off protection
- Control inputs (T/$\overline{R}$n, $\overline{OE}$) levels are referenced to V_{CCA} voltage
- Packaged in the Chipscale MicroPak10 (1.6mm x 2.1mm)
- ESD protection exceeds:
  – 4kV HBM ESD
  (per JESD22-A114 & Mil Std 883e 3015.7)
  – 8kV HBM I/O to GND ESD
  (per JESD22-A114 & Mil Std 883e 3015.7)
  – 1kV CDM ESD (per ESD STM 5.3)
  – 200V MM ESD (per JESD22-A115 & ESD STM5.2)

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Product status/pricing/packaging BUY

Product	Product status	Pb-free Status	Pricing*	Package type	Leads	Packing method	Package Marking Convention**
FXL2TD245L10X	Full Production	Full Production	$0.55	MicroPak	10	TAPE REEL	Line 1: XE

* Fairchild 1,000 piece Budgetary Pricing
** A sample button will appear if the part is available through Fairchild's on-line samples program. If there is no sample button, please contact a Fairchild distributor to obtain samples

Indicates product with Pb-free second-level interconnect. For more information click here.

Package marking information for product FXL2TD245 is available. Click here for more information .

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Models

Package & leads	Condition	Temperature range	Vcc range	Software version	Revision date
HSPICE					
	Typical	-40°C to 85°C	1.1V to 3.6V	2001.4	Jul 27, 2006

MicroPak-10	Slow	-40°C to 85°C	1.1V to 3.6V	2001.4	Jul 27, 2006
	Fast	-40°C to 85°C	1.1V to 3.6V	2001.4	Jul 27, 2006

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Qualification Support

Click on a product for detailed qualification data

Product
FXL2TD245L10X

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