

1.1 Scope.

This specification covers the detail requirements for a precision 10-bit resolution current output D/A converter with an internal precision reference.

1.2 Part Number.

The complete part number per Table 1 of this specification is as follows:

Device	Part Number
-1	AD561SD/883B
-2	AD561TD/883B

1.2.3 Case Outline.

See Appendix 1 of General Specification ADI-M-1000; package outline: D-16.

1.3 Absolute Maximum Ratings. ($T_A = +25^\circ\text{C}$ unless otherwise noted)

Supply Voltage (V_{CC})	+16.5V
Supply Voltage (V_{EE})	-16.5V
Digital Input Voltage (V_{IN})	V_{CC} to Ground
Output Voltage Compliance (V_{OUT})	-2V to +10V
10V Span Resistor to Ground	V_{CC} to V_{EE}
Bipolar Offset Resistor to Ground	V_{CC} to V_{EE}
Junction Temperature (T_J)	175°C
Maximum Power Dissipation	500mW
Storage Temperature Range	-65°C to +150°C
Lead Temperature (Soldering 10sec)	+300°C

1.5 Thermal Characteristics.

Thermal Resistance $\theta_{JC} = 30^\circ\text{C/W}$
 $\theta_{JA} = 100^\circ\text{C/W}$

AD561 — SPECIFICATIONS

Table 1.

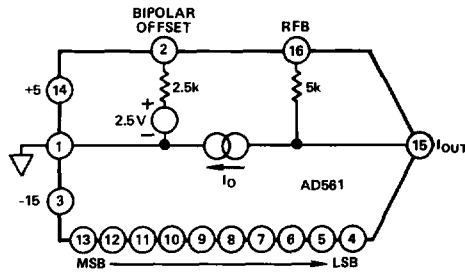
Test	Symbol	Device	Design Limit (@ +25°C)	Sub Group 1	Sub Group 2, 3	Sub Group 4	Test Condition ¹	Units
Relative Accuracy	RA	-1	1/2	1/2			All Bits with + Errors On	± LSB max
		-2	1/4	1/2		1/4	All Bits with - Errors On	
Differential Nonlinearity	DNL	-1	1	1	1		Major Carry Transitions	± LSB max
		-2	1/2	1	1	1/2		
Gain Error	A _E	-1, 2	0.5	0.5			With Fixed 25Ω Resistor ²	± % of FS max
Gain Error Temperature Coefficient	TCA _E	-1			60			± ppm of FS/°C
		-2			30			
Unipolar Offset Error	V _{OS}	-1, 2	0.05	0.05			See Note 2	± % of FS max
Unipolar Error Temperature Coefficient	TCV _{OS}	-1			10			± ppm of FS/°C max
		-2			5			
Bipolar Zero Error	B _{PZE}	-1, 2	3.5	3.5			With 10Ω Resistor	± LSB max
B/P Zero Error Temperature Coefficient	TCB _{PZE}	-1			20			± ppm of FS/°C max
		-2			10			
Output Current	I _{OUT}	-1, 2	1.5	1.5			Digital Inputs at Logic "1"	- mA min
			2.4	2.4			V _{CC} = +5V	- mA max
Power Supply Gain Sensitivity	P _{SS1}	-1, 2	10	10			V _{CC1} + 4.5V to + 5.5 V dc V _{CC2} + 13.5V to + 16.5V dc	± ppm of FS/%
	P _{SS2}	-1, 2	25	25			V _{EE2} - 10.8V to - 13.2V dc V _{EE3} - 13.2V dc to - 16.5V dc	± ppm of FS/%
Power Supply Current ²	I _{CC}	-1, 2	10	10			V _{CC1} + 4.5V dc to + 16.5V dc	+ mA max
	I _{EE}	-1, 2	16	16			V _{EE2} - 10.8V dc to - 16.5V dc	- mA max
Power Dissipation	P _D	-1, 2	500	500				mW max
Digital Input High Voltage	V _{IH}	-1, 2	2.0	2.0				+ V min
Digital Input Low Voltage	V _{IL}	-1, 2	0.8	0.8				+ V max
Digital Input High Current	I _{IH}	-1, 2	100	100			Digital "1" = 15V	± nA max
Digital Input Low Current	I _{IL}	-1, 2	25	25			Digital "0" = 0V	± μA max

NOTES

¹T_A = 25°C, V_{CC} = +5V dc, V_{EE} = -15V dc unless otherwise specified.

²Also tested in CMOS mode. V_{CC} = +15V dc, V_{EE} = -15V dc, V_{IH} = 10.5V dc, V_{IL} = 4.5V dc.

3.2.1 Functional Block Diagram and Terminal Assignments.



3.2.4 Microcircuit Technology Group.

This microcircuit is covered by technology group (56).

4.2.1 Life Test/Burn-In Circuit.

Steady state life test is per MIL-STD-883 Method 1005. Burn-in is per MIL-STD-883 Method 1015 test condition (B).

