HARRIS SEMICONDUCTOR

CD74FCT843A, CD74FCT844A

BiCMOS FCT Interface Logic, 9-Bit Transparent Latches, Three-State

January 1997

NOT RECOMMENDED FOR NEW DESIGNS
Use CMOS Technology

Features

- Buffered Inputs
- Typical Propagation Delay: 6.8ns at V_{CC} = 5V, T_A = 25°C, C_L = 50pF (FCT843A)
- CD74FCT843A
  - Noninverting
- CD74FCT844A
  - Inverting
- SCR Latchup Resistant BiCMOS Process and Circuit Design
- Speed of Bipolar FAST™/AS/S
- 48mA Output Sink Current
- Output Voltage Swing Limited to 3.7V at V_{CC} = 5V
- Controlled Output Edge Rates
- Input/Output Isolation to V_{CC}
- BiCMOS Technology with Low Quiescent Power

Ordering Information

PART NUMBER	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
CD74FCT844AEN	0 to 70	24 Ld PDIP	E24.3
CD74FCT843AM	0 to 70	24 Ld SOIC	M24.3

NOTE: When ordering the suffix M package, use the entire part number. Add the suffix 96 to obtain the variant in the tape and reel.

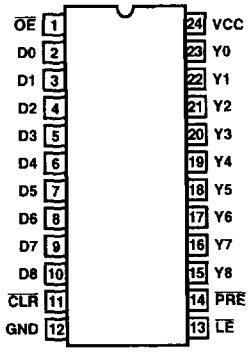
Description

The CD74FCT843A and CD74FCT844A nine bit transparent latches use a small geometry BiCMOS technology. The output stage is a combination of bipolar and CMOS transistors that limits the output HIGH level to two diode drops below V_{CC}. This resultant lowering of output swing (0V to 3.7V) reduces power bus ringing (a source of EMI) and minimizes V_{CC} bounce and ground bounce and their effects during simultaneous output switching. The output configuration also enhances switching speed and is capable of sinking 48 milliamperes.

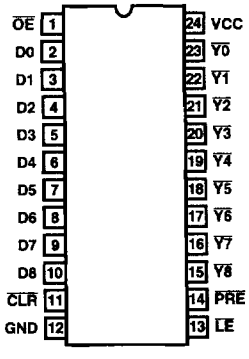
The CD74FCT843A and CD74FCT844A outputs are transparent to the inputs when the Latch Enable ($\overline{LE}$) is HIGH. When the Latch Enable ($\overline{LE}$) goes LOW, the data is latched. The Output Enable ($\overline{OE}$) controls the three state outputs. When the Output Enable ($\overline{OE}$) is HIGH, the outputs are in the high impedance state. The latch operation is independent of the state of the Output Enable. These devices, having Preset ($\overline{PRE}$) and Clear ($\overline{CLR}$), are ideal for parity bus interfacing. When $\overline{PRE}$ is low, the outputs are HIGH if $\overline{OE}$ is LOW. $\overline{PRE}$ overrides $\overline{CLR}$. When $\overline{CLR}$ is LOW, the outputs are LOW if $\overline{OE}$ is LOW. When $\overline{CLR}$ is HIGH, data can be entered into the latch.

Pinouts

CD74FCT843A
(SOIC)
TOP VIEW



CD74FCT844A
(PDIP)
TOP VIEW

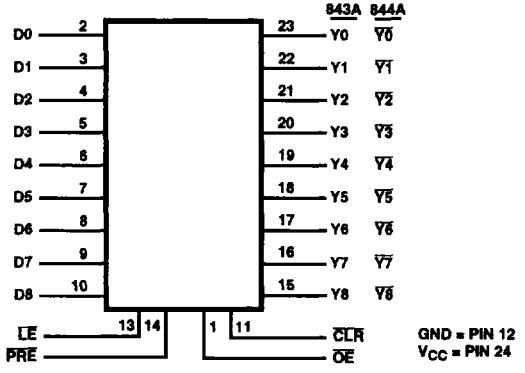


CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.

File Number **2396.2**

FAST™ is a trademark of Fairchild Semiconductor.

Functional Diagram



TRUTH TABLE (Note 1)

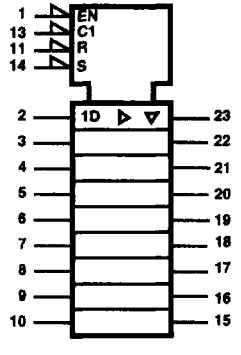
INPUTS						OUTPUTS	
$\overline{CLR}$	$\overline{PRE}$	$\overline{OE}$	$\overline{LE}$	843A Dn	844A Dn	Yn	FUNCTION
H	H	H	X	X	X	Z	High Z
H	H	H	L	X	X	Z	Latched (High Z)
H	H	L	H	L	H	L	Transparent
H	H	L	H	H	L	H	Transparent
H	H	L	L	X	X	NC	Latched
H	L	L	X	X	X	H	Preset
L	H	L	X	X	X	L	Clear
L	L	L	X	X	X	H	Preset
L	H	H	L	X	X	Z	Latched (High Z)
H	L	H	L	X	X	Z	Latched (High Z)

NOTE:

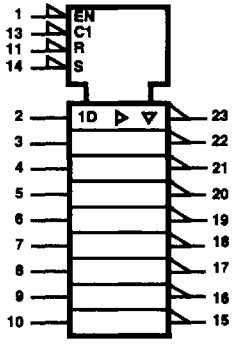
1. H= HIGH Voltage Level
   L = LOW Voltage Level
   X = Immaterial
   NC = No Change
   Z = High Impedance

IEC Logic Symbol

CD74FCT843A



CD74FCT844A



Absolute Maximum Ratings

DC Supply Voltage (V_{CC}) ..... -0.5V to 6V
DC Diode Current, I_{IK} (For V_I < -0.5V) ..... -20mA
DC Output Diode Current, I_{OK} (for V_O < -0.5V) ..... -50mA
DC Output Sink Current per Output Pin, IO 70mA
DC Output Source Current per Output Pin, IO ..... -30mA
DC V_{CC} Current (I_{CC}) 237mA
DC Ground Current (I_{GND}) 453mA

Thermal Information

Thermal Resistance (Typical, Note 2) θ_{JA} (°C/W)
PDIP Package 75
SOIC Package 75
Maximum Junction Temperature ..... 150°C
Maximum Storage Temperature Range ..... -65°C to 150°C
Maximum Lead Temperature (Soldering 10s) ..... 300°C
(SOIC-Lead Tips Only)

Operating Conditions

Operating Temperature Range, T_A ..... 0°C to 70°C
Supply Voltage Range, V_{CC} ..... 4.75V to 5.25V
DC Input Voltage, V_I ..... 0 to V_{CC}
DC Output Voltage, V_O ..... 0 to ≤ V_{CC}
Input Rise and Fall Slew Rate, dt/dv ..... 0 to 10ns/V

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

2. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications Commercial Temperature Range 0°C to 70°C, V_{CC} Max = 5.25V, V_{CC} Min = 4.75V

PARAMETER	SYMBOL	TEST CONDITIONS		V_{CC} (V)	AMBIENT TEMPERATURE (T_A)				UNITS
					25°C		0°C TO 70°C		
		V_I (V)	I_O (mA)		MIN	MAX	MIN	MAX	
High Level Input Voltage	V_{IH}			4.75 to 5.25	2	-	2	-	V
Low Level Input Voltage	V_{IL}			4.75 to 5.25	-	0.8	-	0.8	V
High Level Output Voltage	V_{OH}	V_{IH} or V_{IL}	-15	Min	2.4	-	2.4	-	V
Low Level Output Voltage	V_{OL}	V_{IH} or V_{IL}	48	Min	-	0.55	-	0.55	V
High Level Input Current	I_{IH}	V_{CC}		Max	-	0.1	-	1	µA
Low Level Input Current	I_{IL}	GND		Max	-	-0.1	-	-1	µA
Three-State Leakage Current	I_{OZH}	V_{CC}		Max	-	0.5	-	10	µA
	I_{OZL}	GND		Max	-	-0.5	-	-10	µA
Input Clamp Voltage	V_{IK}	V_{CC} or GND	-18	Min	-	-1.2	-	-1.2	V
Short Circuit Output Current (Note 3)	I_{OS}	V_O = 0 V_{CC} or GND		Max	-75	-	-75	-	mA
Quiescent Supply Current, MSI	I_{CC}	V_{CC} or GND	0	Max	-	8	-	80	µA
Additional Quiescent Supply Current per Input Pin TTL Inputs High, 1 Unit Load	ΔI_{CC}	3.4V (Note 4)		Max	-	1.6	-	1.6	mA

NOTES:

3. *Not more than one output should be shorted at one time. Test duration should not exceed 100ms.*
4. Inputs that are not measured are at VCC or GND.
5. FCT Input Loading: All inputs are 1 unit load. Unit load is ΔI_{CC} limit specified in Static Characteristics Chart, e.g., 1.6mA Max. @ 70°C.

Switching Specifications Over Operating Range FCT Series t_r, t_f = 2.5ns, C_L = 50pF, R_L (Figure 1)

PARAMETER		SYMBOL	V_{CC} (V)	25°C TYP	0°C TO 70°C MIN	0°C TO 70°C MAX	UNITS
Propagation Delays							
Data to Outputs	CD74FCT843A	t_{PLH}, t_{PHL}	5 (Note 6)	6.8	1.5	9	ns
	CD74FCT844A	t_{PLH}, t_{PHL}	5	7.5	1.5	10	ns
$\overline{LE}$ to Outputs		t_{PLH}, t_{PHL}	5	9	1.5	12	ns
$\overline{PRE}$ to Outputs		t_{PLH}	5	9	1.5	12	ns
$\overline{CLR}$ to Outputs		t_{PHL}	5	9.8	1.5	13	ns
Output Enable Times		t_{PZL}, t_{PZH}	-	10.5	1.5	14	ns
Output Disable Times		t_{PLZ}, t_{PHZ}	-	6	1.5	8	ns
Power Dissipation Capacitance		C_{PD} (Note 7)	-	-	-	-	pF
Minimum (Valley) V_{OHV} During Switching of Other Outputs (Output Under Test Not Switching)		V_{OHV}	5	0.5	-	-	V
Maximum (Peak) V_{OLP} During Switching of Other Outputs (Output Under Test Not Switching)		V_{OLP}	5	1	-	-	V
Input Capacitance		C_I	-	-	-	10	pF
Three-State Output Capacitance		C_O	-	-	-	15	pF

NOTES:

6. 5V: Minimum is at 5.25V for 0°C to 70°C, Maximum is at 4.75V for 0°C to 70°C, Typical is at 5V.
7. C_{PD}, measured per flip-flop, is used to determine the dynamic power consumption.
   P_D (per package) = V_{CC} I_{CC} + $\Sigma(V_{CC}^2 f_i C_{PD} + V_O^2 f_O C_L + V_{CC} \Delta I_{CC} D)$ where:
   V_{CC} = supply voltage
   ΔI_{CC} = flow through current x unit load
   C_L = output load capacitance
   D = duty cycle of input high
   f_O = output frequency
   f_i = input frequency

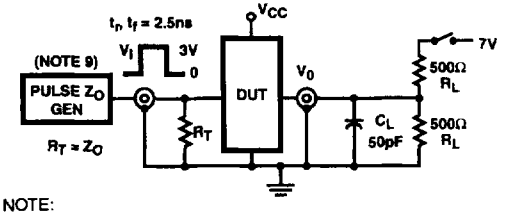
Prerequisite for Switching

PARAMETER	SYMBOL	V_{CC} (V)	25°C TYP	0°C TO 70°C MIN	0°C TO 70°C MAX	UNITS
Setup Time, Data to $\overline{LE}$	t_{SU}	5 (Note 8)	-	2.5	-	ns
Hold Time, Data to $\overline{LE}$	t_H	5	-	2.5	-	ns
$\overline{LE}$ Pulse Width	t_W	5	-	4	-	ns
$\overline{PRE}$, $\overline{CLR}$ Pulse Width	t_W	5	-	8	-	ns
$\overline{PRE}$, $\overline{CLR}$ Recovery Time	t_{REC}	5	-	14	-	ns

NOTE:

8. Minimum is at 4.75V for 0°C to 70°C, Typical is at 5V.

Test Circuits and Waveforms



NOTE:

9. Pulse Generator for All Pulses: Rate ≤ 1.0MHz; Z_{OUT} ≤ 50Ω; t_f, t_r ≤ 2.5ns.

FIGURE 1. TEST CIRCUIT

SWITCH POSITION

TEST	SWITCH
t_{PLZ}, t_{PZL}, Open Drain	Closed
t_{PHZ}, t_{PZH}, t_{PLH}, t_{PHL}	Open

DEFINITIONS:

C_L = Load capacitance, includes jig and probe capacitance.

R_T = Termination resistance, should be equal to Z_{OUT} of the Pulse Generator.

V_{IN} = 0V to 3V.

Input: $t_r = t_f$ = 2.5ns (10% to 90%), unless otherwise specified

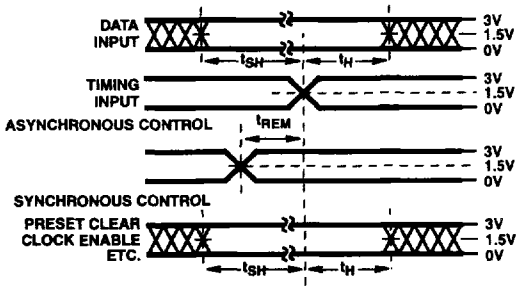


FIGURE 2. SETUP, HOLD, AND RELEASE TIMING

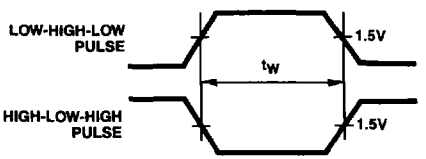


FIGURE 3. PULSE WIDTH

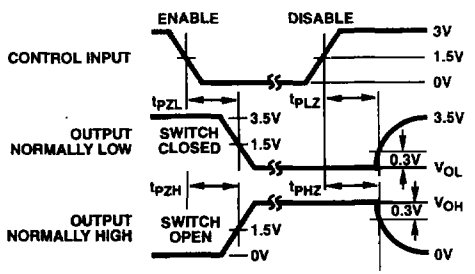


FIGURE 4. ENABLE AND DISABLE TIMING

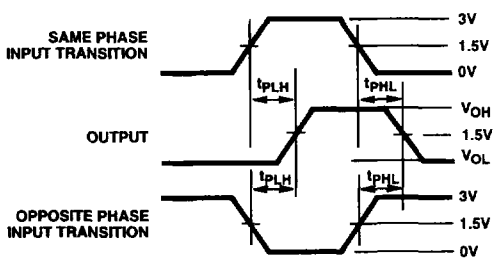
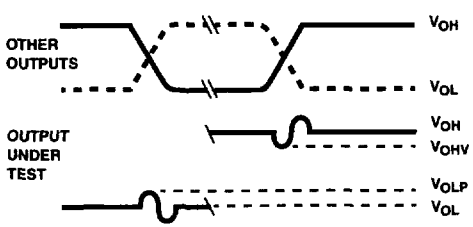


FIGURE 5. PROPAGATION DELAY



NOTES:

10. V_{OLP} is measured with respect to a ground reference near the output under test. V_{OHV} is measured with respect to V_{OH}.
11. Input pulses have the following characteristics: P_{RR} ≤ 1MHz, t_r = 2.5ns, t_f = 2.5ns, skew 1ns.
12. R.F. fixture with 700MHz design rules required. IC should be soldered into test board and bypassed with 0.1µF capacitor. Scope and probes require 700MHz bandwidth.

FIGURE 6. SIMULTANEOUS SWITCHING TRANSIENT WAVEFORMS