DATA SHEET



MOS FIELD EFFECT TRANSISTOR μ PA2723T1A

SWITCHING N-CHANNEL POWER MOSFET

DESCRIPTION

The μ PA2723T1A is N-channel MOSFET designed for low side device of synchronous rectifier DC/DC converter.

FEATURES

• Low on-state resistance

 $R_{DS(on)1} = 2.5 \text{ m}\Omega \text{ MAX.} \text{ (Vgs} = 10 \text{ V, I}_D = 17 \text{ A)}$

 $R_{DS(on)2} = 3.5 \text{ m}\Omega \text{ MAX.} \text{ (Vgs = 4.5 V, ID = 17 A)}$

- Built-in gate protection diode
- Thin type surface mount package with heat spreader (8-pin HVSON)
- RoHS Compliant

ABSOLUTE MAXIMUM RATINGS (TA = 25°C, All terminals are connected.)

Drain to Source Voltage (Vgs = 0 V)	VDSS	30	V
Gate to Source Voltage (VDS = 0 V)	Vgss	±20	V
Drain Current (DC)	ID(DC)	±33	Α
Drain Current (pulse) Note1	D(pulse)	±200	Α
Total Power Dissipation Note2	P _{T1}	1.5	W
Total Power Dissipation (PW =10 sec) Note2	P _{T2}	4.6	W
Channel Temperature	Tch	150	°C
Storage Temperature	Tstg	-55 to +150	°C
Single Avalanche Current Note3	las	33	Α
Single Avalanche Energy Note3	Eas	109	mJ

THERMAL RESISTANCE

<R>

Channel to Ambient Thermal Resistance Note2 Rth(ch-A) 83.3 °C/W Channel to Case (Drain) Thermal Resistance Rth(ch-C) 1.5 °C/W

Notes 1. PW \leq 10 μ s, Duty Cycle \leq 1%

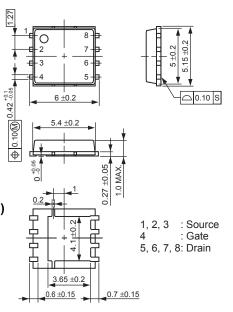
- 2. Mounted on a glass epoxy board of 25.4 mm x 25.4 mm x 0.8 mm
- 3. Starting T_{ch} = 25°C, V_{DD} = 15 V, R_G = 25 Ω , V_{GS} = 20 \rightarrow 0 V, L = 100 μ H

Remark The diode connected between the gate and source of the transistor serves as a protector against ESD. When this device actually used, an additional protection circuit is externally required if a voltage exceeding the rated voltage may be applied to this device.

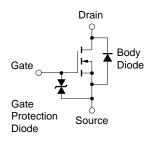
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PACKAGE DRAWING (Unit: mm)



EQUIVALENT CIRCUIT



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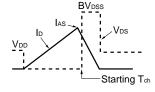
ELECTRICAL CHARACTERISTICS (TA = 25°C, All terminals are connected.)

CHARACTERISTICS	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Zero Gate Voltage Drain Current	IDSS	V _{DS} = 30 V, V _{GS} = 0 V			10	μΑ
Gate Leakage Current	Igss	V _{GS} = ±20 V, V _{DS} = 0 V			±10	μΑ
Gate to Source Cut-off Voltage	V _{GS(off)}	V _{DS} = 10 V, I _D = 1 mA	1.0		2.5	V
Forward Transfer Admittance Note	yfs	V _{DS} = 10 V, I _D = 17 A	17			S
Drain to Source On-state Resistance Note	RDS(on)1	V _{GS} = 10 V, I _D = 17 A		1.9	2.5	mΩ
	RDS(on)2	V _{GS} = 4.5 V, I _D = 17 A		2.6	3.5	mΩ
Input Capacitance	Ciss	V _{DS} = 10 V,		8100		pF
Output Capacitance	Coss	V _{GS} = 0 V,		1290		pF
Reverse Transfer Capacitance	Crss	f = 1 MHz		610		pF
Turn-on Delay Time	t _{d(on)}	V _{DD} = 15 V, I _D = 17 A,		30		ns
Rise Time	tr	V _{GS} = 10 V,		40		ns
Turn-off Delay Time	t _{d(off)}	R _G = 10 Ω		160		ns
Fall Time	tf			55		ns
Total Gate Charge	Q _G	V _{DD} = 15 V,		64		nC
Gate to Source Charge	Qgs	V _{GS} = 5 V,		19		nC
Gate to Drain Charge	Q _{GD}	I _D = 33 A		24		nC
Body Diode Forward Voltage Note	V _{F(S-D)}	I _F = 33 A, V _{GS} = 0 V		0.76		V
Reverse Recovery Time	trr	IF = 33 A, VGS = 0 V,		55		ns
Reverse Recovery Charge	Qrr	di/dt = 100 A/μs		66		nC
Gate Resistance	R _G	f = 1 MHz		1.4		Ω

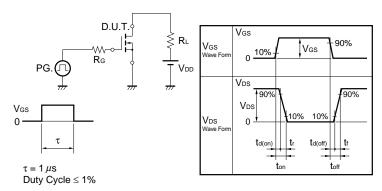
Note Pulsed

TEST CIRCUIT 1 AVALANCHE CAPABILITY

$\begin{array}{c} \text{D.U.T.} \\ \text{Rg} = 25 \, \Omega \\ \text{VGS} = 20 \rightarrow 0 \, \text{V} \end{array} \begin{array}{c} \text{PG.} \\ \text{M} \end{array} \begin{array}{c} \text{D.U.T.} \\ \text{N} \end{array} \begin{array}{c} \text{D.U.T.} \\ \text{N} \end{array} \begin{array}{c} \text{D.U.T.} \\ \text{N} \end{array}$



TEST CIRCUIT 2 SWITCHING TIME

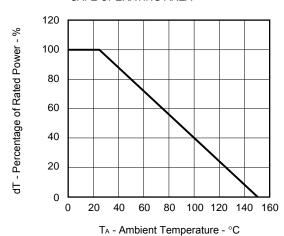


TEST CIRCUIT 3 GATE CHARGE

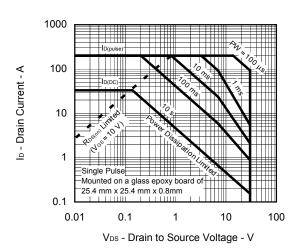
$$\begin{array}{c|c} D.U.T. \\ \hline \\ I_G = 2 \text{ mA} \\ \hline \\ \hline \\ \hline \\ \hline \\ \end{array} \begin{array}{c} R_L \\ \hline \\ \hline \\ V_{DD} \end{array}$$

TYPICAL CHARACTERISTICS (TA = 25°C)

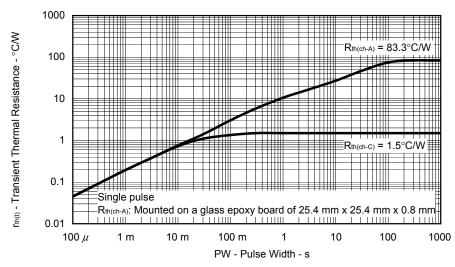
DERATING FACTOR OF FORWARD BIAS SAFE OPERATING AREA



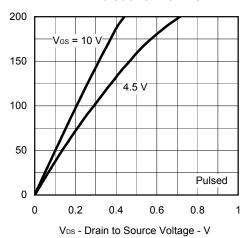
FORWARD BIAS SAFE OPERATING AREA



TRANSIENT THERMAL RESISTANCE vs. PULSE WIDTH

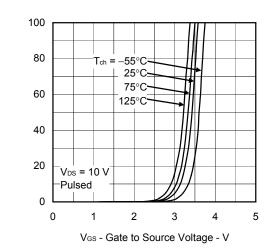


DRAIN CURRENT vs. DRAIN TO SOURCE VOLTAGE



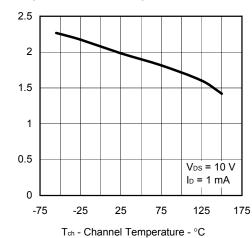
lo - Drain Current - A

FORWARD TRANSFER CHARACTERISTICS

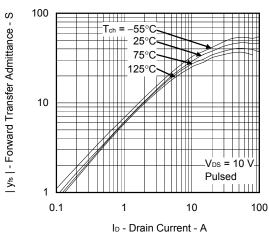


VGS(off) - Gate to Source Cut-off Voltage - V

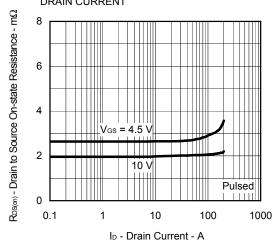
GATE TO SOURCE CUT-OFF VOLTAGE vs. CHANNEL TEMPERATURE



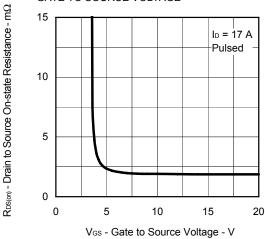
FORWARD TRANSFER ADMITTANCE vs. DRAIN CURRENT



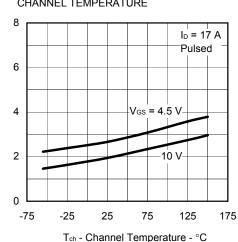
DRAIN TO SOURCE ON-STATE RESISTANCE vs. DRAIN CURRENT



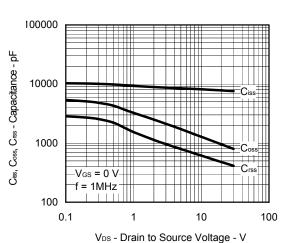
DRAIN TO SOURCE ON-STATE RESISTANCE vs. GATE TO SOURCE VOLTAGE



DRAIN TO SOURCE ON-STATE RESISTANCE vs. CHANNEL TEMPERATURE

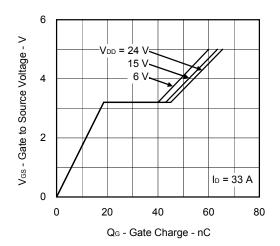


CAPACITANCE vs. DRAIN TO SOURCE VOLTAGE

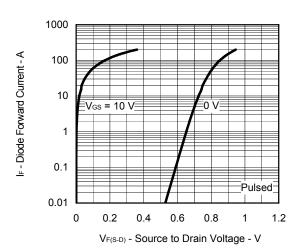


R_{DS(ση)} - Drain to Source On-state Resistance - mΩ

DYNAMIC INPUT/OUTPUT CHARACTERISTICS



SOURCE TO DRAIN DIODE FORWARD VOLTAGE



ORDERING INFORMATION

PART NUMBER	LEAD PLATING	PACKING	PACKAGE	
μPA2723T1A-E1-AZ Note	C- D:		8-pin HVSON	
μPA2723T1A-E2-AZ Note	Sn-Bi	T 2000 - /l		
μPA2723T1A-E1-AY Note	D 0	Tape 3000 p/reel	0.10 g TYP.	
μPA2723T1A-E2-AY ^{Note}	Pure Sn			

Note Pb-free (This product does not contain Pb in the external electrode.)

NEC μ PA2723T1A

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