

BUD42D

High Speed, High Gain Bipolar NPN Transistor with Antisaturation Network and Transient Voltage Suppression Capability

The BUD42D is a state-of-the-art bipolar transistor. Tight dynamic characteristics and lot to lot minimum spread make it ideally suitable for light ballast applications.

Features

- Free-Wheeling Diode Built-In
- Flat DC Current Gain
- Fast Switching Times and Tight Distribution
- “6 Sigma” Process Providing Tight and Reproducible Parameter Spreads
- Epoxy Meets UL 94 V-0 @ 0.125 in
- ESD Ratings: Machine Model, C; >400 V
Human Body Model, 3B; >8000 V
- Pb-Free Packages are Available

Two Versions

- BUD42D-1: Case 369D for Insertion Mode
- BUD42D, BUD42DT4: Case 369C for Surface Mount Mode

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-Emitter Sustaining Voltage	V_{CEO}	350	Vdc
Collector-Base Breakdown Voltage	V_{CBO}	650	Vdc
Collector-Emitter Breakdown Voltage	V_{CES}	650	Vdc
Emitter-Base Voltage	V_{EBO}	9	Vdc
Collector Current – Continuous	I_C	4.0	Adc
– Peak (Note 1)	I_{CM}	8.0	
Base Current – Continuous	I_B	1.0	Adc
– Peak (Note 1)	I_{BM}	2.0	
Total Device Dissipation @ $T_C = 25^\circ\text{C}$	P_D	25	W
Derate above 25°C		0.2	W/ $^\circ\text{C}$
Operating and Storage Temperature	T_J, T_{stg}	-65 to +150	$^\circ\text{C}$

TYPICAL GAIN

Typical Gain @ $I_C = 1\text{ A}, V_{CE} = 2\text{ V}$	h_{FE}	13	–
Typical Gain @ $I_C = 0.3\text{ A}, V_{CE} = 1\text{ V}$	h_{FE}	16	–

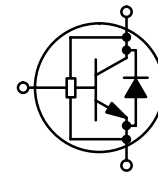
Maximum ratings are those values beyond which device damage can occur. Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and are not valid simultaneously. If these limits are exceeded, device functional operation is not implied, damage may occur and reliability may be affected.



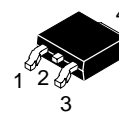
ON Semiconductor®

<http://onsemi.com>

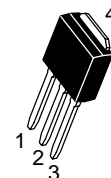
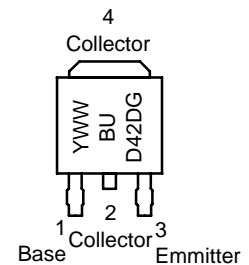
**4 AMPERES
650 VOLTS, 25 WATTS
POWER TRANSISTOR**



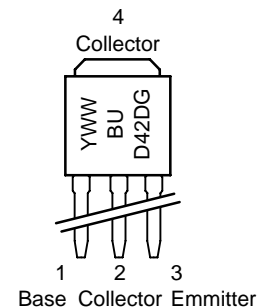
MARKING DIAGRAMS



**DPAK
CASE 369C
STYLE 1**



**DPAK
CASE 369D
STYLE 1**



Y = Year
WW = Work Week
BUD43D = Device Code
G = Pb-Free Package

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 10 of this data sheet.

BUD42D

1. Pulse Test: Pulse Width = 5.0 ms, Duty Cycle = 10%10

THERMAL CHARACTERISTICS

Characteristic	Symbol	Value	Unit
Thermal Resistance, Junction-to-Case	$R_{\theta JC}$	5.0	$^{\circ}C/W$
Thermal Resistance, Junction-to-Ambient	$R_{\theta JA}$	71.4	$^{\circ}C/W$
Maximum Lead Temperature for Soldering Purposes: 1/8 in from Case for 5 seconds	T_L	260	$^{\circ}C$

ELECTRICAL CHARACTERISTICS ($T_C = 25^{\circ}C$ unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
----------------	--------	-----	-----	-----	------

OFF CHARACTERISTICS

Collector-Emitter Sustaining Voltage ($I_C = 100$ mA, $L = 25$ mH)	$V_{CE(sus)}$	350	430	-	Vdc
Collector-Base Breakdown Voltage ($I_{CBO} = 1$ mA)	V_{CBO}	650	780	-	Vdc
Emitter-Base Breakdown Voltage ($I_{EBO} = 1$ mA)	V_{EBO}	9.0	12	-	Vdc
Collector Cutoff Current ($V_{CE} = \text{Rated } V_{CE0}$, $I_B = 0$)	I_{CEO}	-	-	100 200	μAdc
Collector Cutoff Current ($V_{CE} = \text{Rated } V_{CES}$, $V_{EB} = 0$)	I_{CES}	-	-	10 200	μAdc
Emitter-Cutoff Current ($V_{EB} = 9$ Vdc, $I_C = 0$)	I_{EBO}	-	-	100	μAdc

ON CHARACTERISTICS

Base-Emitter Saturation Voltage ($I_C = 1$ Adc, $I_B = 0.2$ Adc)	$V_{BE(sat)}$	-	0.85	1.2	Vdc
Collector-Emitter Saturation Voltage ($I_C = 2$ Adc, $I_B = 0.5$ Adc)	$V_{CE(sat)}$	-	0.2	1.0	Vdc
DC Current Gain ($I_C = 1$ Adc, $V_{CE} = 2$ Vdc) ($I_C = 2$ Adc, $V_{CE} = 5$ Vdc)	h_{FE}	8.0 10	13 12	- -	-

DIODE CHARACTERISTICS

Forward Diode Voltage ($I_{EC} = 1.0$ Adc)	V_{EC}	-	0.9	1.5	V
--	----------	---	-----	-----	---

SWITCHING CHARACTERISTICS: Resistive Load (D.C. $\leq 10\%$, Pulse Width = 40 μs)

Turn-Off Time ($I_C = 1.2$ Adc, $I_{B1} = 0.4$ A, $I_{B2} = 0.1$ A, $V_{CC} = 300$ V)	T_{off}	4.6	-	6.55	μs
Fall Time ($I_C = 2.5$ Adc, $I_{B1} = I_{B2} = 0.5$ A, $V_{CC} = 150$ V, $V_{BE} = -2$ V)	T_f	-	-	0.8	μs

DYNAMIC SATURATION VOLTAGE

Dynamic Saturation Voltage: Determined 1 μs and 3 μs respectively after rising I_{B1} reaches 90% of final I_{B1}	$I_C = 400$ mA $I_{B1} = 40$ mA $V_{CC} = 300$ V	@ 1 μs	@ $T_C = 25^{\circ}C$ @ $T_C = 125^{\circ}C$	$V_{CE(dsat)}$	-	2.8	-	V
		@ 3 μs	@ $T_C = 25^{\circ}C$ @ $T_C = 125^{\circ}C$		-	3.2	-	
	$I_C = 1$ A $I_{B1} = 200$ mA $V_{CC} = 300$ V	@ 1 μs	@ $T_C = 25^{\circ}C$ @ $T_C = 125^{\circ}C$		-	0.75	-	
		@ 3 μs	@ $T_C = 25^{\circ}C$ @ $T_C = 125^{\circ}C$		-	1.3	-	

BUD42D

TYPICAL STATIC CHARACTERISTICS

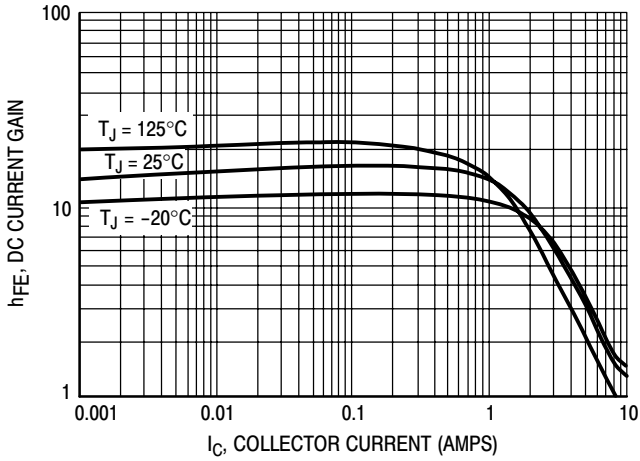


Figure 1. DC Current Gain @ $V_{CE} = 1\text{ V}$

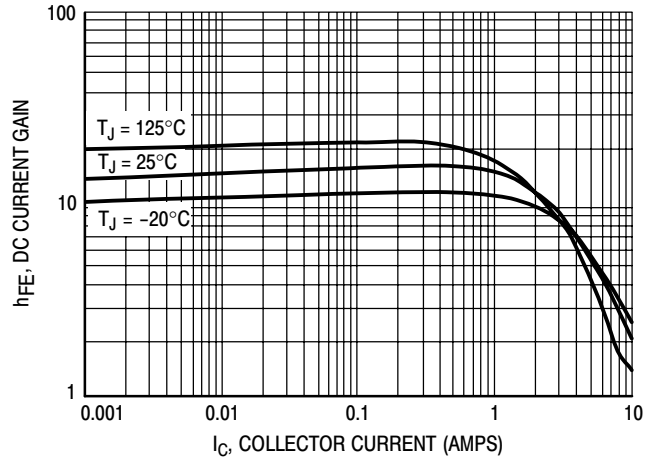


Figure 2. DC Current Gain @ $V_{CE} = 5\text{ V}$

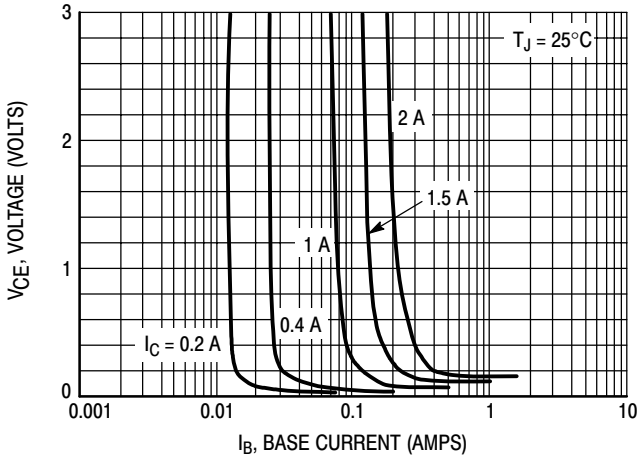


Figure 3. Collector Saturation Region

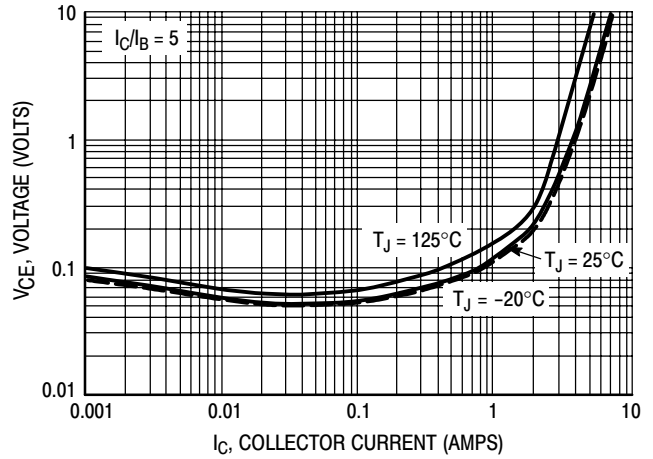


Figure 4. Collector-Emitter Saturation Voltage

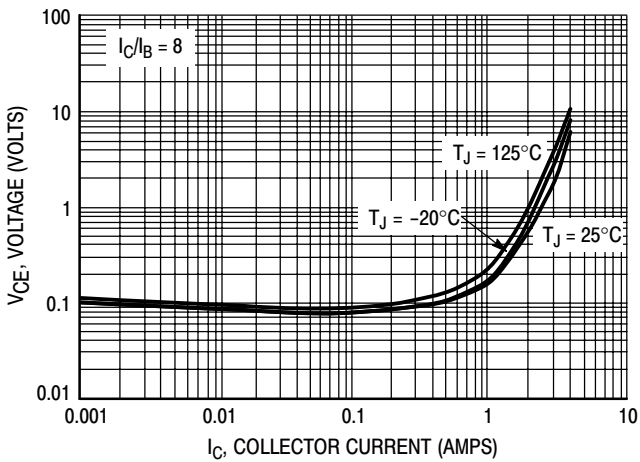


Figure 5. Collector-Emitter Saturation Voltage

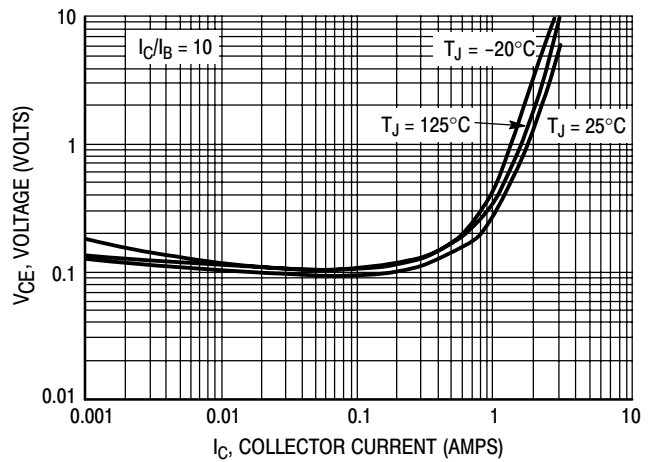


Figure 6. Collector-Emitter Saturation Voltage

BUD42D

TYPICAL STATIC CHARACTERISTICS

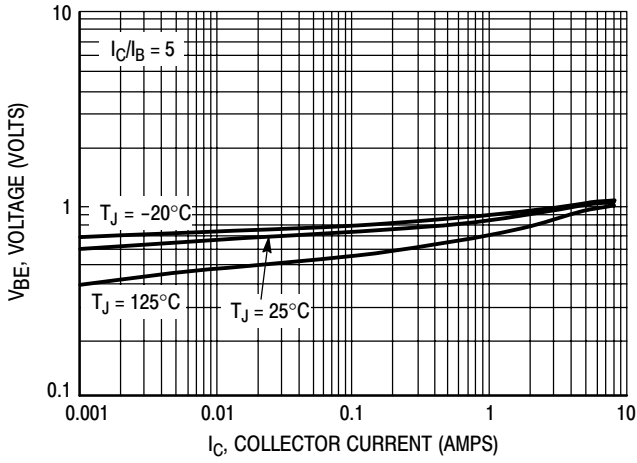


Figure 7. Base-Emitter Saturation Region

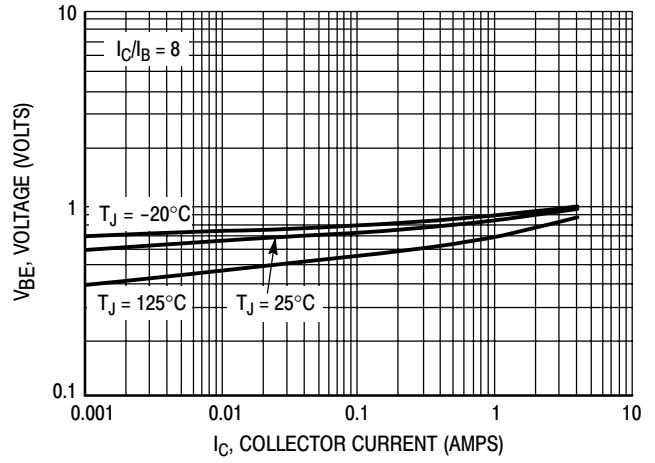


Figure 8. Base-Emitter Saturation Region

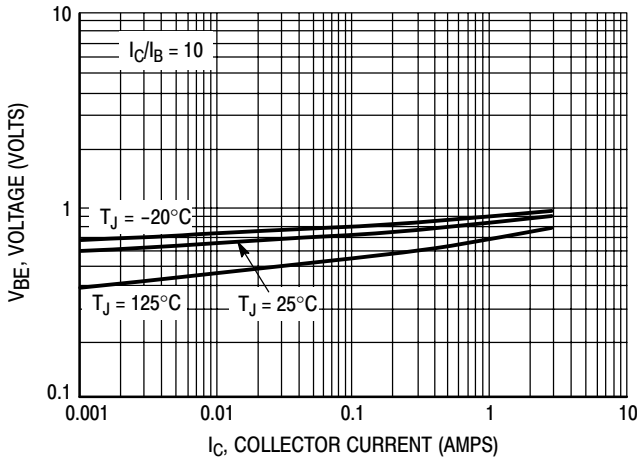


Figure 9. Base-Emitter Saturation Region

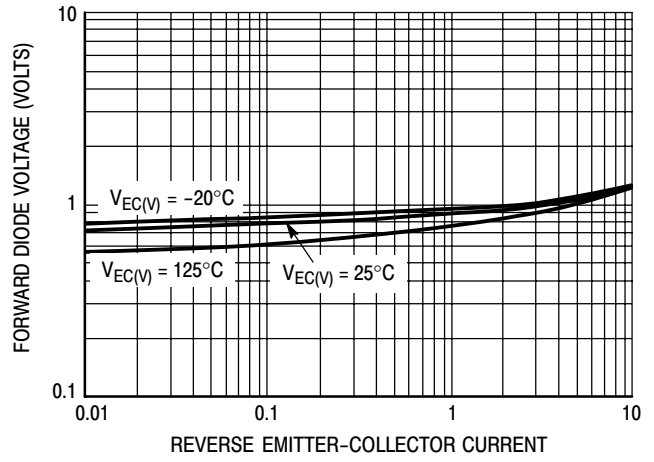


Figure 10. Forward Diode Voltage

BUD42D

TYPICAL SWITCHING CHARACTERISTICS

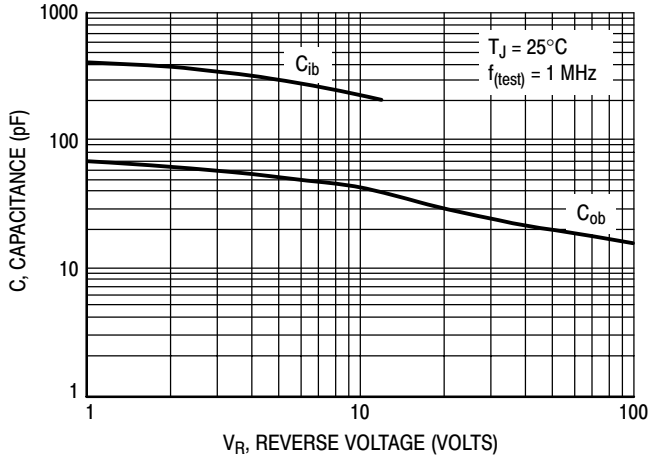


Figure 11. Capacitance

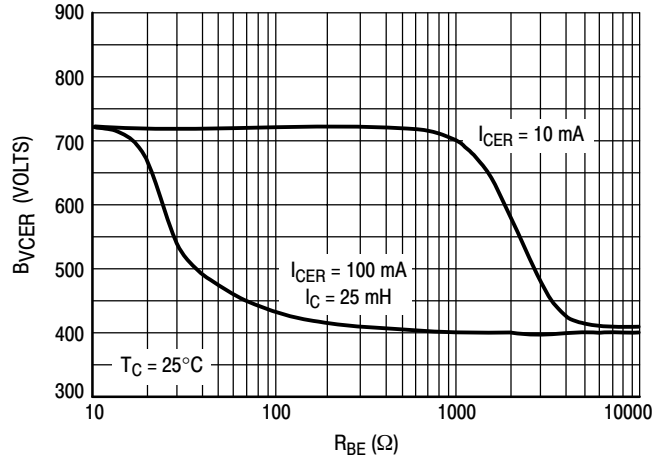


Figure 12. $B_{V_{CER}} = f(R_{BE})$

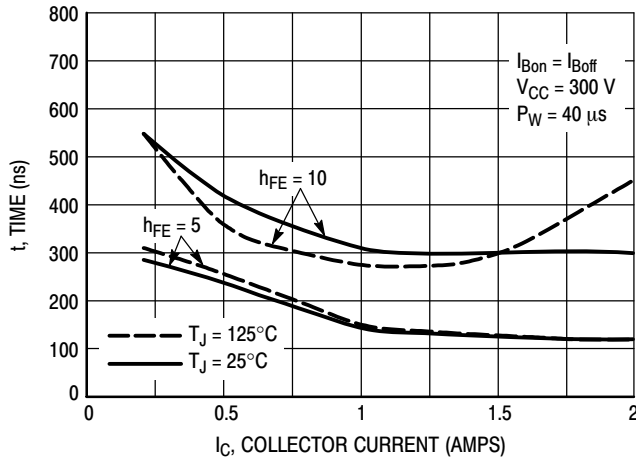


Figure 13. Resistive Switching, t_{on}

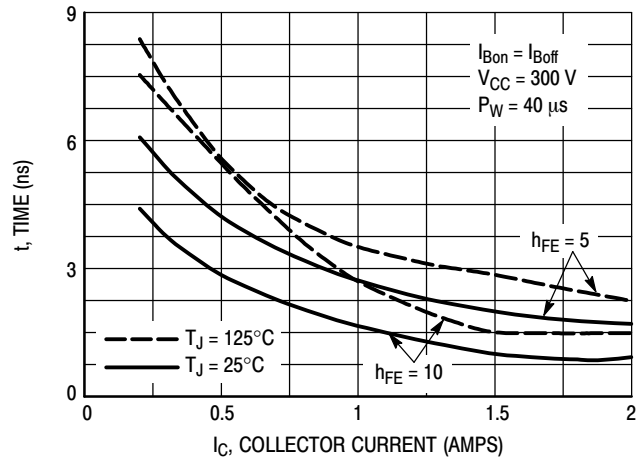


Figure 14. Resistive Switching, t_{off}

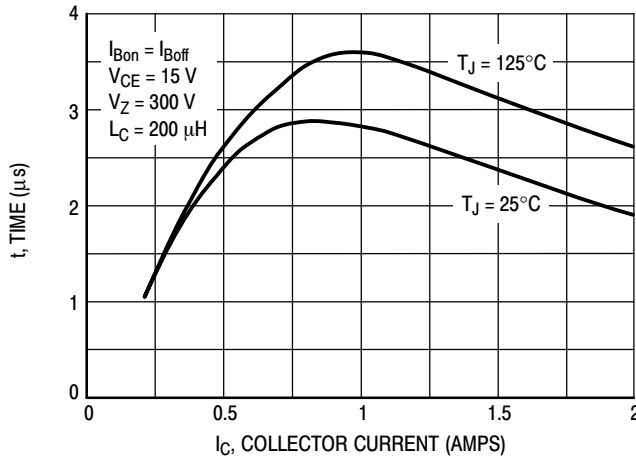


Figure 15. Inductive Storage Time, t_{si} @ $h_{FE} = 5$

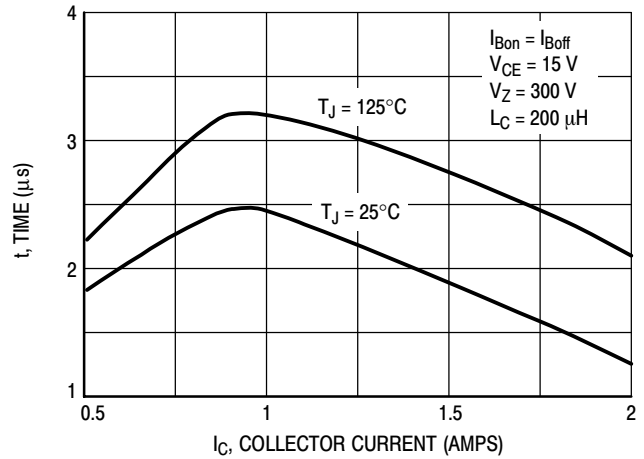


Figure 16. Inductive Storage Time, t_{si} @ $h_{FE} = 10$

TYPICAL SWITCHING CHARACTERISTICS

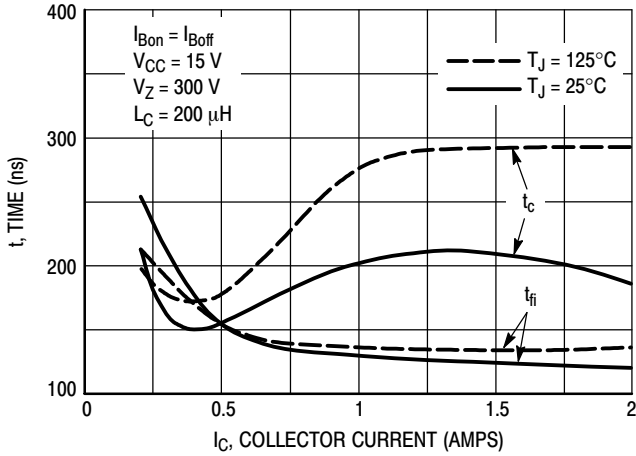


Figure 17. Inductive Fall and Cross Over Time, t_{fi} and t_c @ $h_{FE} = 5$

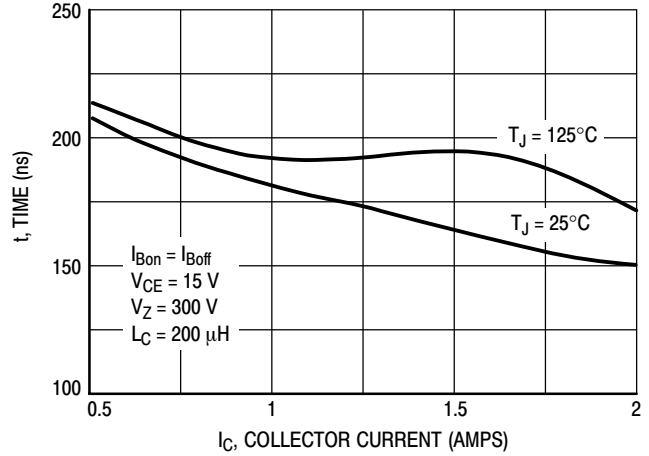


Figure 18. Inductive Fall Time, t_{fi} @ $h_{FE} = 10$

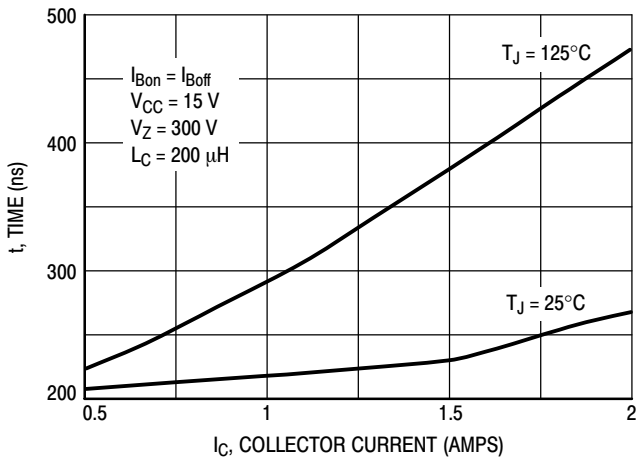


Figure 19. Inductive Cross Over Time, t_c @ $h_{FE} = 10$

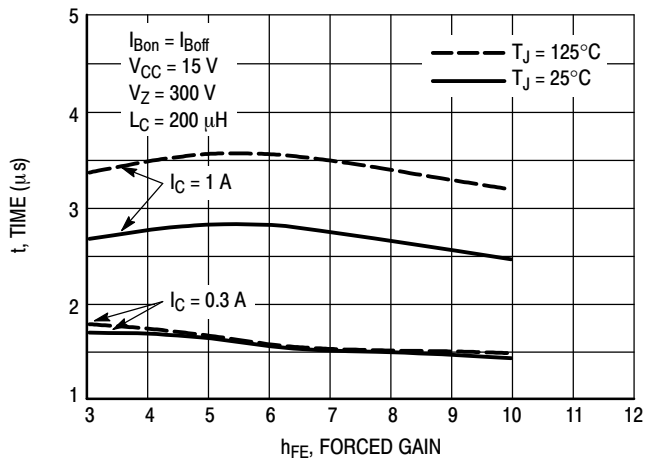


Figure 20. Inductive Storage Time, t_{si}

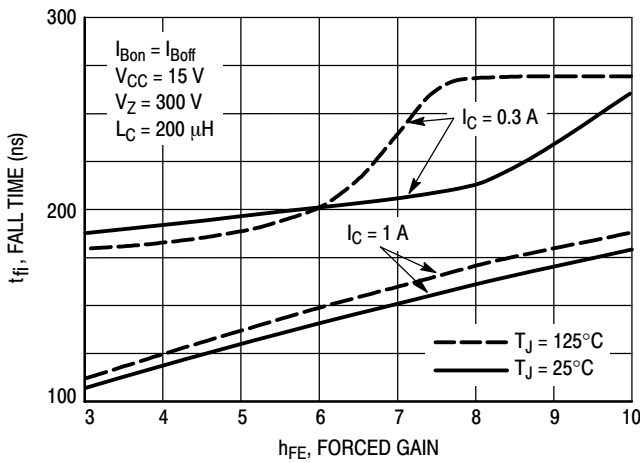


Figure 21. Inductive Fall Time, t_f

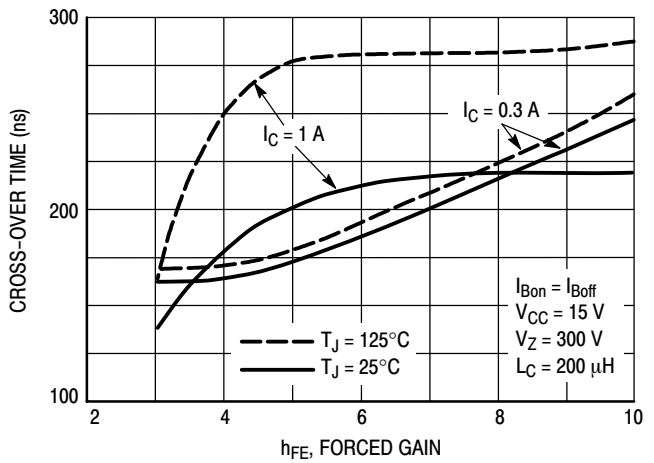


Figure 22. Inductive Cross Over Time, t_c

TYPICAL SWITCHING CHARACTERISTICS

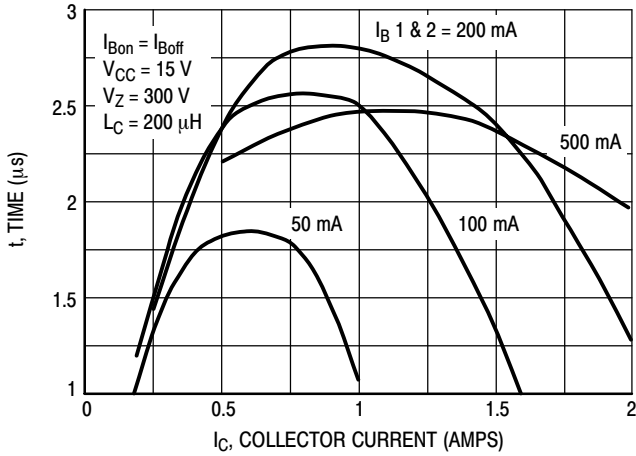


Figure 23. Inductive Storage Time, t_{si}

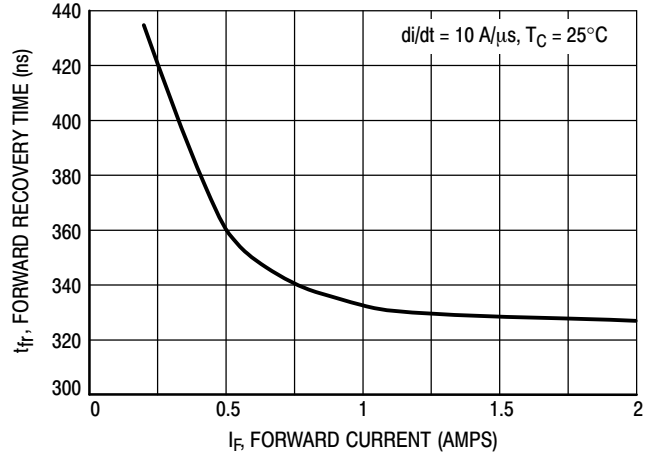


Figure 24. Forward Recovery Time, t_{fr}

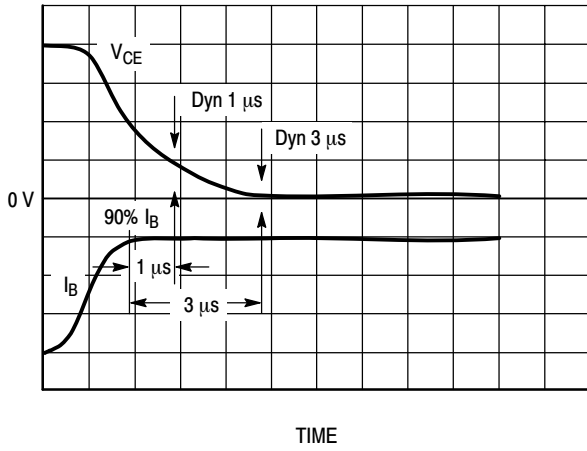


Figure 25. Dynamic Saturation Voltage Measurements

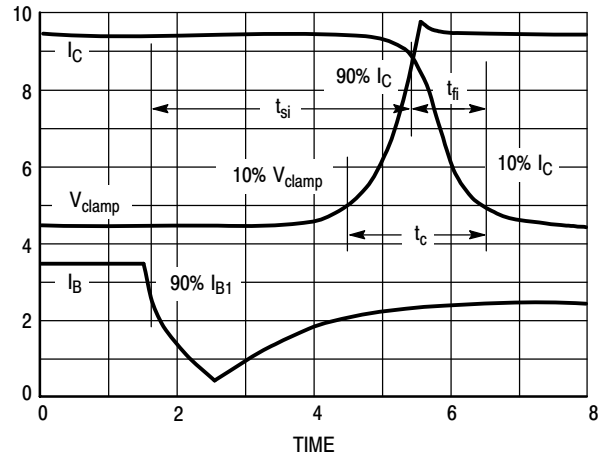
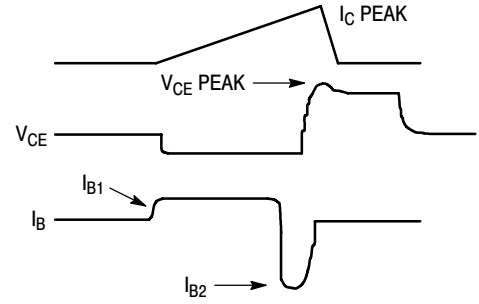
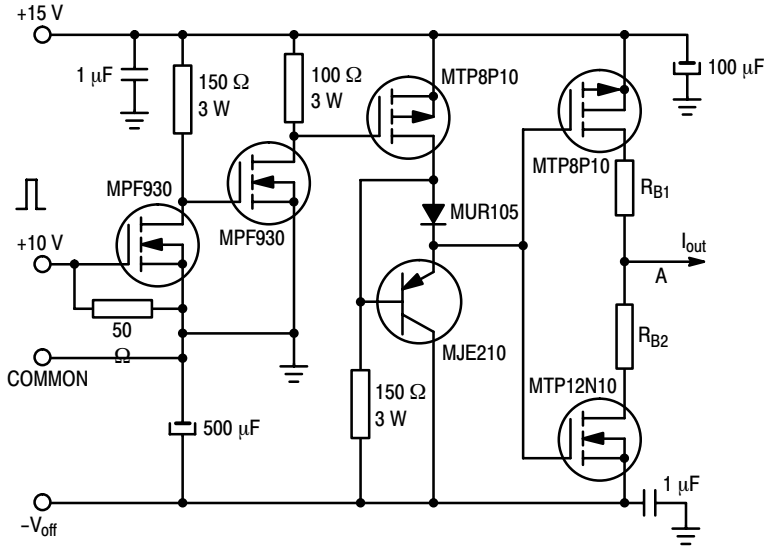


Figure 26. Inductive Switching Measurements

BUD42D

TYPICAL SWITCHING CHARACTERISTICS

Table 1. Inductive Load Switching Drive Circuit



$V_{(BR)CEO(sus)}$
 $L = 10 \text{ mH}$
 $R_{B2} = \infty$
 $V_{CC} = 20 \text{ Volts}$
 $I_{C(pk)} = 100 \text{ mA}$

Inductive Switching
 $L = 200 \mu\text{H}$
 $R_{B2} = 0$
 $V_{CC} = 15 \text{ Volts}$
 R_{B1} selected for
 desired I_{B1}

RBSOA
 $L = 500 \mu\text{H}$
 $R_{B2} = 0$
 $V_{CC} = 15 \text{ Volts}$
 R_{B1} selected for
 desired I_{B1}

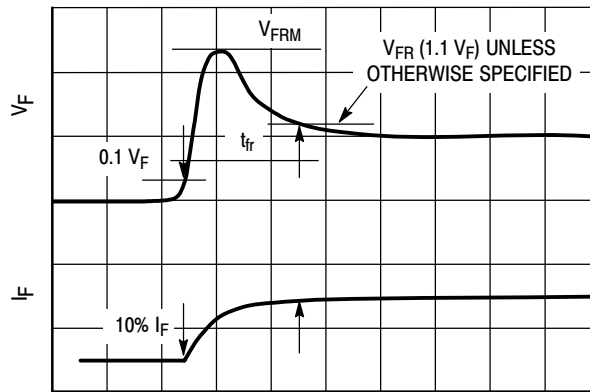


Figure 27. t_{fr} Measurement

BUD42D

MAXIMUM RATINGS

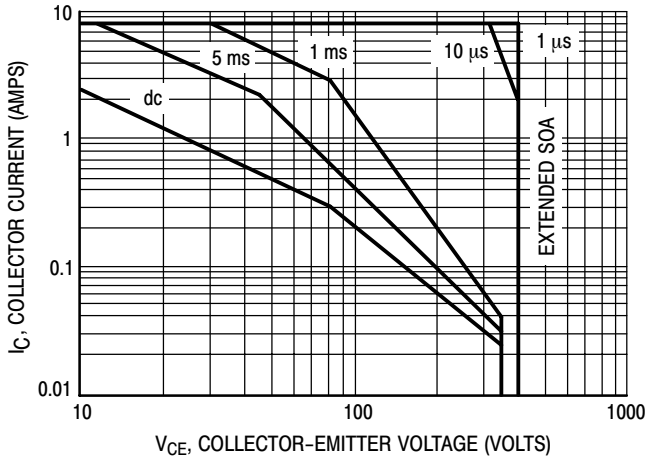


Figure 28. Forward Bias Safe Operating Area

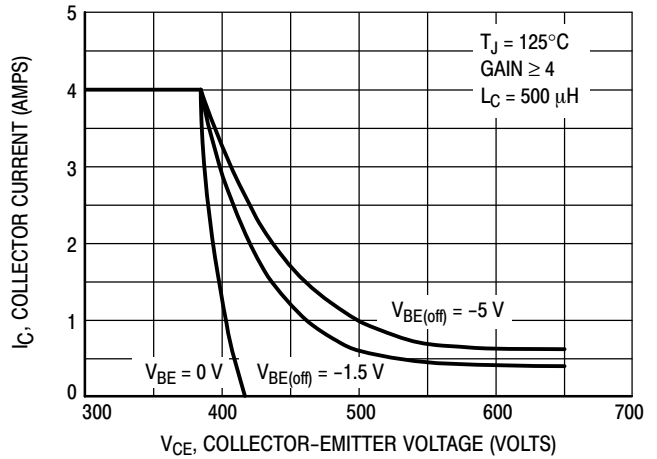


Figure 29. Reverse Bias Safe Operating Area

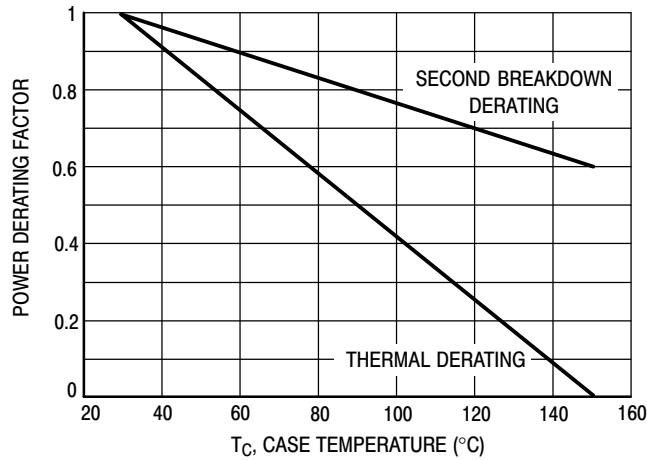


Figure 30. Power Derating

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C - V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate. The data of Figure 28 is based on $T_C = 25^\circ\text{C}$; $T_{j(pk)}$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when $T_C > 25^\circ\text{C}$. Second Breakdown limitations do not derate like thermal limitations. Allowable current at the voltages shown on

Figure 28 may be found at any case temperature by using the appropriate curve on Figure 30.

$T_{j(pk)}$ may be calculated from the data in Figure 31. At any case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown. For inductive loads, high voltage and current must be sustained simultaneously during turn-off with the base to emitter junction reverse biased. The safe level is specified as reverse biased safe operating area (Figure 29). This rating is verified under clamped conditions so that the device is never subjected to an avalanche mode.

BUD42D

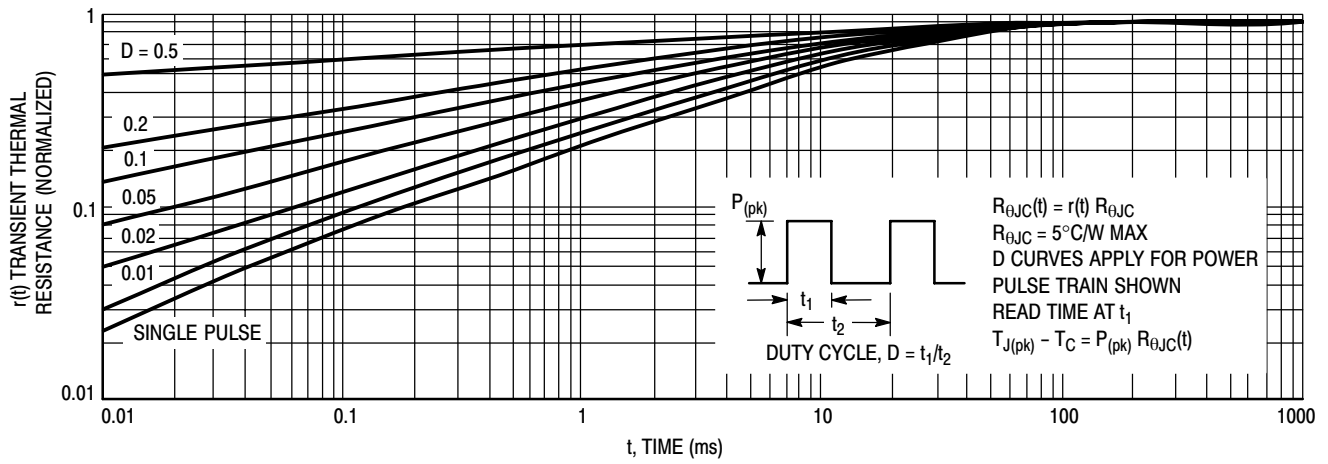


Figure 31. Thermal Response

ORDERING INFORMATION

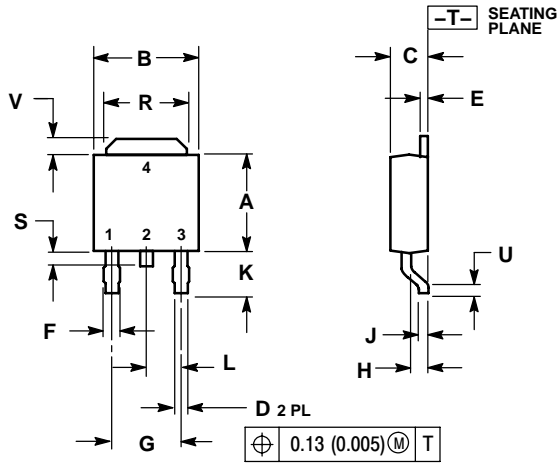
Device	Package	Shipping [†]
BUD42D	DPAK	75 Units / Rail
BUD42DG	DPAK (Pb-Free)	75 Units / Rail
BUD42D-1	DPAK Straight Lead	75 Units / Rail
BUD42D-1G	DPAK Straight Lead (Pb-Free)	75 Units / Rail
BUD42DT4	DPAK	2500 Units / Tape & Reel
BUD42DT4G	DPAK (Pb-Free)	2500 Units / Tape & Reel

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

BUD42D

PACKAGE DIMENSIONS

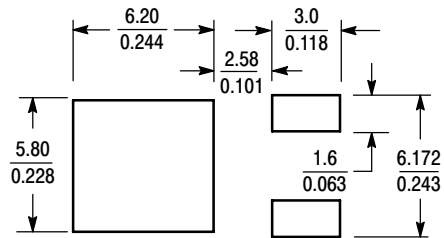
DPAK
CASE 369C-01
ISSUE O



DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.235	0.245	5.97	6.22
B	0.250	0.265	6.35	6.73
C	0.086	0.094	2.19	2.38
D	0.027	0.035	0.69	0.88
E	0.018	0.023	0.46	0.58
F	0.037	0.045	0.94	1.14
G	0.180 BSC		4.58 BSC	
H	0.034	0.040	0.87	1.01
J	0.018	0.023	0.46	0.58
K	0.102	0.114	2.60	2.89
L	0.090 BSC		2.29 BSC	
R	0.180	0.215	4.57	5.45
S	0.025	0.040	0.63	1.01
U	0.020	---	0.51	---
V	0.035	0.050	0.89	1.27
Z	0.155	---	3.93	---

STYLE 1:
PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

SOLDERING FOOTPRINT*



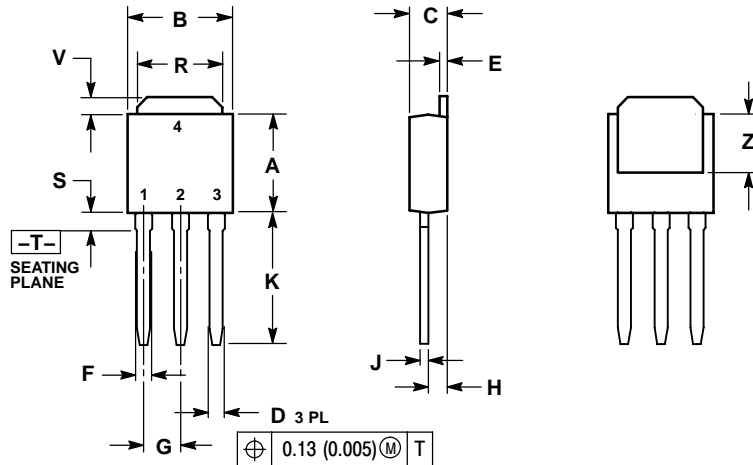
SCALE 3:1 $\left(\frac{\text{mm}}{\text{inches}}\right)$

*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

BUD42D

PACKAGE DIMENSIONS

DPAK STRAIGHT LEAD CASE 369D-01 ISSUE B



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.235	0.245	5.97	6.35
B	0.250	0.265	6.35	6.73
C	0.086	0.094	2.19	2.38
D	0.027	0.035	0.69	0.88
E	0.018	0.023	0.46	0.58
F	0.037	0.045	0.94	1.14
G	0.090 BSC		2.29 BSC	
H	0.034	0.040	0.87	1.01
J	0.018	0.023	0.46	0.58
K	0.350	0.380	8.89	9.65
R	0.180	0.215	4.45	5.45
S	0.025	0.040	0.63	1.01
V	0.035	0.050	0.89	1.27
Z	0.155	---	3.93	---

STYLE 1:

- PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

ON Semiconductor and are registered trademarks of Semiconductor Components Industries, LLC (SCILLC). SCILLC reserves the right to make changes without further notice to any products herein. SCILLC makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does SCILLC assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. "Typical" parameters which may be provided in SCILLC data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. SCILLC does not convey any license under its patent rights nor the rights of others. SCILLC products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the SCILLC product could create a situation where personal injury or death may occur. Should Buyer purchase or use SCILLC products for any such unintended or unauthorized application, Buyer shall indemnify and hold SCILLC and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that SCILLC was negligent regarding the design or manufacture of the part. SCILLC is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
Literature Distribution Center for ON Semiconductor
P.O. Box 61312, Phoenix, Arizona 85082-1312 USA
Phone: 480-829-7710 or 800-344-3860 Toll Free USA/Canada
Fax: 480-829-7709 or 800-344-3867 Toll Free USA/Canada
Email: orderlit@onsemi.com

N. American Technical Support: 800-282-9855 Toll Free
USA/Canada

Japan: ON Semiconductor, Japan Customer Focus Center
2-9-1 Kamimeguro, Meguro-ku, Tokyo, Japan 153-0051
Phone: 81-3-5773-3850

ON Semiconductor Website: <http://onsemi.com>

Order Literature: <http://www.onsemi.com/litorder>

For additional information, please contact your local Sales Representative.