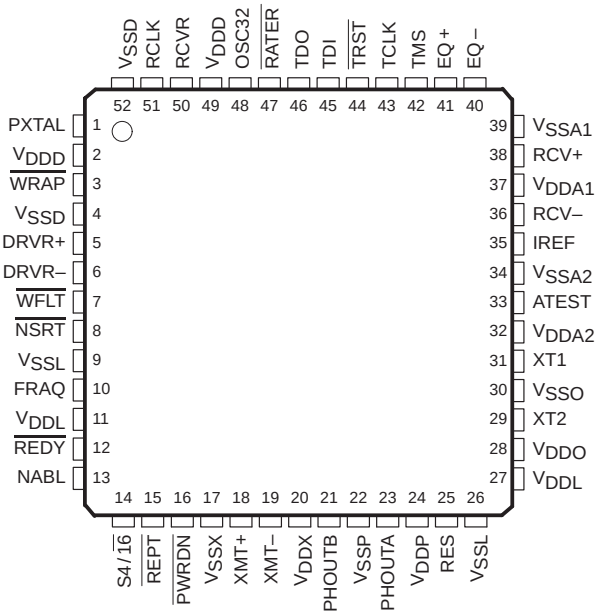
- **Facilitates Connection of the TI380C25, TMS380C26, or TI380C27 to Token Ring**
- **Internal Crystal Oscillator for Reference-Clock Generation**
- **Loop Back (Wrap Mode) for Self-Test Diagnostics**
- **Compatible With Electrical Interface of ISO/IEC 8802.5: 1995 (ANSI/IEEE Std. 802.5) Token-Ring Access Method and Physical Layer Specifications**
- **Glueless Interface to TI380C2x Commprocessor for Token Ring**
- **16- and 4-Mbps Token-Ring Data Rates With no External Switching Circuits**
- **Repeater Application Requires no Additional Active Components**
- **Digital Phase-Locked Loop**
  - **Provides Precise Control of Bandwidths**
  - **Provides Improved Jitter Tolerance**
  - **Minimizes Accumulated Phase Slope**
- **Phantom Drive for Physical Insertion Onto Ring**
- **Differential Line Receiver With Level-Dependent Frequency Equalization**
- **Low-Impedance Differential Line Driver to Ease Transmit-Filter Design**

PAH PACKAGE
(TOP VIEW)



- **On-Chip Watchdog Timer**
- **Low-Power 0.8-μm Enhanced Performance Implanted CMOS (EPIC™) Technology by Texas Instruments (TI™)**
- **PCMCIA-Compatible 52-Lead 1,0-mm Plastic Quad Flatpack**

description

The TI380C60A token-ring interface device is a full-duplex electrical interface compatible with ISO/IEC 8802.5:1995 (ANSI/IEEE Std. 802.5) token-ring access method and physical layer specifications. The TI380C60A operates at the IEEE standard 4- and 16-Mbps data rates. The Manchester-encoded data stream is received and phase-aligned using an on-chip phase-locked loop (PLL). Both the recovered clock and data are passed to the protocol-handling circuits of one of the TI380C2x single-chip token-ring commprocessors for serial-to-parallel conversion and data processing. On transmit, the TI380C60A buffers the output of the TI380C2x and drives the media by way of suitable isolation and waveform-shaping components.

All necessary functions required to interface with an IEEE-802.5 token ring are provided. These include the PLL, the phantom drive (to control the relays within a trunk-coupling unit), and wire-fault detection circuits. An internal wrap function is provided for self-test, and a watchdog timer is included to provide fail-safe deinsertion from the ring in the event of a station microcode or commprocessor failure.

The TI380C60A, when coupled with one of the TI380C2x token-ring commprocessors, forms a highly integrated token-ring LAN adapter compatible with the ISO/IEEE Standard 802.5. The TI380C60A synthesizes the necessary token-ring reference clock for its own use and for the TI380C2x. This removes the need for external components to provide this function.

description (continued)

The TI380C60A can function as a stand-alone device because the digital PLL is self-contained and requires no additional circuits for frequency management. Using the device in this manner in the repeat mode provides a highly integrated token-ring repeater with no additional active components needed for wiring center applications.

The TI380C60A is available in a 52-lead 1,0-mm plastic quad flatpack and is characterized for operation from 0°C to 95°C with a typical power dissipation of 600 mW.

Pin Functions

PIN NAME	PIN NO.	I/O/E†	TYPE‡	DESCRIPTION
ATEST	33	E	N	Analog test. ATEST should be left unconnected.
DRVR+ DRVR–	5 6	I I	D D	Differential driver data inputs. DRVR+ and DRVR– receive the ’380C2x transmit data.
EQ+ EQ–	41 40	E E	N N	Equalization/gain points. EQ+ and EQ- provide connections to allow frequency tuning of the equalization circuit.
FRAQ	10	I	TTL	Frequency acquisition control. FRAQ is driven by the ’380C2x or can be tied low for repeater applications. H = Clock-recovery PLL is initialized L = Normal operation
IREF	35	E	N	Internal reference. IREF allows the internal bias current of analog circuitry to be set by way of an external resistor.
NABL	13	I	TTL	Output-enable control. NABL can be used in token-ring /Ethernet™ applications to disable the token-ring function. (See Note 1) H = TI380C60A operates normally L = All outputs are driven to the high-impedance state, except XMT+/XMT–, which are driven low. Internal logic continues to operate unless $\overline{\text{PWRDN}}$ is asserted low.
$\overline{\text{NSRT}}$	8	I	TTL	Insert control. $\overline{\text{NSRT}}$ enables the phantom-driver outputs (PHOUTA and PHOUTB) through the watchdog timer for insertion onto the token ring. Static high = Inactive, phantom current removed (due to watchdog timer) Static low = Inactive, phantom current removed (due to watchdog timer) Falling edge = Active, current output on PHOUTA and PHOUTB
PHOUTA PHOUTB	23 21	O O	N N	Phantom-driver outputs A and B. PHOUTA and PHOUTB are the outputs that cause insertion onto the token ring. PHOUTA and PHOUTB should be connected to the center tap of the transmit transformer secondary winding for phantom-drive generation.
$\overline{\text{PWRDN}}$	16	I	TTL	Power-down control H = Normal operation. $\overline{\text{PWRDN}}$ is required to be tied to V_{CC} with an external pullup resistor of 4.7 kΩ. L = TI380C60A is placed into a power-down state. All TTL outputs are driven to the high-impedance state.
PXTAL	1	O	TTL	Token-ring reference-clock output. For 16-Mbps operations, PXTAL is a 32-MHz clock; and for 4-Mbps operations, PXTAL is an 8-MHz clock.
OSC32	48	O	TTL	Oscillator output. OSC32 provides a 32-MHz clock output and can be used to drive OSCIN of a TI380C2x.
$\overline{\text{REPT}}$	15	I	TTL	Repeat-mode enable L = Repeat mode selected. The received and sampled data present on RCVR is also driven out on the XMT+/XMT– pair. This function is overridden if $\overline{\text{WRAP}}$ is asserted low. H = TI380C60A operates normally. (See Note 1)

† I = input, O = output, E = provides external-component connection to the internal circuitry for tuning
‡ TTL = TTL signal, N = non-TTL signal, D = differential drive or data
NOTE 1: Pin has an internal pullup device to maintain a high-voltage level when left unconnected (no etch).

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Pin Functions (Continued)

PIN NAME	PIN NO.	I/O/E†	TYPE‡	DESCRIPTION
$\overline{\text{RATER}}$	47	O	TTL	Rate error. $\overline{\text{RATER}}$ indicates that there are transitions on the RCV+/RCV– input pair (DRVR+/DRVR– if $\overline{\text{WRAP}}$ is asserted low) but that the transition rate is not consistent with the ring speed selected by S4/$\overline{16}$.
RCLK	51	O	TTL	Recovered clock. RCLK is the clock recovered from the token-ring received data. For 16-Mbps operations, it is a 32-MHz clock. For 4-Mbps operations, it is an 8-MHz clock.
RCV+ RCV–	38 36	I I	D D	Receiver inputs. RCV+ and RCV– receive the token-ring data by way of isolation transformers.
RCVR	50	O	TTL	Recovered data. RCVR contains the data recovered from the token ring and should be sampled at the rising edge of RCLK.
$\overline{\text{REDY}}$	12	O	TTL	PLL ready. $\overline{\text{REDY}}$ is normally asserted (active) low. $\overline{\text{REDY}}$ is cleared following the assertion of FRAQ and reasserted after the data-recovery PLL has been reinitialized. H = Received data not valid L = Received data valid
RES	25	—	—	Reserved. RES should be left unconnected.
S4/$\overline{16}$	14	I	TTL	Speed switch. S4/$\overline{16}$ specifies the token-ring data rate. H = 4-Mbps data rate L = 16-Mbps data rate
TCLK TMS TDI TDO	43 42 45 46	I I I O	TTL	Test ports used during the production test of the device. TCLK, TMS, TDI, and TDO should be left unconnected.
$\overline{\text{TRST}}$	44	I	TTL	Test-port reset. $\overline{\text{TRST}}$ should be tied to ground for normal operation of the TI380C60A. H = Reserved L = Test ports forced to an idle state
$\overline{\text{WFLT}}$	7	O	TTL	Phantom-wire fault. $\overline{\text{WFLT}}$ provides an indication of the presence of a short or open circuit on PHOUTA or PHOUTB. H = No fault L = Open or short. The dc fault condition is present in the phantom-drive lines.
$\overline{\text{WRAP}}$	3	I	TTL	Internal wrap-mode control. $\overline{\text{WRAP}}$ allows the TI380C60A to be placed in the loop-back wrap mode for adapter self test. H = Normal ring operation L = Transmit data drives the receive data. RCV+ and RCV– are ignored by the TI380C60A, and XMT+ and XMT– are both forced low.
XMT+ XMT–	18 19	E	D	Transmit differential outputs. XMT+ and XMT– provide a low-impedance differential source for line drive by way of filtering and transformer isolation.
XT1 XT2	31 29	E	N/TTL N	XTAL connection. An 8-MHz crystal network can be connected here to provide a reference clock for the TI380C60A. Alternatively, an 8-MHz TTL clock source can be connected to XT1.
V_{DDA1}	37	—	—	Positive supply voltage for receiver circuits
V_{DDD}	2, 49	—	—	Positive supply voltage for output buffers
V_{DDL}	11, 27	—	—	Positive supply voltage for internal logic
V_{DDA2}	32	—	—	Positive supply voltage for data-recovery PLL
V_{DDO}	28	—	—	Positive supply voltage for XTAL oscillator
V_{DDP}	24	—	—	Positive supply voltage for phantom drive
V_{DDX}	20	—	—	Positive supply voltage for transmit output

† I = input, O = output, E = provides external-component connection to the internal circuitry for tuning
‡ TTL = TTL signal, N = non-TTL signal, D = differential drive or data

Pin Functions (Continued)

PIN NAME	PIN NO.	I/O/E†	TYPE‡	DESCRIPTION
V_{SSA1}	39	—	—	Ground reference for receiver circuits
V_{SSA2}	34	—	—	Ground reference for data-recovery PLL
V_{SSD}	4, 52	—	—	Ground reference for output buffers
V_{SSL}	9, 26	—	—	Ground reference for internal logic
V_{SSX}	17	—	—	Ground reference for transmit output
V_{SSO}	30	—	—	Ground reference for XTAL oscillator
V_{SSP}	22	—	—	Ground reference for phantom drive

† I = input, O = output, E = provides external-component connection to the internal circuitry for tuning
‡ TTL = TTL signal, N = non-TTL signal, D = differential drive or data

architecture

The major blocks of the TI380C60A include the receiver/equalizer, clock recovery PLL, wrap function, phantom drive with wire-fault detector, and watchdog timer. Figure 1 is the block diagram illustrating these major blocks, and the functionality of each block is described in the following sections.

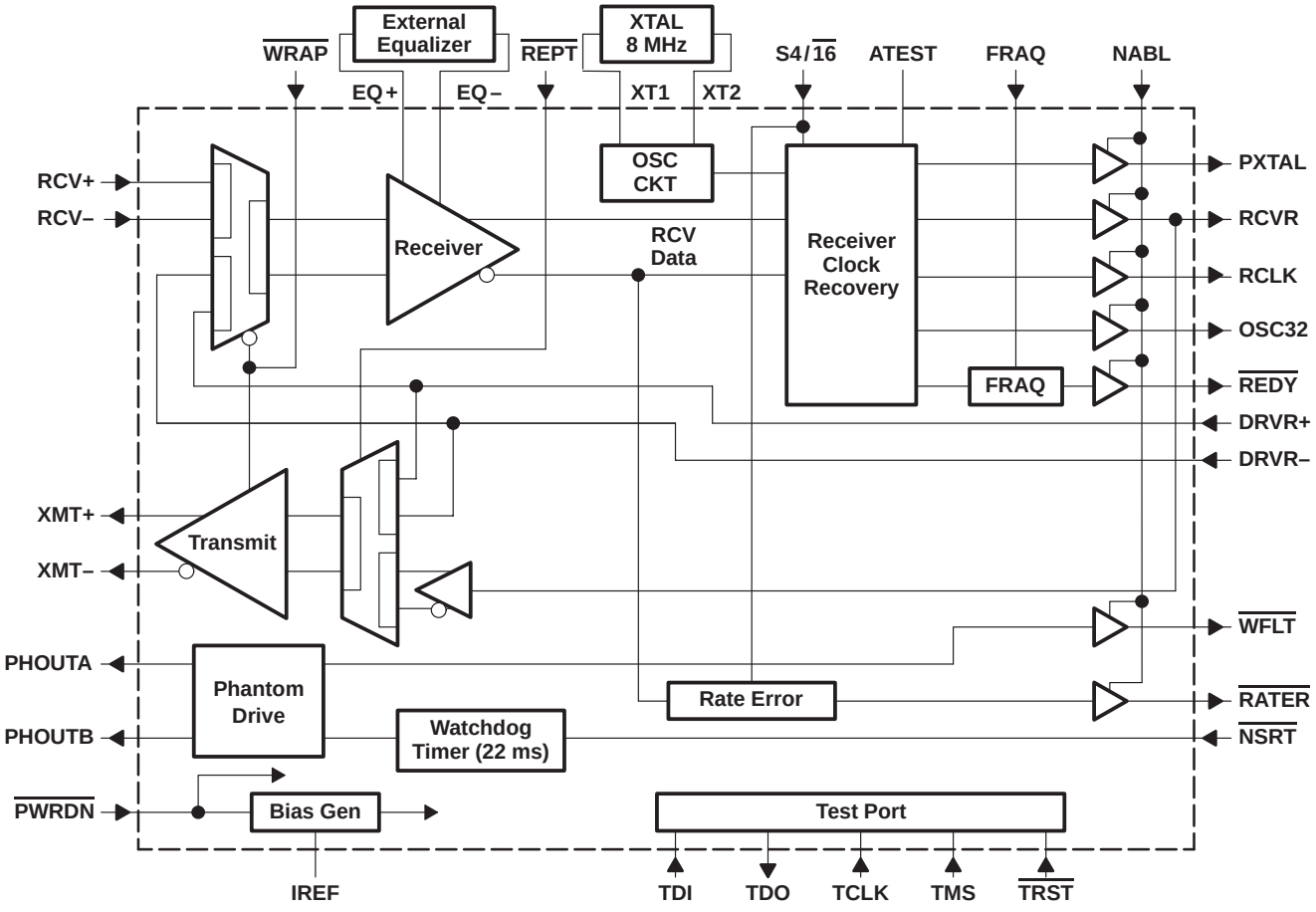


Figure 1. Functional Block Diagram

receiver

Figure 2 shows the arrangement of the line-receiver/equalizer circuit. The differential-input pair, RCV+ and RCV–, is designed to be connected to a floating winding of an isolation transformer. Each is equipped with a bias circuit to center the operating point of the differential input at approximately $V_{DD}/2$.

The differential-input pair consists of a pair of metal oxide semiconductor field effect transistors (MOSFETs), each with an identical current source in its source pin that is set to supply a nominal current of 1.5 mA. At low signal levels, the gain of this pair is inversely proportional to the impedance connected between their sources on EQ– and EQ+. A frequency-equalization network can be connected between EQ+ and EQ– to provide equalization for media signal distortion.

The internal wrap mode is provided for self-test of the device. When selected by taking $\overline{\text{WRAP}}$ low, the normal input path is disabled by a multiplexer and a path is enabled from the DRVR+/DRVR– pair. Receiver gain, thresholds, and equalization are unchanged in the internal wrap mode.

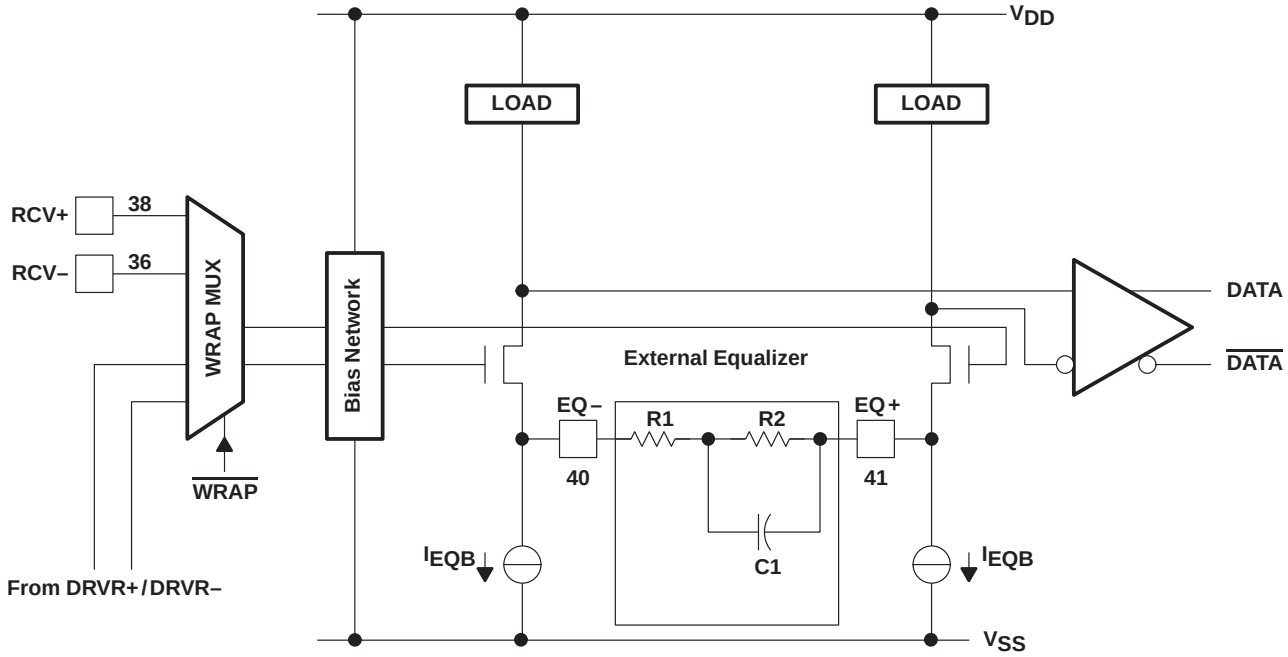


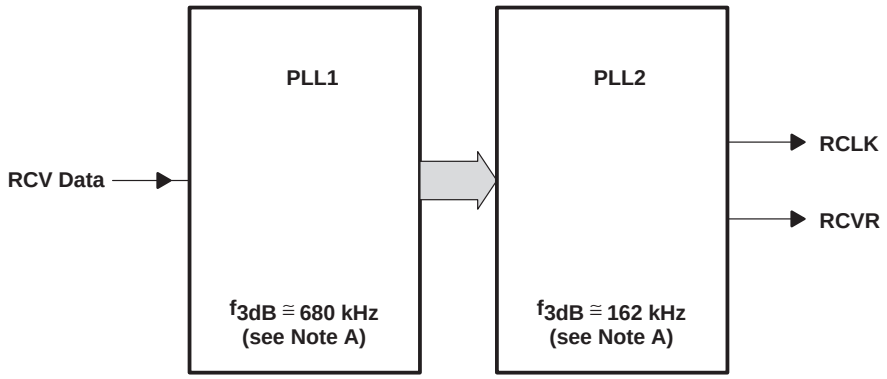
Figure 2. Line Receiver/Equalizer

receiver-clock recovery

The clock and data recovery in TI380C60A is performed by an advanced, digitally controlled phase-locked loop. In contrast to the TMS38054, the PLL of the TI380C60A is digitally controlled and the loop parameters are set by internally programmed digital constants. This results in precise control of loop parameters and requires no external loop-filter components.

The TI380C60A implements an intelligent algorithm to determine the optimum phase position for data-sampling and extracted clock synthesis. The resulting action of the TI380C60A can be modeled as two cascaded PLLs as shown in Figure 3.

receiver-clock recovery (continued)



NOTE A: f_{3dB} = –3dB bandwidth of PLL

Figure 3. Dual-PLL Arrangement

PLL1 represents the algorithm to recover data from the incoming stream detected by the receiver. It has a relatively high bandwidth to provide good jitter tolerance. Data and embedded clock phase information are fed as digital values to PLL2, which generates the extracted clock (RCLK) for the TI380C2x commprocessor. The recovered data is sent to the TI380C2x as the RCVR signal is synchronous with RCLK. In addition to sampling the RCVR signal, the TI380C2x uses RCLK to re-transmit data in most cases. The lower bandwidth of PLL2 greatly reduces the rate of accumulation of data-correlated phase jitter in a token-ring network and provides very good accumulated-phase-slope (APS) characteristics. In addition to RCLK, the token-ring reference clock (PXTAL) and a fixed-frequency 32-MHz clock (OSC32) are also synthesized from the 8-MHz crystal reference.

line driver, wrap function, and repeat mode

The line-drive function of the TI380C60A is performed by XMT+ and XMT–. Unlike the TMS38054, these pins are low-impedance outputs and require external series resistance to provide line termination. These pins provide buffering of the differential signal from the TI380C2x on DRVR+/DRVR– with action to control skew and asymmetry and with no re-timing in the transmit path.

The wrap function is designed to provide a signal path for system self-test diagnostics. When $\overline{\text{WRAP}}$ is taken low, the receiver inputs are ignored and the transmit signal is fed to the receiver input circuitry by way of a multiplexer. In the internal wrap mode, $\overline{\text{WRAP}}$ can be checked by observing the signal amplitude at the equalization pins, EQ+ and EQ–. Equalization is active at this signal level, although the signal does not exhibit the high-frequency attenuation effects for which equalization is intended to compensate. During internal wrap mode, both XMT+ and XMT– are driven to a low state to prevent any dc in the isolation transformer.

When the repeat function is selected, the sampled and re-timed ring data present on RCVR is also driven out on XMT+ and XMT–. This allows the TI380C60A to operate as a stand-alone repeater. Both RCVR and RCLK continue to provide valid sampled ring data and extracted clock as normal. The DRVR+/DRVR– inputs are ignored. The repeat function is enabled by taking $\overline{\text{REPT}}$ low while holding $\overline{\text{WRAP}}$ high.

phantom driver and wire-fault detection

The phantom-drive circuit under control of $\overline{\text{NSRT}}$ generates a dc voltage on both of the phantom-drive outputs, PHOUTA and PHOUTB. In order to maintain the phantom drive, $\overline{\text{NSRT}}$ is toggled by the TI380C2x at least once every 20 ms. An internal watchdog timer is included in the TI380C60A to remove the phantom drive if $\overline{\text{NSRT}}$ fails to have the required transitions.

phantom driver and wire-fault detection (continued)

The watchdog timer is normally not allowed to expire because it is being reinitialized at least every 20 ms. If there is a problem in the TI380C2x or its microcode, resulting in failure to toggle $\overline{\text{NSRT}}$, the timer expires in a maximum duration of 22 ms. If this happens, the phantom drive is deasserted and remains so until the next falling edge of $\overline{\text{NSRT}}$. The watchdog timer requires no external timing components. When the phantom drive is deasserted, the phantom-drive lines are actively pulled low, reaching a level of 1 V or less within 50 ms.

The dc voltage from PHOUTA and PHOUTB is superimposed on the transmit-signal pair to the trunk-coupling unit (TCU) to request that the station be inserted into the ring. This is achieved by connecting them to the center of the secondary winding of the transmit-isolation transformer. Since PHOUTA and PHOUTB are connected to the media side of the isolation transformer, they require extensive protection against line surges. A capacitor is connected between the two phantom lines to provide an ac path for the transmit signal. PHOUTA and PHOUTB independently drive the dc voltage on each of the transmit lines, allowing for independent wire-fault detection on each.

The phantom voltage is detected by the TCU, causing the external wrap path from the transmitter outputs back to the receiver inputs to be broken, and the ring to be broken. A signal connection is then established from the ring to the receiver inputs and from the transmitter outputs to the ring. The return current from the dc-phantom voltage on the transmit pair is returned to the station by way of the receive pair. This provides some measure of wire-fault detection on the receive lines. The phantom-drive outputs are current limited to prevent damage if short-circuited. They detect either an abnormally high or an abnormally low load current at either output, corresponding to a short or an open circuit in the ring or TCU wiring. Either fault causes the wire-fault indicator output, $\overline{\text{WFLT}}$, to be driven low. The logic state of $\overline{\text{WFLT}}$ is high when the phantom drive is not active.

frequency acquisition and $\overline{\text{REDY}}$

Unlike its predecessors, the TMS3805x family, the data-recovery PLL of the TI380C60A does not require constant frequency monitoring; neither is it necessary to recenter its frequency by way of the FRAQ control line. However, it is necessary to provide the interaction with the TI380C2x or other commprocessors that expect to perform this frequency-management task.

When the TI380C2x asserts FRAQ, it initiates a reset of the clock-recovery PLL. The $\overline{\text{REDY}}$ signal is deasserted for the duration of this action and reasserted low when it is complete (a maximum of 3 μs later). This low-going transition of $\overline{\text{REDY}}$ is required by the TI380C2x following the setting of FRAQ high to indicate to the commprocessor that any frequency error that it detected has been corrected. In fact, the TI380C60A never requires FRAQ to be asserted after the PLL has been initialized. This interaction is provided purely for the benefit of the TI380C2x. $\overline{\text{REDY}}$ is also de-asserted if no incoming transitions are detected by the rate error function.

When the TI380C60A is used as a standalone, it is necessary to initialize the device once following initial power-up. This can be done in one of the three ways:

- A falling edge on FRAQ after power has stabilized
- A rising edge on $\overline{\text{PWRDN}}$ after power has stabilized. [However, note that the clock signals (PXTAL, RCLK, OSC32) will not operate while $\overline{\text{PWRDN}}$ is low.]
- By toggling the S4/$\overline{16}$ pin in either direction after power has stabilized

rate error ($\overline{\text{RATER}}$) function

$\overline{\text{RATER}}$ provides an indication that incoming data transitions are present on the RCV+/RCV– pair but the rate of transitions is outside the range that would be expected for the ring speed selected by S4/$\overline{16}$. $\overline{\text{RATER}}$ is not asserted low if no incoming transitions are present. In wrap mode, the rate error function monitors the transitions on the DRVR+/DRVR– pair.

The rate error function interprets 16 or more transitions in a 1.5-μs period as valid 16-Mbps data. It interprets 15 or less transitions in a 1.5-μs period as 4-Mbps data. One transition or less in a 1.5-μs period is interpreted as no incoming transitions—in which case, $\overline{\text{RATER}}$ and $\overline{\text{REDY}}$ are not asserted.

disable and power-down mode

The TI380C60A can be disabled by either NABL or $\overline{\text{PWRDN}}$. If NABL is taken low, the output buffers of the commproccessor interface are placed in the high-impedance state; however, internal logic continues to operate. Phantom drive is disabled, but XMT+ and XMT– are driven to a low value to sustain line termination in token-ring/Ethernet 10 Base-T applications that share magnetics.

If $\overline{\text{PWRDN}}$ is taken low, all outputs are in the high-impedance state and all internal logic is powered down, bringing power consumption to a very low level. Upon removing $\overline{\text{PWRDN}}$, the device resets and initializes itself. This process can take up to 2 ms and care should be taken to ensure that the system does not require stable clocks during this period. In particular, slow-clock errors can be seen by a TI380C2x commprocessor in a dual-physical-layer application if the TI380C60A is powered down when not in use.

test facilities

A 5-pin test port is included for production-device testing. While the signals are similar to ports defined by IEEE-1149.1, this port is not compliant with the standard and the port is not suitable for in-circuit test.

ATEST gives access to the filter of the internal PLL. This pin is also for production test purposes, and no connection should be made to it in an application.

absolute maximum ratings over operating case temperature range (unless otherwise noted)†

Supply voltage range, V_{DD} (see Note 2) . . . . . – 0.5 V to 7 V
Input voltage range (see Notes 2 and 3) . . . . . – 0.5 V to 7 V
Output voltage range . . . . . – 0.5 V to 7 V
Power dissipation (see Note 4) . . . . . 0.75 W
ESD protection, V_{ESD} (see Note 5) . . . . . 1500 V
Junction-to-ambient package thermal impedance @ 0 LFPM air flow, $\Theta_{ja}(0)$ . . . . . 80.5°C/W
Junction-to-ambient package thermal impedance @ 100 LFPM air flow, $\Theta_{ja}(100)$ . . . . . 64.9°C/W
Junction-to-case package thermal impedance, Θ_{jc} . . . . . 8.9°C/W
Operating case temperature range, T_C . . . . . 0°C to 95°C
Storage temperature range, T_{stg} . . . . . – 65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 2. All voltage values are with respect to V_{SS} unless otherwise noted.
3. Inputs can be taken to more negative voltages if the current is limited to 20 mA.
4. Maximum power dissipation per package
5. The device is classified as ESDS class 1 (A:1500). ESD protection measured per MIL-STD-883C, Method 3015.

recommended operating conditions‡

			MIN	NOM	MAX	UNIT
V_{DD}	Supply voltage	All V_{DD}	4.75	5	5.25	V
V_{IH}	High-level input voltage (see Note 6)	TTL inputs	2		V_{DD} + 0.3	V
V_{IL}	Low-level input voltage (see Notes 6 and 7)	TTL inputs	– 0.3		0.8	V
V_{IB}	Receiver input bias voltage	See Note 8	V_{SB} – 1		V_{SB} + 1	V
I_{OH}	High-level output current (see Note 6)	TTL outputs			– 0.2	mA
I_{OL}	Low-level output current (see Note 6)	TTL outputs			2	mA
T_C	Operating case temperature range		0		95	°C

‡ Recommended operating conditions indicate the conditions that must be met to ensure that the device functions as intended and meets the detailed electrical specifications. Unless otherwise noted, all electrical specifications apply for all recommended operating conditions. Voltages are measured with respect to the device V_{SS} pins. Currents into the device are considered to be positive.

NOTES: 6. The TTL input and TTL output pins are identified in the pin functions table.
7. Inputs can be taken to more negative voltages if the I_{DD} current is limited to 20 mA.
8. V_{SB} is the self-bias voltage of the input pair RCV+ and RCV–. It is defined as $V_{SB} = (V_{SB+} + V_{SB-}) / 2$ (where V_{SB+} is the self-bias voltage of RCV+; V_{SB-} is the self-bias voltage of RCV–). The self-bias voltage of both pins is approximately $V_{DD} / 2$.

electrical characteristics over recommended ranges of supply voltage and operating case temperature (unless otherwise noted)

TTL input and output pins (see Note 6)

PARAMETER			TEST CONDITIONS§	MIN	TYP	MAX	UNIT
I_{IH}	High-level input current		$V_I = V_{DD}$	– 20		20	µA
I_{IL}	Low-level input current		V_I = OV ($\overline{PWRDN}$ = High)	– 100		– 20	µA
V_{OH}	High-level output voltage		I_{OH} = – 0.2 mA	2.6			V
V_{OL}	Low-level output voltage		I_{OL} = 2 mA			0.45	V
I_{OZH}	Off-state output current with high-level voltage applied		V_O = 2.7 V	– 20		20	µA
I_{OZL}	Off-state output current with low-level voltage applied		V_O = 0.4 V	– 20		20	µA
I_{DD}	Supply current	Normal mode	V_{DD} = MAX		120		mA
		Power-down mode			10		mA

§ For conditions shown as MIN/MAX, use the appropriate value specified under recommended operating conditions.

NOTE 6: The TTL input and TTL output pins are identified in the pin functions table.

electrical characteristics over recommended ranges of supply voltage and operating case temperature (unless otherwise noted) (continued)

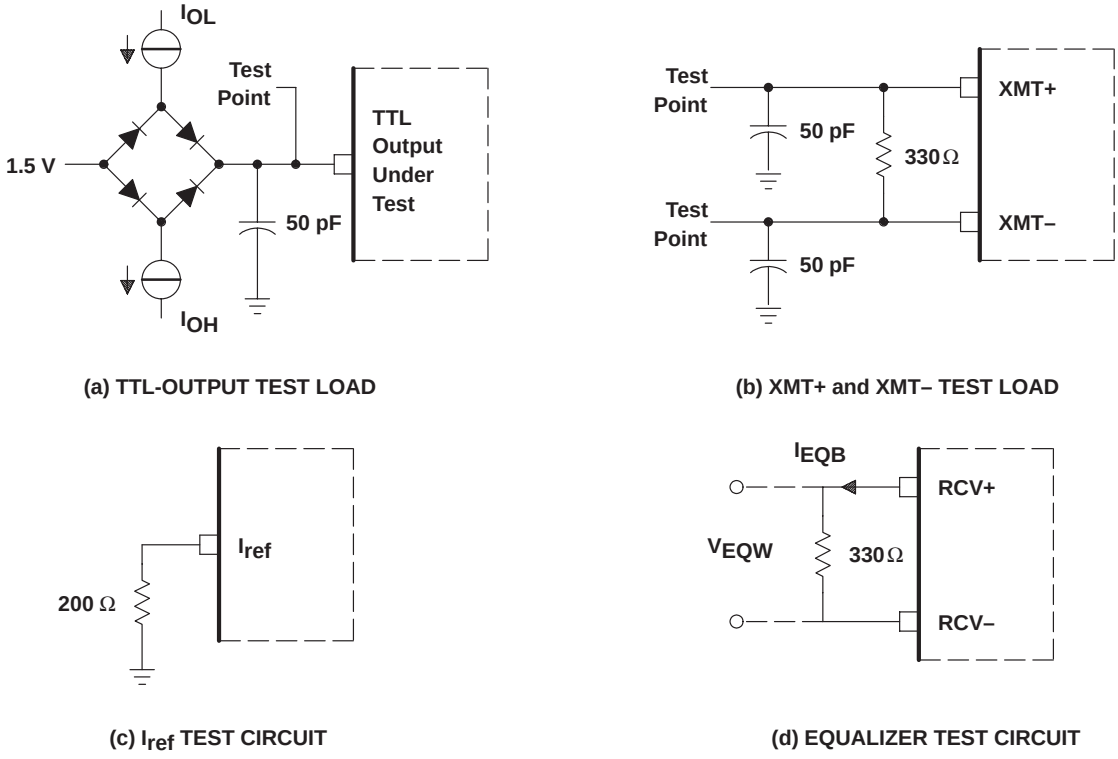
receiver input (RCV+ and RCV–)

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
V_{T+}	Rising input threshold voltage	$V_{ICM} = V_{SB}$, See Notes 8 and 9, and Figure 6		50	mV
V_{T-}	Falling input threshold voltage	$V_{ICM} = V_{SB}$, See Notes 8 and 9, and Figure 6	– 50		mV
V_{AT}	Asymmetry threshold voltage, $(V_{T+} + V_{T-}) \div 2$	$V_{ICM} = V_{SB}$, See Notes 8 and 9, and Figure 6	– 15	15	mV
V_{CM+}	Rising input common-mode rejection $[V_{T+} (@V_{SB} + 0.5\ V) – V_{T+} (@V_{SB} – 0.5\ V)]$	See Notes 8 and 9, and Figure 6	– 30	30	mV
V_{CM-}	Falling input common-mode rejection $[V_{T-} (@V_{SB} + 0.5\ V) – V_{T-} (@V_{SB} – 0.5\ V)]$	See Notes 8 and 9, and Figure 6	– 30	30	mV
$I_{I(RCV)}$	Receiver input current	Both inputs at V_{SB}, See Note 8 and Figure 6	– 10	10	µA
		Input under test at $V_{SB} + 1\ V$, Other input at $V_{SB} – 1\ V$, See Note 8 and Figure 6	10	60	
		Input under test at $V_{SB} – 1\ V$, Other input at $V_{SB} + 1\ V$, See Note 8 and Figure 6	–10	–60	
I_{EQB}	Equalizer bias current	RCV+ at 4 V, RCV– at 1 V or RCV+ at 1 V, RCV– at 4 V See Figure 4d	1	2.2	mA
V_{EQW}	Equalizer wrap voltage	$\overline{WRAP}$ = low, See Figure 4d	300	700	mV

NOTES: 8. V_{SB} is the self-bias voltage of the input pair RCV+ and RCV–. It is defined as $V_{SB} = (V_{SB+} + V_{SB-}) / 2$ (where V_{SB+} is the self-bias voltage of RCV+; V_{SB-} is the self-bias voltage of RCV–). The self-bias voltage of both pins is approximately $V_{DD} / 2$.

9. V_{ICM} is the common-mode voltage applied to RCV+ and RCV–.

electrical characteristics over recommended ranges of supply voltage and operating case temperature (unless otherwise noted) (continued)



(a) TTL-OUTPUT TEST LOAD

(b) XMT+ and XMT– TEST LOAD

(c) I_{ref} TEST CIRCUIT

(d) EQUALIZER TEST CIRCUIT

Figure 4. Test and Load Circuits

electrical characteristics over recommended ranges of supply voltage and operating case temperature (unless otherwise noted) (continued)

phantom driver (PHOUTA and PHOUTB)

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
V_{OH}	High-level output voltage	I_{OH} = – 1 mA	4.1		V
		I_{OH} = – 2 mA	3.8		V
I_{OS}	Short-circuit output current	V_O = 0 V	– 4	– 20	mA
I_{OL}	Low-level output current	$V_O = V_{DD}$	1	10	mA
I_{OZH}	Off-state output current with high-level voltage applied	$V_O = V_{DD}$	– 100	100	μA
I_{OZL}	Off-state output current with low-level voltage applied	V_O = 0 V	– 100	100	μA

wire fault ($\overline{WFLT}$) (see Notes 10 and 11)

PARAMETER		MIN	MAX	UNIT
$R_{L(S)}$	Phantom-drive load resistance detected as short circuit		0.15	kΩ
$R_{L(O)}$	Phantom-drive load resistance detected as open circuit	50		kΩ
$R_{L(N)}$	Phantom-drive load resistance detected as normal	2.9	5.5	kΩ

NOTES: 10. The wire-fault circuit recognizes a fault condition for any phantom-drive load resistance to ground greater than $R_{L(O)}$ or any load resistance less than $R_{L(S)}$. Any resistance in the range specified for $R_{L(N)}$ is not recognized as a wire fault. A fault condition on either PHOUTA or PHOUTB results in $\overline{WFLT}$ being asserted (low).

11. Resistor [$R_{L(S)}$, $R_{L(O)}$, $R_{L(N)}$] connected from output under test to ground, other output loaded with 4.1 Ω to ground.

PLL characteristics

PARAMETER	TEST CONDITIONS	MIN	MAX	UNIT
Reference PLL operating filter voltage	$t_{c(XT1)}$ = 125 ns	1.8	4	V

crystal-oscillator characteristics

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
$V_{IB(XT1)}$	Input self-bias voltage		1.8	4	V
$I_{OH(XT2)}$	High-level output current	$V_{(XT2)} = V_{SB(XT1)}$ $V_{(XT1)} = V_{SB(XT1)}$ + 0.5 V	– 2.5	– 6.5	mA
$I_{OL(XT2)}$	Low-level output current	$V_{(XT2)} = V_{SB(XT1)}$ $V_{(XT1)} = V_{SB(XT1)}$ – 0.5 V	0.4	1.3	mA

switching characteristics over recommended range of supply voltage (unless otherwise noted)

transmitter-drive characteristics

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
$V_{PP(XMT)}$	XMT+ / XMT– peak-to-peak voltage (see Note 12)	V_{DD} = 4.75 V, See Figures 4 and 5	8.2		V
		V_{DD} = 5.25 V, See Figures 4 and 5		10.3	

NOTE 12: $V_{PP(XMT)}$ is determined by:
$V_{OH(XMT+)} + V_{OH(XMT–)} – V_{OL(XMT+)} – V_{OL(XMT–)}$

electrical characteristics over recommended ranges of supply voltage and operating case temperature (unless otherwise noted) (continued)

transmitter switching characteristics (see Figures 4 and 5)

PARAMETER	TEST CONDITIONS	MIN	MAX	UNIT
XMT+/XMT– skew (see Note 13)	$t_{sk(DRV)}$ = – 1 ns	– 3	+ 3	ns
	$t_{sk(DRV)}$ = + 1 ns	– 3	+ 3	ns
XMT+/XMT– asymmetry (see Note 14)	$t_{sk(DRV)}$ = –1 ns	– 2	+ 2	ns
	$t_{sk(DRV)}$ = + 1 ns	– 2	+ 2	ns

NOTES: 13. XMT+/XMT– skew is determined by: $t_{d(XMT+\ H)} - t_{d(XMT-\ L)}$ or $t_{d(XMT+\ L)} - t_{d(XMT-\ H)}$

14. XMT+/XMT– asymmetry is determined by:

$$\frac{t_{d(XMT+L)} + t_{d(XMT-H)}}{2} - \frac{t_{d(XMT+H)} + t_{d(XMT-L)}}{2}$$

PARAMETER MEASUREMENT INFORMATION

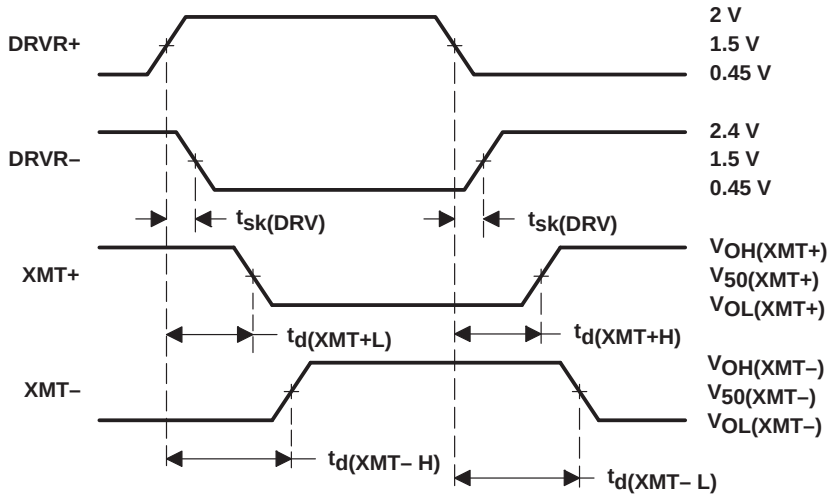


Figure 5. Transmitter Timing

clock and data switching characteristics over recommended range of supply voltage, $t_{c(XT1)}$ = 125 ns (see Figure 6)

		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{c(XT1)}$	Cycle time of clock applied to XT1			125		ns
$t_{w(OSC32H)}$	Pulse duration, OSC32 high		10			ns
$t_{w(OSC32L)}$	Pulse duration, OSC32 low		12			ns
$t_{w(PXTALL)}$	Pulse duration, PXTAL low	16-Mbps mode	12			ns
		4-Mbps mode	46			ns
$t_{w(PXTALH)}$	Pulse duration, PXTAL high	16-Mbps mode	10			ns
		4-Mbps mode	46			ns
$t_{w(RCLKL)}$	Pulse duration, RCLK low	16-Mbps mode	12			ns
		4-Mbps mode	46			ns
$t_{w(RCLKH)}$	Pulse duration, RCLK high	16-Mbps mode	10			ns
		4-Mbps mode	46			ns
$t_{su(RCVR)}$	Setup time, RCVR valid to RCLK rising edge	16-Mbps mode	18			ns
$t_{h(RCVR)}$	Hold time, RCVR valid after RCLK rising edge	16-Mbps mode	2.5			ns

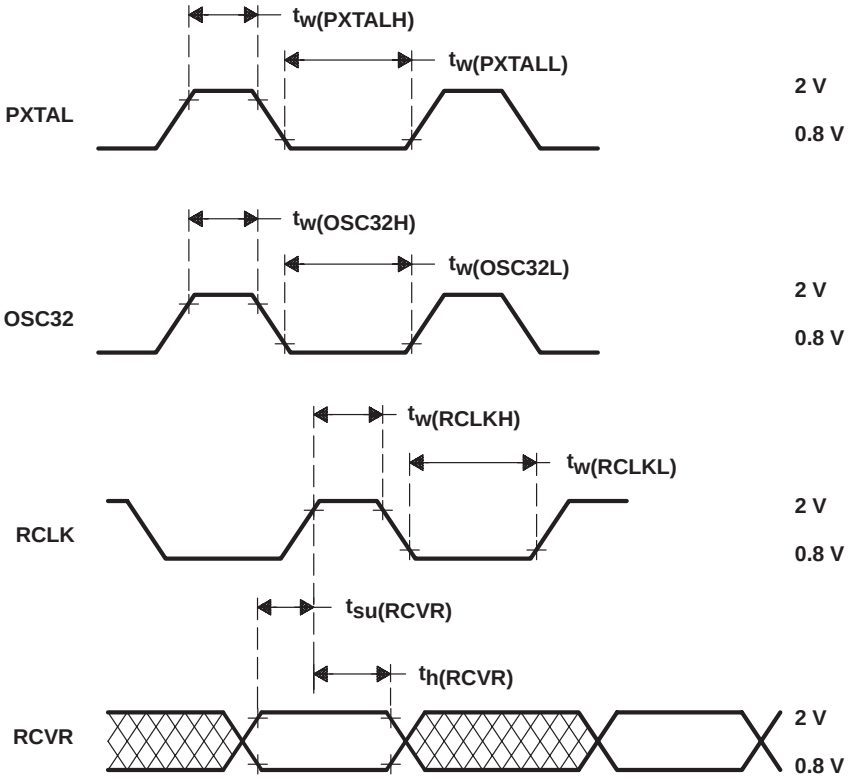
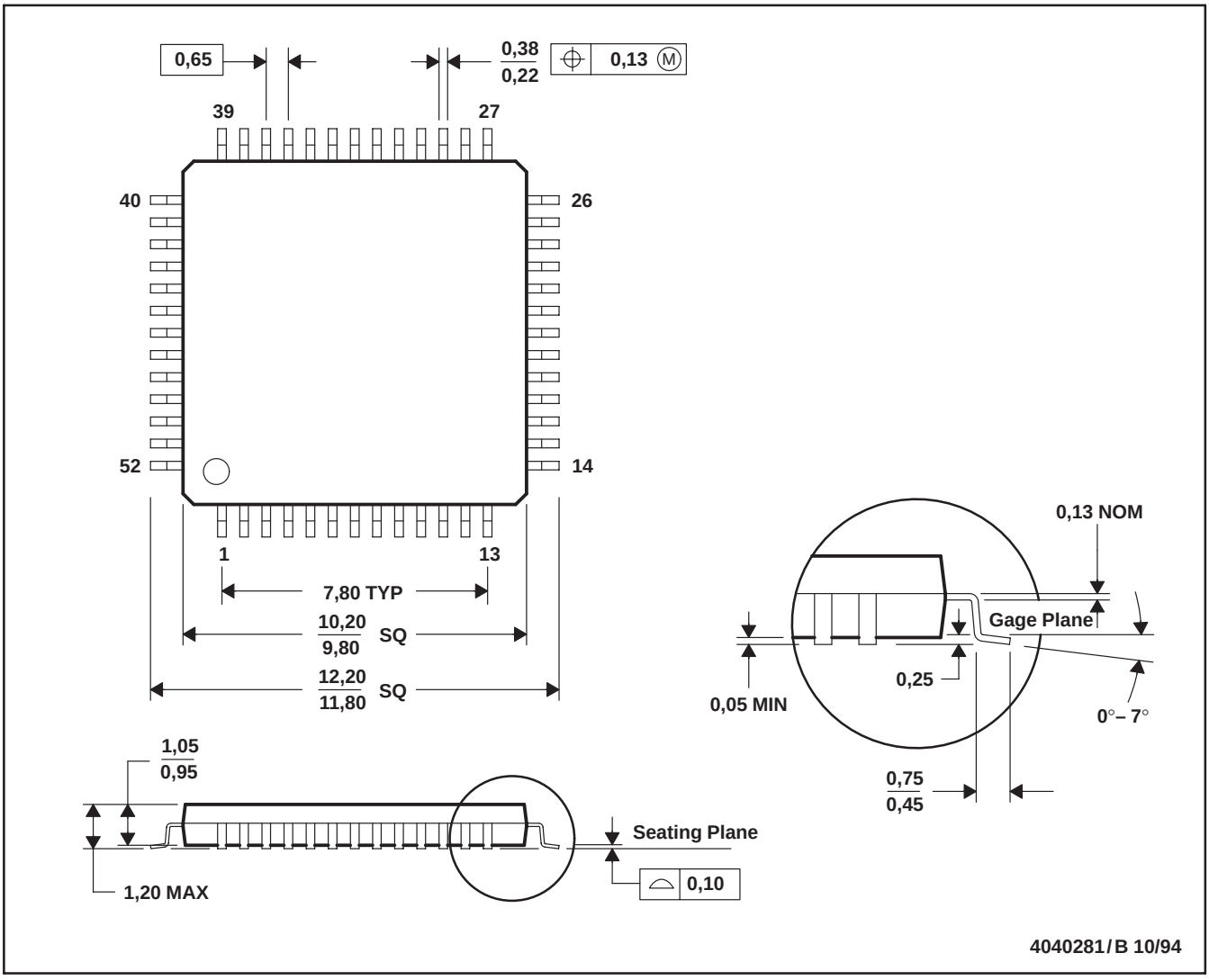


Figure 6. PXTAL, OSC32, RCLK, and RCVR Timing

MECHANICAL DATA

PAH (S-PQFP-G52) **PLASTIC QUAD FLATPACK**



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Falls within JEDEC MO-136

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