Siliconix incorporated

DG526/527
16-Channel and Dual 8-Channel Latchable Multiplexers

FEATURES

- TTL Compatible
- 44 V Power Supply Rating
- On-board Address Latches
- $r_{DS(ON)}$ < 400 Ω
- Break-Before-Make

BENEFITS

- Easily Interfaced
- Increased Analog Signal Range
- Microprocessor Bus Compatible
- Improved System Accuracy
- Reduced Crosstalk

APPLICATIONS

- Data Acquisition Systems
- Automatic Test Equipment
- Avionics And Military Systems
- Communication Systems
- Microprocessor Controlled Systems
- Audio Signal Multiplexing

DESCRIPTION

DG526 and DG527 are 16 and 8-channel analog multiplexers, respectively, with on-chip address and control latches to simplify design in microprocessor based applications. Break-Before-Make switching action protects against momentary shorting of the input signals. Designed on the Siliconix PLUS-40 CMOS process, each bidirectional switch features low 400 Ω ON resistance over the full analog range, and will block signals to 30 V peak-to-peak in the unselected channels. All logic levels are TTL-compatible. An epitaxial layer prevents latch up.

DG526 is a 16-channel single-ended analog multiplexer designed to connect 1 of 16 inputs to a common output as determined by a 4-bit binary address (A_0, A_1, A_2, A_3). DG527, an 8-channel dual analog multiplexer, is designed to connect 1 of 8 differential inputs to a common differential output as determined by its 3-bit binary address (A_0, A_1, A_2) logic.

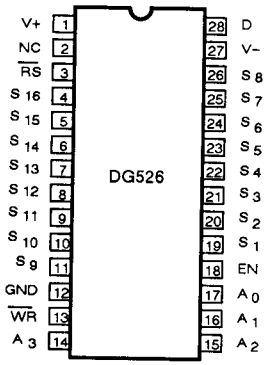
The on-board TTL-compatible address latches simplify the digital interface design and reduce board space in bus-controlled systems such as data acquisition systems, process controls, avionics, and ATE. The DG526 is available in 28-pin CerDIP in the military, A suffix (-55 to 125°C), industrial, B suffix (-25 to 85°C) temperature ranges, and in the plastic DIP for commercial, C suffix (0 to 70°C) temperature operation.

For more information on the DG526 and DG527, please refer to Siliconix Application Note AN83-4.

5

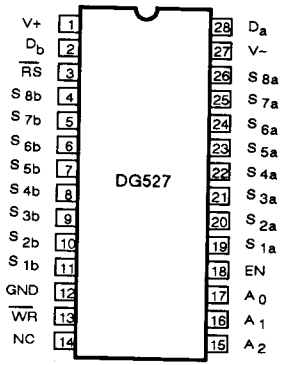
PIN CONFIGURATION

Dual-In-Line Package
Top View

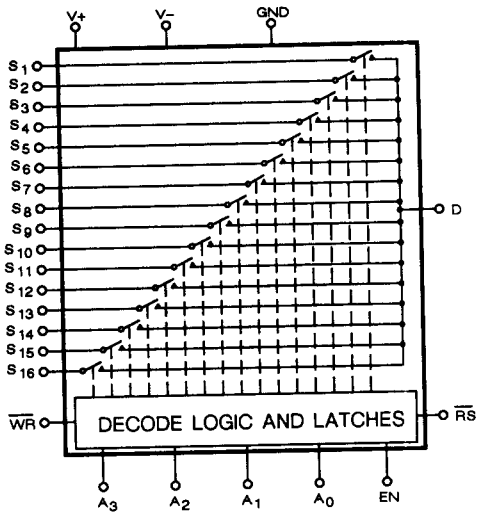


Order Numbers:
CerDIP: DG526AK, DG526BK, DG526CK, DG527AK, DG527BK, DG527CK
Plastic: DG526CJ, DG527CJ

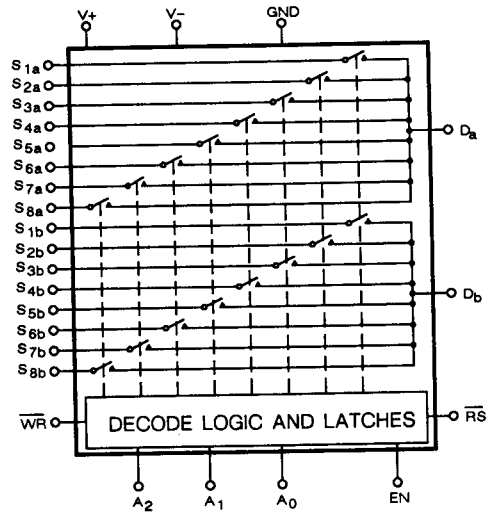
Dual-In-Line Package
Top View



FUNCTIONAL BLOCK DIAGRAM



DG526
16 Channel Single Ended Multiplexer



DG527
Differential 8 Channel Multiplexer

ABSOLUTE MAXIMUM RATINGS

Voltage Referenced to V-

V+ ..... 44 V

GND ..... 25 V

Digital Inputs, V_S, V_D[h] ..... (V-) -2 V to (V+) +2 V or ..... 20 mA, whichever occurs first.

Current (Any Terminal Except S or D) ..... 30 mA

Continuous Current, S or D ..... 20 mA

Peak Current, S or D
(Pulsed at 1 ms, 10% Duty Cycle Max) ..... 40 mA

Operating Temperature (A Suffix) ..... -55 to 125°C
(B Suffix) ..... -25 to 85°C
(C Suffix) ..... 0 to 70°C

Storage Temperature (A & B Suffix) ..... -65 to 150°C
(C Suffix) ..... -65 to 125°C

Power dissipation (Package)*
28-Pin CerDIP DIP** ..... 1046 mW
28-Pin Plastic DIP** ..... 1046 mW

* All leads soldered or welded to PC board.
** Derate 6.5 mW/°C above 25°C.

ELECTRICAL CHARACTERISTICS [a]

PARAMETER		SYMBOL	Test Conditions Unless Otherwise Specified: V+ = 15 V, V− = −15 V, GND = 0, $\overline{WR}$ = 0, $\overline{RS}$ = 2.4 V		LIMITS 1=25°C, 2=125,70,85 °C, 3=−55,−25,0 °C		ALL SUFFIXES		UNIT
					TEMP	TYP [d]	MIN [b]	MAX [b]	
SWITCH									
Analog Signal Range [c]		V_{ANALOG}			1,2,3		−15	15	V
Drain-Source [e] ON Resistance		$r_{DS(ON)}$	V_D = ±10 V, V_{AL} = 0.8 V, I_S = −200 µA, V_{AH} = 2.4 V		1, 3 2	250		400 500	Ω
Greatest Change in $r_{DS(ON)}$ Between Channels [f]		$\Delta r_{DS(ON)}$	−10 V < V_S < 10 V		1	6			%
Source OFF Leakage Current		$I_{S(OFF)}$	V_{EN} = 0 V	V_S = ±10 V, V_D = ∓10 V	1 2	0.02	−1 −50	1 50	nA
Drain OFF Leakage Current	DG526	$I_{D(OFF)}$		V_D = ±10 V, V_S = ∓10 V	1 2	0.2	−10 −300	10 300	
	DG527			V_D = ±10 V, V_S = ∓10 V	1 2	0.2	−10 −200	10 200	
Drain ON Leakage Current [e,g]	DG526	$I_{D(ON)}$	V_S = V_D = ±10 V, V_{EN} = 2.4 V, V_{AL} = 0.8 V, V_{AH} = 2.4 V		1 2	0.2	−10 −300	10 300	
	DG527				1 2	0.2	−10 −200	10 200	
INPUT									
Logic Input Current Input Voltage High		I_{AH}	V_A = 2.4 V		1 2	0.02	−10 −30	20 30	µA
			V_A = 15 V		1 2	0.02	−10 −30	10 30	
Logic Input Current Input Voltage Low		I_{AL}	V_{EN} = 0 or 2.4 V, V_A = 0 V, $\overline{RS}$ = 0 V, $\overline{WR}$ = 0 V		1 2	0.01	−10 −30	10 30	
DYNAMIC									
Switching Time of Multiplexer		t_{TRANS}	See Figure 3		1	0.65		1	µs
Break-Before-Make Interval		t_{OPEN}	See Figure 5		1	0.2			
Enable and Write Turn ON Time		$t_{ON(EN,\overline{WR})}$	See Figure 4 and 6		1	0.7		1.5	
Enable and Reset Turn OFF Time		$t_{OFF(EN,\overline{RS})}$	See Figure 4 and 7		1	0.4		1	
Charge Injection		Q	See Figure 8		1	10			pC
OFF Isolation			V_{EN} = 0, R_L = 1 kΩ, C_L = 15 pF, V_S = 7 V_{RMS}, f = 500 kHz		1	55			dB
Logic Input Capacitance		C_{in}	f = 1 MHz		1	6			pF

5

ELECTRICAL CHARACTERISTICS [a]

PARAMETER		SYMBOL	Test Conditions Unless Otherwise Specified: V+ = 15 V, V− = −15 V, GND = 0, $\overline{WR}$ = 0, $\overline{RS}$ = 2.4 V		LIMITS 1=25°C 2=125,70,85 °C 3=−55,−25,0 °C TEMP	TYP [d]	ALL SUFFIXES MIN [b]	MAX [b]	UNIT
DYNAMIC (Cont'd)									
Source OFF Capacitance		$C_{S(OFF)}$	V_{EN} = 0, f = 140 kHz	V_S = 0	1	10			PF
Drain OFF Capacitance	DG526	$C_{D(OFF)}$	V_{EN} = 0, f = 140 kHz	V_D = 0	1	65			PF
	DG527	$C_{D(OFF)}$	V_{EN} = 0, f = 140 kHz	V_D = 0	1	35			PF
MINIMUM INPUT TIMING REQUIREMENTS									
$\overline{WR}$ Pulse Width		t_{WW}	See Figure 1		1,2,3	260	300		ns
A_X, $\overline{EN}$ Data Valid to $\overline{WR}$		t_{DW}	(Stabilization Time) See Figure 1		1,2,3	150	180		ns
A_X, $\overline{EN}$ Data Valid after $\overline{WR}$		t_{WD}	(Hold Time) See Figure 1		1,2,3	20	30		ns
$\overline{RS}$ Pulse Width [i]		$t_{\overline{RS}}$	See Figure 2 V_S = 5 V		1,2,3	350	500		ns
SUPPLY									
Positive Supply Current		I+	V_{EN} = 0, V_A = 0		1 2,3	2.0		3.0 4.5	mA
Negative Supply Current		I−	V_{EN} = 0, V_A = 0		1 2,3	−1.2	−2.0 −3.2		mA

NOTES:

a. Refer to PROCESS OPTION FLOWCHART for additional information.

b. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.

c. Guaranteed by design, not subject to production test.

d. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.

e. Sequence each switch ON.

f. $\Delta r_{DS(ON)} = \left(\frac{r_{DS(ON)}\ MAX - r_{DS(ON)}\ MIN}{r_{DS(ON)}\ AVE} \right)$

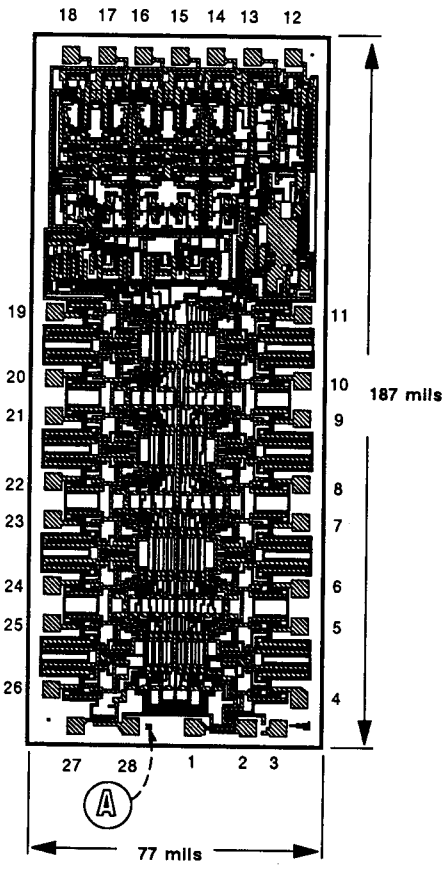
g. $I_{D(ON)}$ is leakage from driver into "ON" switch.

h. Signals on S_X, D_X, IN_X exceeding V+ or V− will be clamped by internal diodes. Limit forward diode current to maximum current ratings.

i. Period of Reset ($\overline{RS}$) pulse must be at least 50 µs during or after power ON.

DIE TOPOGRAPHIES

DG526



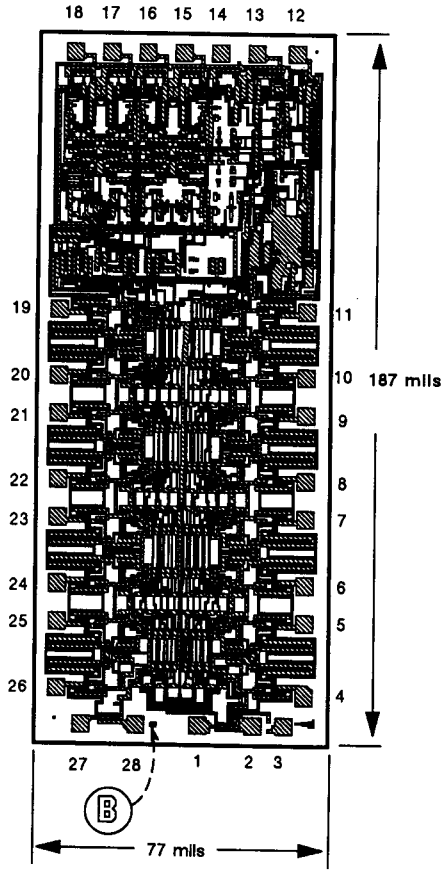
20X

Pad No.	Function	Pad No.	Function
1	V+ (substrate)	15	A_2
2	No connection	16	A_1
3	RS	17	A_0
4	S_{16}	18	EN
5	S_{15}	19	S_1
6	S_{13}	20	S_2
7	S_{14}	21	S_3
8	S_{12}	22	S_4
9	S_{11}	23	S_5
10	S_{10}	24	S_6
11	S_9	25	S_7
12	GND	26	S_8
13	$\overline{WR}$	27	V-
14	A_3	28	D

ICMNA

10 Resistors	177 P-channel enhancement MOSFET
14 Diodes	201 N-channel enhancement MOSFET
2 Zener Diodes	2 PNP Bipolar Transistors

DG527



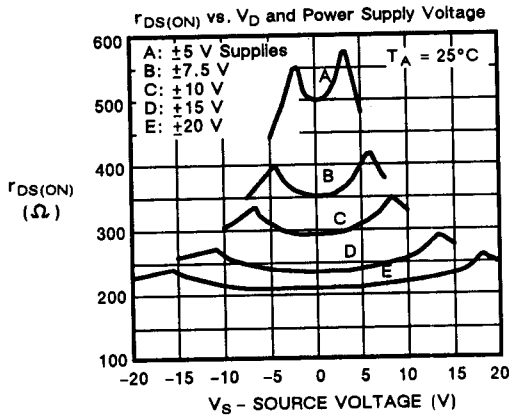
20X

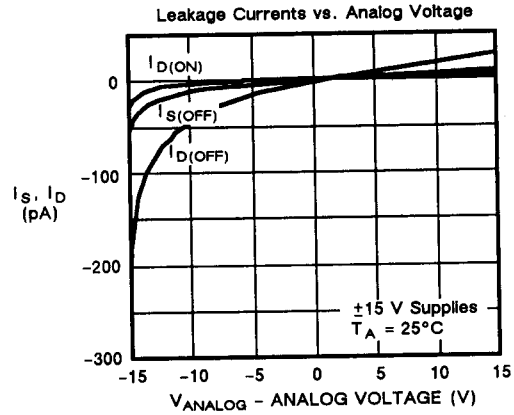
Pad No.	Function	Pad No.	Function
1	V+ (substrate)	15	A_2
2	D	16	A_1
3	RS	17	A_0
4	S_{8b}	18	EN
5	S_{7b}	19	S_{1a}
6	S_{6b}	20	S_{2a}
7	S_{5b}	21	S_{3a}
8	S_{4b}	22	S_{4a}
9	S_{3b}	23	S_{5a}
10	S_{2b}	24	S_{6a}
11	S_9	25	S_{7a}
12	GND	26	S_{8a}
13	$\overline{WR}$	27	V-
14	No Connection	28	D_a

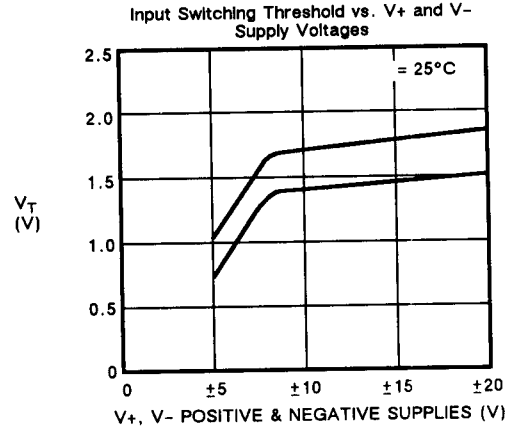
ICMNB

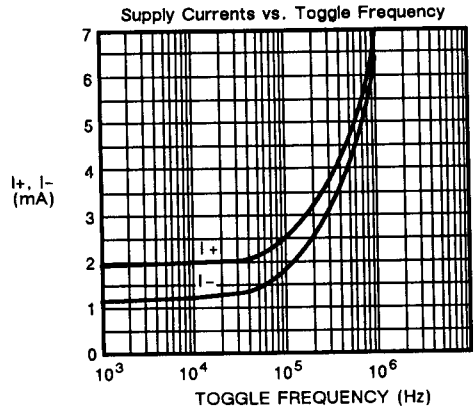
9 Resistors	164 P-channel enhancement MOSFET
16 Diodes	189 N-channel enhancement MOSFET
2 Zener Diodes	2 PNP Bipolar Transistors

TYPICAL CHARACTERSITICS









TRUTH TABLES

DG526

A_3	A_2	A_1	A_0	EN	$\overline{WR}$	$\overline{RS}$	On Switch
Latching							
X	X	X	X	X	↓	1	Maintains previous switch condition
Reset							
X	X	X	X	X	X	0	NONE (latches cleared)
Transparent Operation							
X	X	X	X	0	0	1	NONE
0	0	0	0	1	0	1	1
0	0	0	1	1	0	1	2
0	0	1	0	1	0	1	3
0	0	1	1	1	0	1	4
0	1	0	0	1	0	1	5
0	1	0	1	1	0	1	6
0	1	1	0	1	0	1	7
0	1	1	1	1	0	1	8
1	0	0	0	1	0	1	9
1	0	0	1	1	0	1	10
1	0	1	0	1	0	1	11
1	0	1	1	1	0	1	12
1	1	0	0	1	0	1	13
1	1	0	1	1	0	1	14
1	1	1	0	1	0	1	15
1	1	1	1	1	0	1	16

DG527

A_2	A_1	A_0	EN	$\overline{WR}$	$\overline{RS}$	On Switch
Latching						
X	X	X	X	↓	1	Maintains previous switch condition
Reset						
X	X	X	X	X	0	NONE (latches cleared)
Transparent Operation						
X	X	X	0	0	1	NONE
0	0	0	1	0	1	1
0	0	1	1	0	1	2
0	1	0	1	0	1	3
0	1	1	1	0	1	4
1	0	0	1	0	1	5
1	0	1	1	0	1	6
1	1	0	1	0	1	7
1	1	1	1	0	1	8

Logic "1": $V_{AH} > 2.4$ V

Logic "0" $V_{AL} < 0.8$ V

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TIMING DIAGRAMS

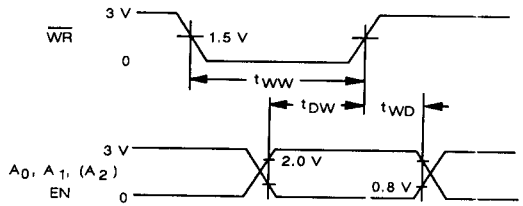

Figure 1

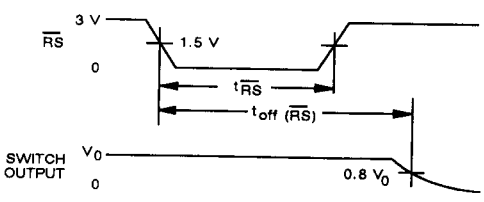

Figure 2

TRANSITION TIME TEST CIRCUIT

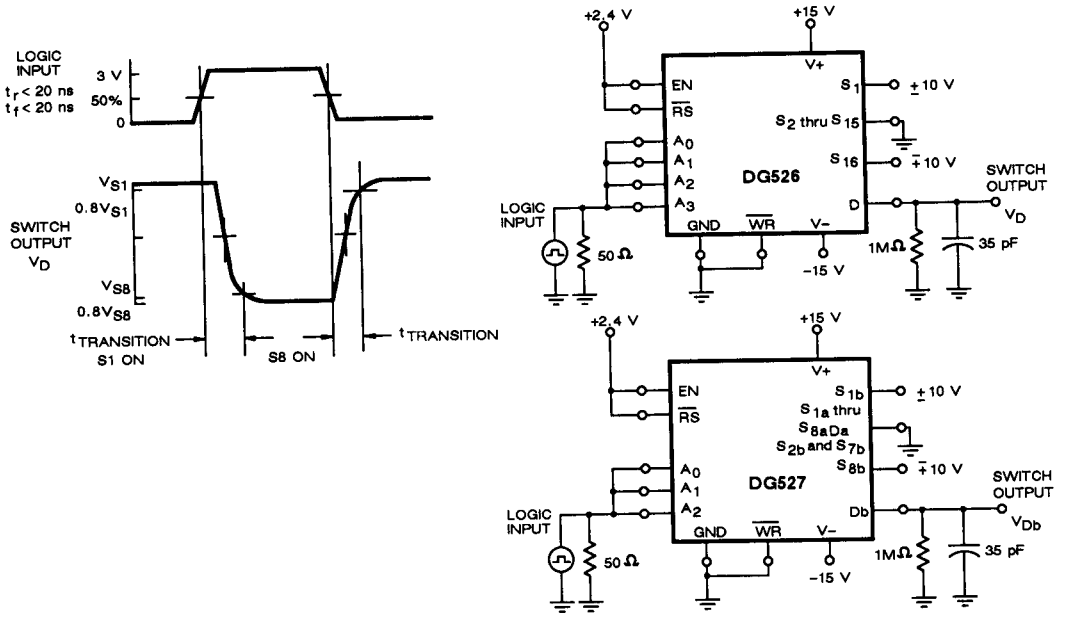

Figure 3

ENABLE t_{ON}/t_{OFF} TIME TEST CIRCUIT

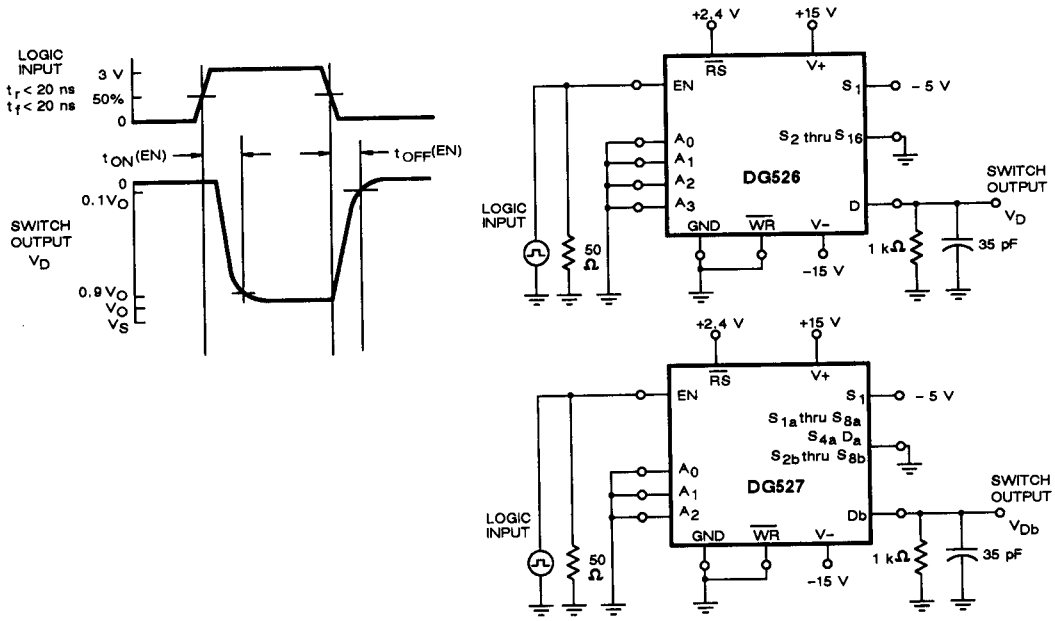

Figure 4

OPEN TIME (B.B.M.) INTERVAL TEST CIRCUIT

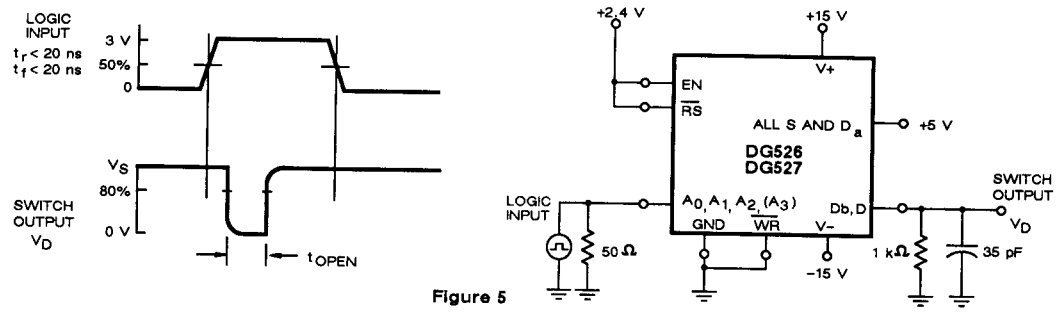

Figure 5

WRITE TURN-ON TIME $t_{ON(\overline{WR})}$ TEST CIRCUIT

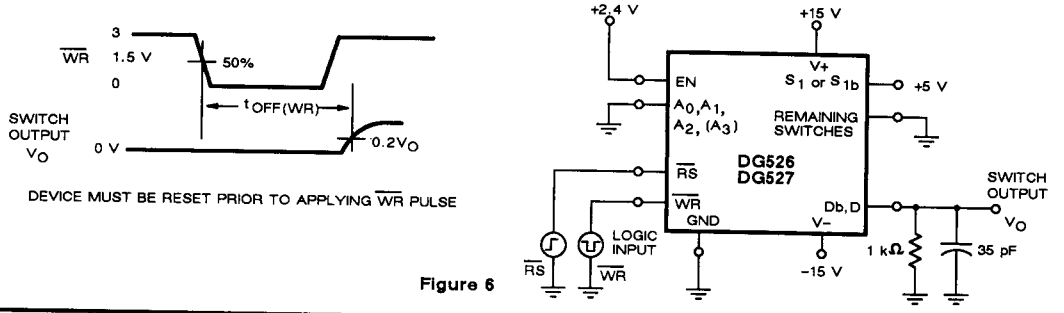

Figure 6

RESET TURN-OFF TIME $t_{OFF(\overline{RS})}$ TEST CIRCUIT

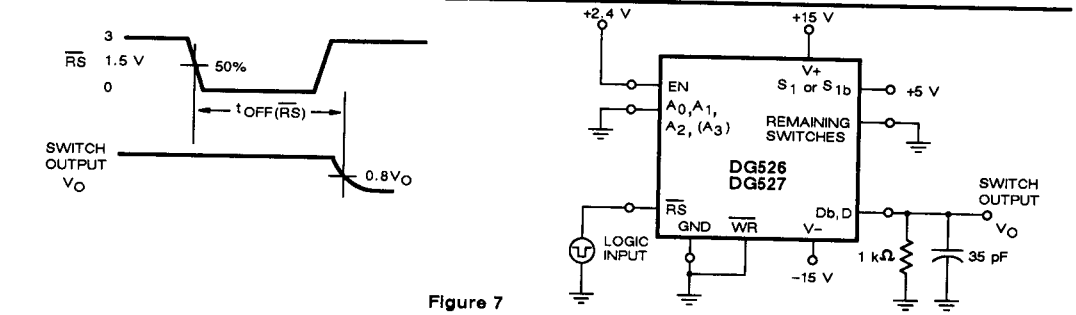

Figure 7

CHARGE INJECTION TEST CIRCUIT

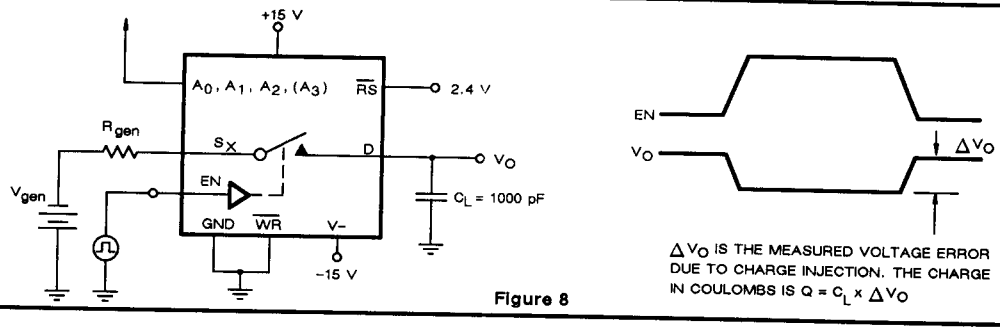

Figure 8

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DETAILED DESCRIPTION

The internal structure of the DG526 and DG527 includes a 5 V logic interface with input protection circuitry followed by a latch, level shifter, decoder and finally the switch constructed with parallel N and P-channel MOSFETs (see figure 9).

The input protection on the logic lines A_0, A_1, A_2, A_3, EN and control lines $\overline{WR}$, $\overline{RS}$ shown in figure 9 minimize susceptibility to static encountered during handling and operational transients.

The logic interface circuit compares the TTL input signal against a TTL threshold reference voltage. The output of the comparator feeds the data input of a D type latch. The level sensitive D latch continuously places the D_X input signal on the Q_X output when the CLK ($\overline{WR}$) input is low, resulting in transparent operation. As soon as CLK ($\overline{WR}$) returns high the latch holds the data last present on the D_X input at the Q_X output, subject to the "Minimum Input Timing Requirements" table.

Following the latches the Q_X signals are level shifted and decoded to provide proper drive levels for the CMOS switches. This level shifting insures full ON/OFF switch operation for any analog signal present between the V+ and V– supply pins.

The enable (EN) pin is used to enable the address latches during the $\overline{WR}$ pulse. It can be hard wired to the logic supply if one of the channels will always be used (except during a reset) or it can be tied to address decoding circuitry for memory mapped operation. The $\overline{RS}$ pin is used as a master reset. All latches are cleared regardless of the state of any other latch or control line. The $\overline{WR}$ pin is used to transfer the state of the address control lines to their latches, except during a reset or when EN is low (see Truth Tables).

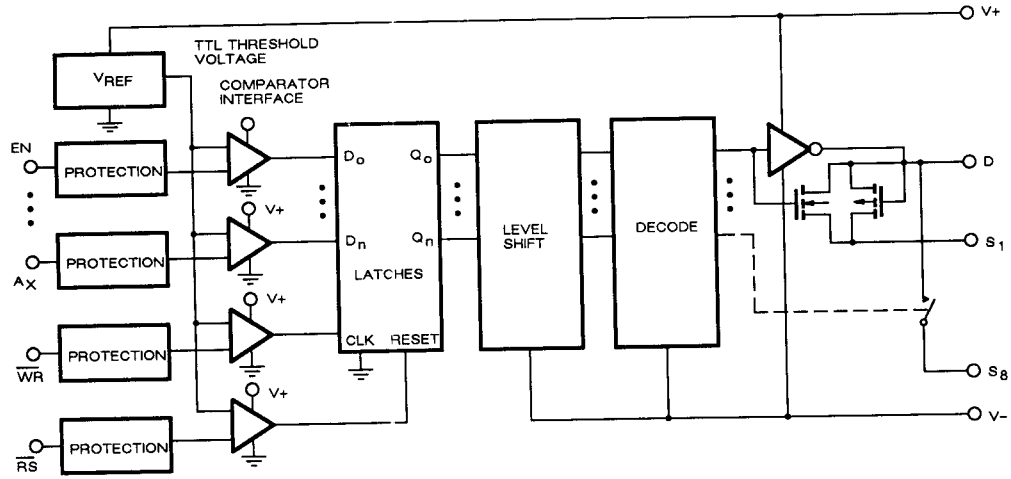

Figure 9. DG526/527 Simplifed Internal Structure

APPLICATIONS

INTRODUCTION

The DG526 and DG527 minimize the amount of interface hardware between a microprocessor system bus and the analog system being controlled or measured. The internal TTL compatible latches give these multiplexers write-only memory, that is, they can be programmed to stay in a particular switch state (e.g., switch 1 ON) until the microprocessor determines it is necessary to turn different switches ON or turn all switches OFF.

The input latches become transparent when $\overline{WR}$ is held low; therefore, these multiplexers operate by direct command of the coded switch state on the address inputs. In this mode the DG526 is identical

to the very popular DG506 even sharing the same pin locations. The same is true of the DG527 versus the popular DG507.

CIRCUIT OPERATION (See Figure 10)

Initially during system power-up $\overline{RS}$ would be active LOW maintaining all 16 switches in the OFF state. After $\overline{RS}$ returned HIGH the DG526 maintains all switches in the OFF state. As soon as the system program was ready to perform a write operation to the address assigned to the DG526, the address decoder would provide a $\overline{CS}$ active LOW signal which is gated with the WRITE ($\overline{WR}$) control signal. At this time the data on the DATA BUS (that will determine which switch to close) is stabilizing. When the $\overline{WR}$ signal returns to the HIGH state, (positive edge) the input latches of the DG526 save the data from the DATA BUS. The coded information in the A_0, A_1, A_2, A_3, and EN latches is decoded and the appropriate switch is turned ON.

The EN latch allows all switches to be turned OFF under program control. This becomes useful when two or more DG526s are cascaded to build 32-line and larger analog signal input multiplexers.

Figure 11 illustrates one use of the DG527. Dual multiplexers are generally used with differential or instrumentation amplifiers in process control applications to eliminate errors due to common mode signals. In this circuit however, advantage is taken of the dual multiplexing capability of the switch. This is achieved by using the multiplexer to select pairs of R.C. networks to control the pulse width of the multivibrator. This can be a particularly useful feature in process control applications where there is a requirement for a variable width sample "window" for different control signals.

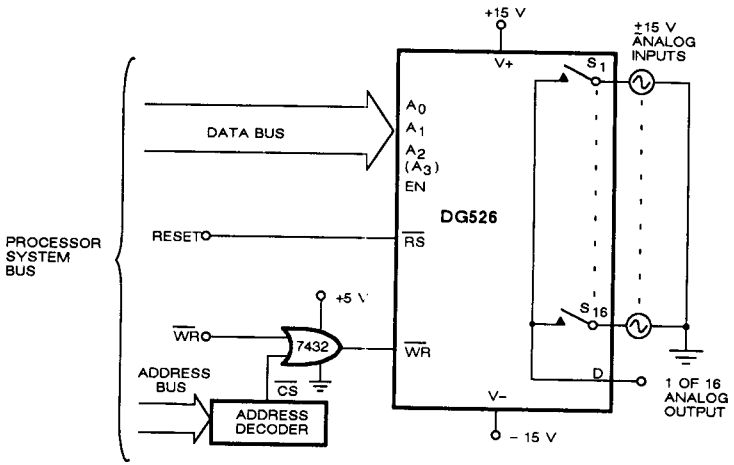

Figure 10

APPLICATIONS (Cont'd)

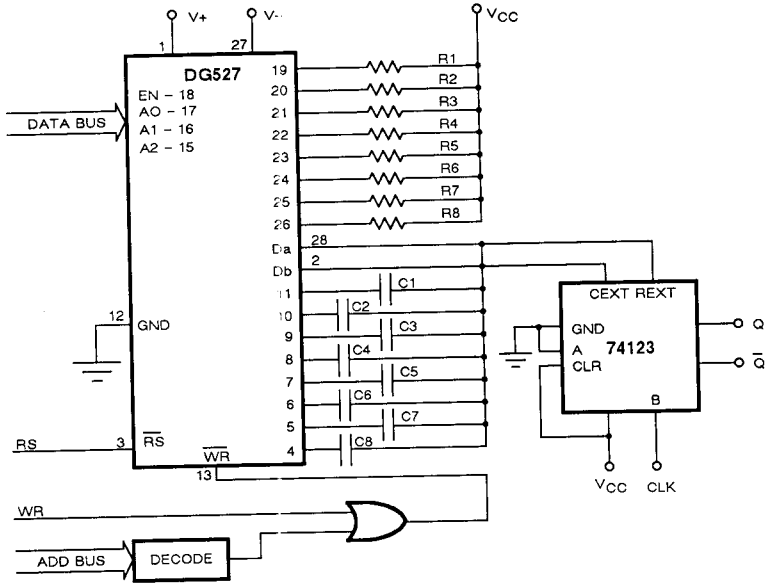

Figure 11. µP-selected Pulse-Width Control

APPLICATIONS HINTS

V+ Positive Supply Voltage (V)	V– Negative Supply Voltage (V)	GND Analog & Power Supply GND (V)	V_{IN} Logic Input Voltage V_{INH} Min/ V_{INL} Max (V)	V_S or V_D Analog Voltage Range (V)
20	–20	GND	2.4/0.8	± 20
15	–15	GND	2.4/0.8	±15
8	–8	GND	2.4/0.8	± 8