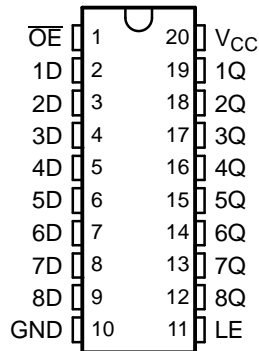


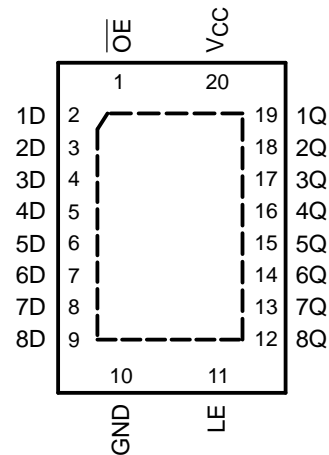
FEATURES

- Inputs Are TTL-Voltage Compatible
- 4.5-V to 5.5-V V_{CC} Operation
- Typical $t_{pd} = 5.1$ ns at 5 V
- Typical V_{OLP} (Output Ground Bounce)
<0.8 V at $V_{CC} = 5$ V, $T_A = 25^\circ\text{C}$
- Typical V_{OHV} (Output V_{OH} Undershoot)
>2.3 V at $V_{CC} = 5$ V, $T_A = 25^\circ\text{C}$
- Supports Mixed-Mode Voltage Operation on All Ports
- I_{off} Supports Partial-Power-Down Mode Operation
- Latch-Up Performance Exceeds 250 mA Per JESD 17
- ESD Protection Exceeds JESD 22
 - 2000-V Human-Body Model (A114-A)
 - 200-V Machine Model (A115-A)
 - 1000-V Charged-Device Model (C101)

DB, DGV, DW, NS, OR PW PACKAGE
(TOP VIEW)



RGY PACKAGE
(TOP VIEW)



DESCRIPTION/ORDERING INFORMATION

The SN74LV573AT is an octal transparent D-type latch. When the latch-enable (LE) input is high, the Q outputs follow the data (D) inputs. When LE is low, the Q outputs are latched at the logic levels of the D inputs.

ORDERING INFORMATION

T_A	PACKAGE ⁽¹⁾		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 85°C	QFN – RGY	Tape and reel	SN74LV573ATRGYR	VV573
	SOIC – DW	Tube	SN74LV573ATDW	LV573AT
		Tape and reel	SN74LV573ATDWR	
	SOP – NS	Tape and reel	SN74LV573ATNSR	74LV573AT
	SSOP – DB	Tape and reel	SN74LV573ATDBR	LV573AT
	TSSOP – PW	Tube	SN74LV573ATPW	LV573AT
		Tape and reel	SN74LV573ATPWR	
	TVSOP – DGV	Tape and reel	SN74LV573ATDGV	LV573AT

(1) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

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To ensure the high-impedance state during power up or power down, $\overline{\text{OE}}$ shall be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

This device is fully specified for partial-power-down applications using I_{off} . The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

INPUTS			OUTPUTS Q
OE	LE	D	
L	H	H	H
L	H	L	L
L	L	X	Q ₀
H	X	X	Z

To Seven Other Channels

Absolute Maximum Ratings⁽¹⁾

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_{CC}	Supply voltage range		–0.5	7	V
V_I	Input voltage range ⁽²⁾		–0.5	7	V
V_O	Voltage range applied to any output in the high-impedance or power-off state ⁽²⁾		–0.5	7	V
V_O	Output voltage range applied in the high or low state ⁽²⁾⁽³⁾		–0.5	$V_{CC} + 0.5$	V
I_{IK}	Input clamp current	$V_I < 0$		–20	mA
I_{OK}	Output clamp current	$V_O < 0$		–50	mA
I_O	Continuous output current	$V_O = 0$ to V_{CC}		±35	mA
	Continuous current through V_{CC} or GND			±70	mA
θ_{JA}	Package thermal impedance	DB package ⁽⁴⁾		70	°C/W
		DGV package ⁽⁴⁾		92	
		DW package ⁽⁴⁾		58	
		NS package ⁽⁴⁾		60	
		PW package ⁽⁴⁾		83	
		RGYpackage ⁽⁵⁾		37	
T_{stg}	Storage temperature range		–65	150	°C

- (1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.
- (3) This value is limited to 5.5 V maximum.
- (4) The package thermal impedance is calculated in accordance with JESD 51-7.
- (5) The package thermal impedance is calculated in accordance with JESD 51-5.

Recommended Operating Conditions⁽¹⁾

			MIN	MAX	UNIT
V_{CC}	Supply voltage		4.5	5.5	V
V_{IH}	High-level input voltage	$V_{CC} = 4.5$ V to 5.5 V	2		V
V_{IL}	Low-level input voltage	$V_{CC} = 4.5$ V to 5.5 V		0.8	V
V_I	Input voltage		0	5.5	V
V_O	Output voltage	High or low state	0	V_{CC}	V
		3-state	0	5.5	
I_{OH}	High-level output current	$V_{CC} = 4.5$ V to 5.5 V		–16	mA
I_{OL}	Low-level output current	$V_{CC} = 4.5$ V to 5.5 V		16	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	$V_{CC} = 4.5$ V to 5.5 V		20	ns/V
T_A	Operating free-air temperature		–40	85	°C

- (1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

SN74LV573AT

OCTAL TRANSPARENT D-TYPE LATCH

WITH 3-STATE OUTPUTS

SCES574C–JUNE 2004–REVISED AUGUST 2005

Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC}	T _A = 25°C			T _A = –40°C to 85°C		UNIT
			MIN	TYP	MAX	MIN	MAX	
V _{OH}	I _{OH} = –50 µA	4.5 V	4.4	4.5		4.4		V
	I _{OH} = –16 mA	4.5 V	3.8			3.8		
V _{OL}	I _{OL} = 50 µA	4.5 V		0	0.1		0.1	V
	I _{OL} = 16 mA	4.5 V			0.55		0.55	
I _I	V _I = 5.5 V or GND	0 to 5.5 V			±0.1		±1	µA
I _{OZ}	V _O = V _{CC} or GND	5.5 V			±0.25		±2.5	µA
I _{CC}	V _I = V _{CC} or GND, I _O = 0	5.5 V			2		20	µA
ΔI _{CC} (¹)	One input at 3.4 V, Other inputs at V _{CC} or GND	5.5 V			1.35		1.5	mA
I _{off}	V _I or V _O = 0 to 5.5 V	0			0.5		5	µA
C _i	V _I = V _{CC} or GND			4.5				pF

(1) This is the increase in supply current for each input at one of the specified TTL voltage levels, rather than 0 V or V_{CC}.

Timing Requirements

over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see [Figure 1](#))

		T _A = 25°C		T _A = –40°C to 85°C		UNIT
		MIN	MAX	MIN	MAX	
t _w	Pulse duration, LE high	6.5		8.5		ns
t _{su}	Setup time, data before LE↓	1.5		1.5		ns
t _h	Hold time, data after LE↓	3.5		3.5		ns

Switching Characteristics

over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see [Figure 1](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T _A = 25°C			T _A = –40°C to 85°C		UNIT
				MIN	TYP	MAX	MIN	MAX	
t _{PLH}	D	Q	C _L = 15 pF	2.6	5.1	8.5	1	9.5	ns
t _{PHL}				3	5.1	8.5	1	9.5	
t _{PLH}	LE	Q	C _L = 15 pF	3	7.7	12.3	1	14.5	ns
t _{PHL}				3.5	7.7	12.3	1	14.5	
t _{PZH}	\overline{OE}	Q	C _L = 15 pF	3	6.3	10.9	1	12.5	ns
t _{PZL}				3.3	6.3	10.9	1	12.5	
t _{PHZ}	\overline{OE}	Q	C _L = 15 pF	2.8	5.5	8	1	11	ns
t _{PLZ}				1.6	5.4	8	1	9.5	
t _{PLH}	D	Q	C _L = 50 pF	3.7	5.9	9.5	1	10.5	ns
t _{PHL}				5.5	5.9	9.5	1	10.5	
t _{PLH}	LE	Q	C _L = 50 pF	4.3	8.5	13.3	1	14.5	ns
t _{PHL}				5.9	8.5	13.3	1	14.5	
t _{PZH}	\overline{OE}	Q	C _L = 50 pF	4.5	7.1	11.9	1	13.5	ns
t _{PZL}				5.4	7.1	11.9	1	13.5	
t _{PHZ}	\overline{OE}	Q	C _L = 50 pF	3.3	8.8	11.2	1	12	ns
t _{PLZ}				2.6	8.8	11.2	1	12	
t _{sk(o)}			C _L = 50 pF			1.5		1.5	ns

Noise Characteristics⁽¹⁾

 $V_{CC} = 5\text{ V}$, $C_L = 50\text{ pF}$

		$T_A = 25^\circ\text{C}$			UNIT
		MIN	TYP	MAX	
$V_{OL(P)}$	Quiet output, maximum dynamic V_{OL}		1.1	1.5	V
$V_{OL(V)}$	Quiet output, minimum dynamic V_{OL}		–1.1	–1.5	V
$V_{OH(V)}$	Quiet output, maximum dynamic V_{OH}		4		V
$V_{IH(D)}$	High-level dynamic input voltage	2			V
$V_{IL(D)}$	Low-level dynamic input voltage			0.8	V

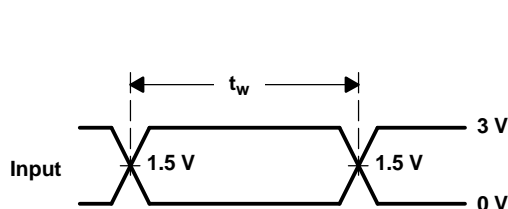
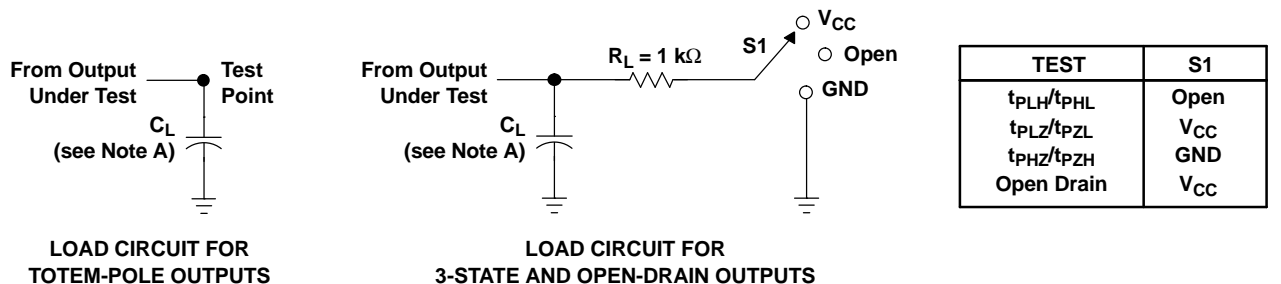
(1) Characteristics are for surface-mount packages only.

Operating Characteristics

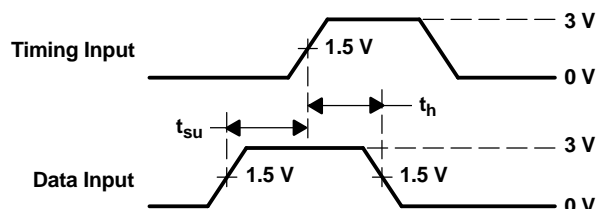
 $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$

PARAMETER		TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance	Outputs enabled		
		$C_L = 50\text{ pF}$, $f = 10\text{ MHz}$	8	pF

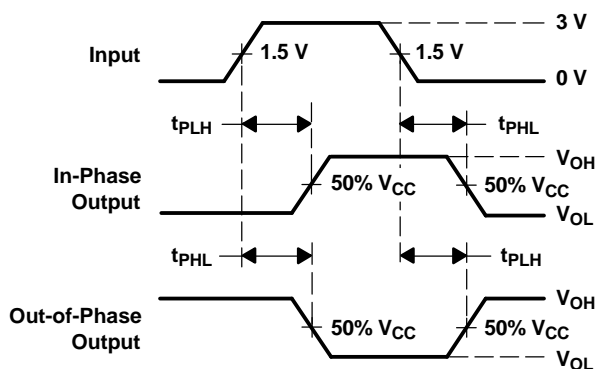
PARAMETER MEASUREMENT INFORMATION



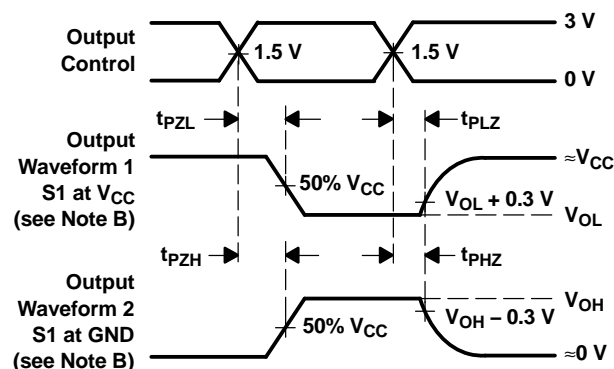
**VOLTAGE WAVEFORMS
PULSE DURATION**



**VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES**



**VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS**



**VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING**

- NOTES:
- C_L includes probe and jig capacitance.
 - Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
 - All input pulses are supplied by generators having the following characteristics: $PRR \leq 1\text{ MHz}$, $Z_O = 50\ \Omega$, $t_r \leq 3\text{ ns}$, $t_f \leq 3\text{ ns}$.
 - The outputs are measured one at a time, with one input transition per measurement.
 - t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 - t_{PZL} and t_{PZH} are the same as t_{en} .
 - t_{PHL} and t_{PLH} are the same as t_{pd} .
 - All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuits and Voltage Waveforms

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74LV573ATDWE4	ACTIVE	SOIC	DW	20		TBD	Call TI	Call TI	-40 to 85	LV573AT	Samples
SN74LV573ATDWG4	ACTIVE	SOIC	DW	20		TBD	Call TI	Call TI	-40 to 85	LV573AT	Samples
SN74LV573ATDWR	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LV573AT	Samples
SN74LV573ATDWRE4	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LV573AT	Samples
SN74LV573ATDWRG4	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LV573AT	Samples
SN74LV573ATPW	ACTIVE	TSSOP	PW	20	70	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LV573AT	Samples
SN74LV573ATPWE4	ACTIVE	TSSOP	PW	20	70	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LV573AT	Samples
SN74LV573ATPWG4	ACTIVE	TSSOP	PW	20	70	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LV573AT	Samples
SN74LV573ATPWR	ACTIVE	TSSOP	PW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LV573AT	Samples
SN74LV573ATPWRE4	ACTIVE	TSSOP	PW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LV573AT	Samples
SN74LV573ATPWRG4	ACTIVE	TSSOP	PW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LV573AT	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBsolete: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

⁽⁴⁾ There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

⁽⁵⁾ Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

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TAPE AND REEL INFORMATION
REEL DIMENSIONS

TAPE DIMENSIONS


A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

TAPE AND REEL INFORMATION

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LV573ATDWR	SOIC	DW	20	2000	330.0	24.4	10.8	13.0	2.7	12.0	24.0	Q1
SN74LV573ATPWR	TSSOP	PW	20	2000	330.0	16.4	6.95	7.1	1.6	8.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS

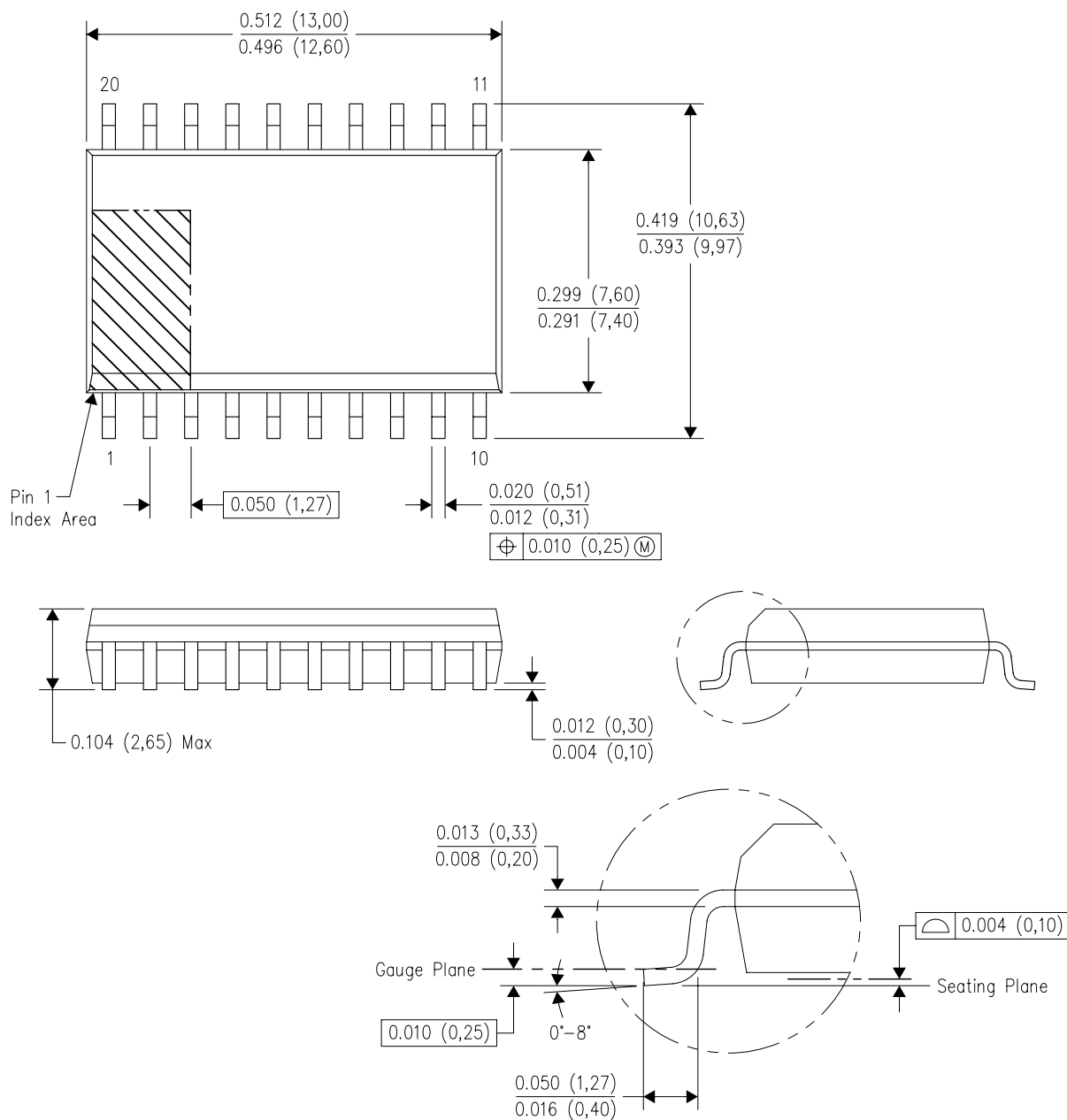


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LV573ATDWR	SOIC	DW	20	2000	367.0	367.0	45.0
SN74LV573ATPWR	TSSOP	PW	20	2000	367.0	367.0	38.0

DW (R-PDSO-G20)

PLASTIC SMALL OUTLINE



4040000-4/G 01/11

- NOTES: A. All linear dimensions are in inches (millimeters). Dimensioning and tolerancing per ASME Y14.5M-1994.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
D. Falls within JEDEC MS-013 variation AC.

DW (R-PDSO-G20)

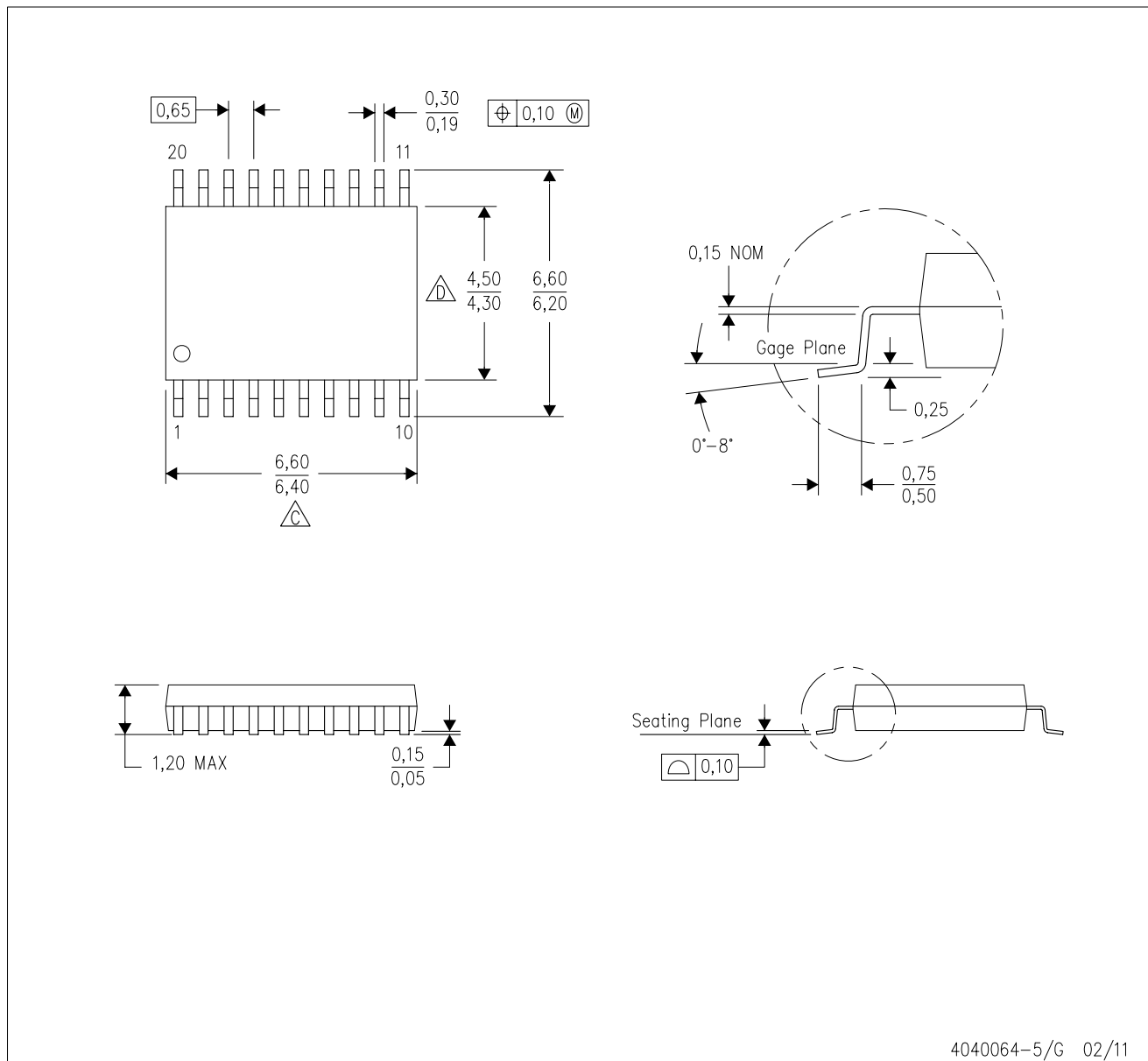
PLASTIC SMALL OUTLINE



- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Refer to IPC7351 for alternate board design.
 - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525
 - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

PW (R-PDSO-G20)

PLASTIC SMALL OUTLINE



4040064-5/G 02/11

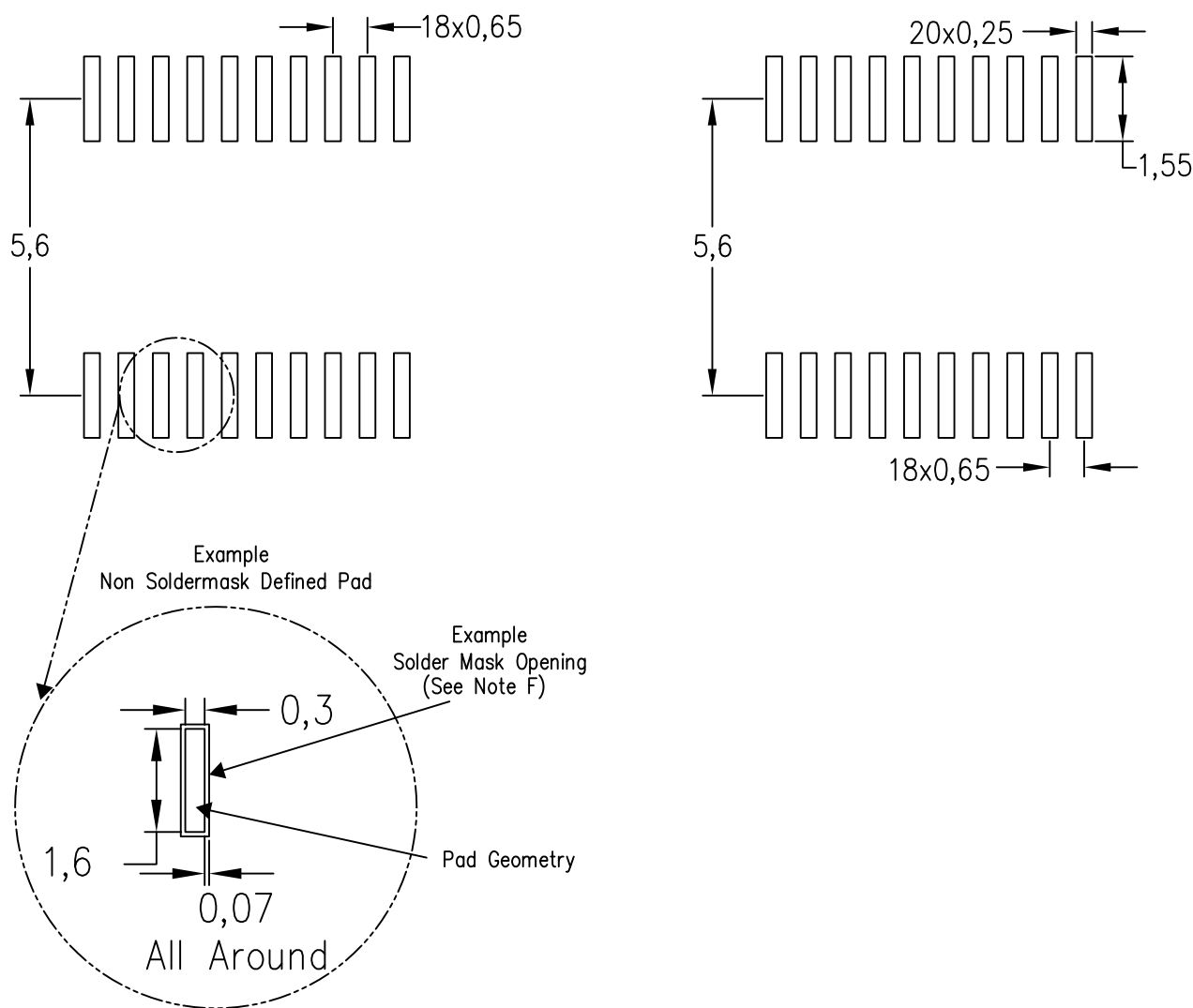
- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
 - D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
 - E. Falls within JEDEC MO-153

PW (R-PDSO-G20)

PLASTIC SMALL OUTLINE

Example Board Layout

Based on a stencil thickness
of .127mm (.005inch).



4211284-5/F 12/12

- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Publication IPC-7351 is recommended for alternate design.
 - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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