Click here for production status of specific part numbers.

MAX77734

Ultra-Low Power Tiny PMIC with Power Path Charger for Small Li+ and 150mA LDO

General Description

The MAX77734 is a tiny PMIC for applications where size and simplicity are critical. The IC integrates a linear-mode Li+ battery charger, low-dropout linear regulator (LDO), analog multiplexer, and dual-channel current sink driver.

The charger is designed for small-battery systems that require accurate termination as low as 0.375mA. The circuit can instantly regulate the system voltage when an input source is connected even if the battery is depleted.

The 150mA LDO's output is programmable between 0.8V and 3.975V with I²C. The analog MUX enables an external ADC to perform conversions on battery V&I signals for power monitoring. The current sinks are capable of sinking 12.8mA each and can be programmed for LEDs to blink in custom patterns.

The MAX77734 is available in a 20-bump, 0.4mm pitch wafer-level package (WLP). For a similar product with additional regulators, see the MAX77650.

Applications

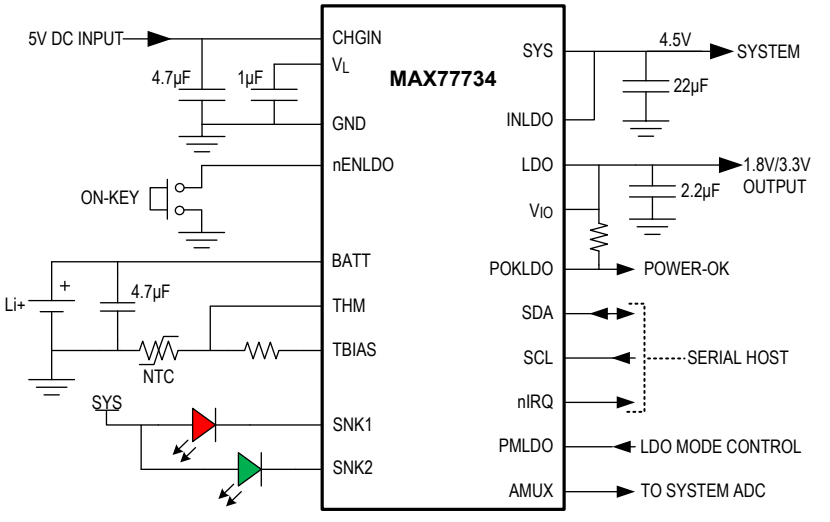
- Hearables: Headsets, Headphones, Earbuds
- Fitness Bands and other Bluetooth Wearables
- Action Cameras, Wearable/Body Cameras
- Low-Power Internet of Things (IoT) Gadgets

Benefits and Features

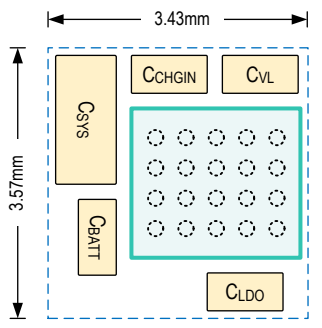
- Extends Battery Life
  - 200nA Factory-Ship Mode for Long Shelf Life
  - 500nA Shutdown Current
  - 4.5µA Quiescent Current with LDO Enabled
  - Charger Allows Battery to Relax after Charging
- Linear Charger Optimized for Small Battery Size
  - 7.5mA to 300mA Fast-Charge Current
  - Battery Regulation Voltage from 3.6V to 4.6V
  - Accurate Termination Current as low as 0.375mA
  - Instant-On Functionality provided by Maxim's Smart Power Selector™
  - JEITA Battery Temperature Monitors for Safe Charging
- Highly Integrated
  - 150mA LDO with Power-OK Output
  - Dual-Channel Current Sink for LEDs
  - Analog Multiplexer for Power Monitoring
  - Watchdog Timer
  - On-Key Input for LDO Enable and Manual Reset
- Small Size
  - 2.23mm x 1.97mm (0.5mm max height) WLP
  - 20-Bump, 0.4mm Pitch, 4 x 5 Array
  - 12.25mm² Total Solution Size

***Ordering Information* appears at end of data sheet.**

Simplified Application Circuit



POWER PATH LINEAR CHARGER WITH 0.375mA TERMINATION AND DUAL-CHANNEL CURRENT SINKS



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Absolute Maximum Ratings

nIRQ, POKLDO to GND .....-0.3V to V_{SYS} + 0.3V
SCL, SDA, PMLDO to GND .....-0.3V to V_{IO} + 0.3V
nENLDO to GND (Note 1)..... -0.3V to V_{CCINT} + 0.3V
CHGIN to GND.....-0.3V to +30.0V
SYS, BATT to GND .....-0.3V to +6.0V
V_L to GND .....-0.3V to +6.0V
AMUX, THM, TBIAS to GND.....-0.3V to +6.0V
nIRQ, POKLDO Continuous Current.....±3mA
SDA, AMUX Continuous Current .....±20mA
CHGIN, SYS, BATT Continuous Current .....1.2A_{RMS}
LDO to GND..... -0.3V to V_{INLDO} + 0.3V
INLDO, V_{IO} to GND .....-0.3V to V_{SYS} + 0.3V
SNK1, SNK2 to GND .....-0.3V to +6.0V
Operating Temperature Range..... -40°C to +85°C
Junction Temperature.....+150°C
Storage Temperature Range..... -65°C to +150°C
Soldering Temperature (reflow).....+260°C
Continuous Power Dissipation (70°C ambient).....
WLP (derate 18mW/°C above +70°C) 1440mW

Note 1: V_{CCINT} is internally connected to either BATT or V_L. Refer to *nENLDO Pullup Resistors to V_{CCINT} (V_{CC} Internal)* section.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Information

PACKAGE CHARACTERISTICS	VALUES
Package Code	N201B2+1
Outline Number	**21-100154**
Land Pattern Number	Refer to **Application Note 1891**
Thermal Resistance, Four-Layer Board:	
Junction to Ambient (θ_{JA})	55.49 °C/W

For the latest package outline information and land patterns (footprints), go to **www.maximintegrated.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to **www.maximintegrated.com/thermal-tutorial**.

Electrical Characteristics

(V_{CHGIN} = 0V, V_{SYS} = V_{BATT} = V_{INLDO} = 3.7V, V_{IO} = 1.8V, limits are 100% production tested at T_A = +25°C, limits over the operating temperature range (T_A = -40°C to +85°C) are guaranteed by design and characterization, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
SYS Voltage Range	V_{SYS}			2.7		5.5	V
BATT Factory-Ship Mode Current	$I_{BATT-FSM}$	Factory-ship mode (BATT to SYS switch open), T_A = +25°C, V_{BATT} = 3.7V, V_{SYS} = V_{INLDO} = 0V			0.2	1	µA
BATT Shutdown Current	$I_{BATT-SHDN}$	Shutdown state (all resources and bias off), BATT to SYS switch closed, T_A = +25°C, no load			0.5	1	µA
BATT Standby Current	$I_{BATT-STDBY}$	Standby state (all resources off), BATT to SYS switch closed, no load	Bias enabled in low-power mode (BIAS_REQ = 1, BIAS_LPM = 1)		1.5		µA
			Bias enabled in normal mode (BIAS_REQ = 1, BIAS_LPM = 0)		30		
BATT Quiescent Current	I_{BATT-Q}	Resource on state, BATT to SYS switch closed, current sinks and analog MUX disabled, V_{LDO} = 1.2V, no load	Bias is in low-power mode (BIAS_LPM = 1), LDO enabled in low-power mode		4.5	10	µA
			Bias is in low-power mode (BIAS_LPM = 1), LDO enabled in normal mode		22	40	
			Bias is in normal mode (BIAS_LPM = 0), LDO enabled in normal mode		40	60	
POWER-ON RESET (POR)							
POR Threshold	V_{POR}	V_{SYS} falling		1.5	1.9	2.1	V
POR Threshold Hysteresis					100		mV
UNDERVOLTAGE LOCKOUT (UVLO)							
UVLO Threshold	$V_{SYSUVLO}$	V_{SYS} falling		2.65	2.85	3.05	V
UVLO Threshold Hysteresis	$V_{SYSUVLO\_HYS}$				150		mV

Electrical Characteristics (continued)

(V_{CHGIN} = 0V, V_{SYS} = V_{BATT} = V_{INLDO} = 3.7V, V_{IO} = 1.8V, limits are 100% production tested at T_A = +25°C, limits over the operating temperature range (T_A = -40°C to +85°C) are guaranteed by design and characterization, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
OVERVOLTAGE LOCKOUT (OVLO)							
OVLO Threshold	$V_{SYSOVLO}$	V_{SYS} rising		5.55	5.85	6.15	V
THERMAL MONITORS							
Over-Temperature Lockout Threshold	T_{OTLO}	T_J rising			165		°C
Thermal Alarm Temperature 1	T_{JAL1}	T_J rising			80		°C
Thermal Alarm Temperature 2	T_{JAL2}	T_J rising			100		°C
Thermal Alarm Temperature Hysteresis					15		°C
ENABLE INPUT (nENLDO)							
nENLDO Leakage Current	$I_{nENLDO-LKG}$	V_{BATT} = 5.5V, V_{nENLDO} = 5.5V	T_A = +25°C	-1	±0.001	+1	µA
			T_A = +85°C		±0.01		
nENLDO Falling Threshold	$V_{TH\_nENLDO\_F}$	nENLDO Falling		V_{CCINT} - 1.4	V_{CCINT} - 1.0		V
nENLDO Rising Threshold	$V_{TH\_nENLDO\_R}$	nENLDO Rising			V_{CCINT} - 0.9	V_{CCINT} - 0.6	V
V_{CC} Internal	V_{CCINT}	(Note 2)	V_{CHGIN} = 0V, battery is present (V_{BATT} is valid)		V_{BATT}		V
			V_{CHGIN} = 5V, not USB suspended (USBS = 0)		V_L		
nENLDO Pullup	R_{nEN-PU}	Pullup to V_{CCINT}	PU_DIS = 0		200		kΩ
			PU_DIS = 1		10000		
Debounce Time	t_{DBNC_nENLDO}	Rising and falling, not in factory-ship mode	DB_nENLDO = 0 (Note 3)		200		µs
			DB_nENLDO = 1		30		ms
	$t_{FSM-EXDB}$	Falling only, factory-ship mode (Note 4)			250		
Manual Reset Time	t_{MRST}	T_MRST = 0		5	8	10	s
		T_MRST = 1		10	16	20	
Watchdog Timer Period	t_{WD}	WDT_PER[1:0] = 0b11		89	128	154	s

Electrical Characteristics (continued)

(V_{CHGIN} = 0V, V_{SYS} = V_{BATT} = V_{INLDO} = 3.7V, V_{IO} = 1.8V, limits are 100% production tested at T_A = +25°C, limits over the operating temperature range (T_A = -40°C to +85°C) are guaranteed by design and characterization, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
INTERRUPT OUTPUT (nIRQ)							
nIRQ Output Low Voltage	$V_{nIRQ-LO}$	Sinking 2mA				0.4	V
nIRQ Leakage Current	$I_{nIRQ-LKG}$	V_{SYS} = V_{IO} = 5.5V, nIRQ set to be high impedance (i.e., no interrupts), V_{nIRQ} = 0V and 3.6V	T_A = +25°C	-1	±0.001	+1	µA
			T_A = +85°C		±0.01		

Electrical Characteristics—Smart Power Selector Charger

(V_{CHGIN} = 5.0V, V_{SYS} = 4.5V, V_{BATT} = 4.2V, limits are 100% production tested at T_A = +25°C, limits over the operating temperature range (T_A = -40°C to +85°C) are guaranteed by design and characterization, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DC INPUT						
CHGIN Valid Voltage Range	V_{CHGIN}	Initial CHGIN voltage before enabling charging	4.10		7.25	V
CHGIN Standoff Voltage Range	$V_{STANDOFF}$	DC rising		28		V
CHGIN Overvoltage Threshold	V_{CHGIN_OVP}	DC rising	7.25	7.50	7.75	V
CHGIN Overvoltage Hysteresis				100		mV
CHGIN Undervoltage Lockout	V_{CHGIN_UVLO}	DC rising	3.9	4.0	4.1	V
CHGIN Undervoltage-Lockout Hysteresis				500		mV
Input Current-Limit Range	$I_{CHGIN-LIM}$	V_{SYS} = $V_{SYS-REG}$ - 100mV, programmable in 95mA steps	95		475	mA
Input Current-Limit Accuracy		$I_{CHGIN-LIM}$ = 95mA, V_{SYS} = $V_{SYS-REG}$ - 100mV	90	95	100	mA
Minimum Input Voltage Regulation Range	$V_{CHGIN-MIN}$	V_{CHGIN} falling due to loading conditions and/or high-impedance charge source, programmable in 100mV increments with VCHGIN_MIN[2:0]	4.0		4.7	V
Minimum Input Voltage Regulation Accuracy		$V_{CHGIN-MIN}$ = 4.5V (VCHGIN_MIN[2:0] = 0b101), I_{CHGIN} reduced by 10%	4.32	4.50	4.68	V
Charger Input Debounce Timer	$t_{CHGIN-DB}$	V_{CHGIN} = 5V, time before CHGIN is allowed to deliver current to SYS or BATT	100	120	140	ms

Electrical Characteristics—Smart Power Selector Charger (continued)

(V_{CHGIN} = 5.0V, V_{SYS} = 4.5V, V_{BATT} = 4.2V, limits are 100% production tested at T_A = +25°C, limits over the operating temperature range (T_A = -40°C to +85°C) are guaranteed by design and characterization, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
SUPPLY AND QUIESCENT CURRENTS							
CHGIN Supply Current	I_{CHGIN}	V_{CHGIN} = 5V, charger is not in USB suspend (USBS = 0), charging is finished (CHG_DTLS[3:0] indicate done), I_{SYS} = 0mA			1.0	1.8	mA
		V_{CHGIN} = 0V to 1V, V_{BATT} = 3.3V, I_{SYS} = 0mA				50	µA
CHGIN Suspend Supply Current	$I_{CHGIN-SUS}$	V_{CHGIN} = 5V, charger in USB suspend (USBS = 1)				50	µA
BATT Bias Current	$I_{BATT-BIAS}$	V_{CHGIN} = 5V, charger is not in USB suspend (USBS = 0), charging is finished (CHG_DTLS[3:0] indicate done), I_{SYS} = 0mA			5		µA
PREQUALIFICATION							
Charge Current Soft-Start Slew Time		Zero to full-scale			1		ms
Prequalification Voltage Threshold Range	V_{PQ}	Programmable in 100mV steps with CHG_PQ[2:0]		2.3		3.0	V
Prequalification Voltage Threshold Accuracy		V_{PQ} = 3.0V		-3		+3	%
Prequalification Mode Charge Current	I_{PQ}	V_{BATT} = 2.5V, V_{PQ} = 3.0V, expressed as a percentage of $I_{FAST-CHG}$	I_PQ = 0		10		%
			I_PQ = 1		20		
Prequalification Safety Timer	t_{PQ}	V_{BATT} < V_{PQ} = 3.0V		27	30	33	minutes
FAST-CHARGE							
Fast-Charge Voltage Range	$V_{FAST-CHG}$	I_{BATT} = 0mA, programmable in 25mV steps with CHG_CV[5:0]		3.6		4.6	V
Fast-Charge Voltage Accuracy		I_{BATT} = 0mA	$V_{FAST-CHG}$ = 4.3V, V_{SYS} = 4.5V, T_A = +25°C	-0.5	±0.15	+0.5	%
			$V_{FAST-CHG}$ = 3.6V to 4.6V, V_{SYS} = 4.8V			1.0	
Fast-Charge Current Range	$I_{FAST-CHG}$	Programmable in 7.5mA steps with CHG_CC[5:0]		7.5		300	mA

Electrical Characteristics—Smart Power Selector Charger (continued)

(V_{CHGIN} = 5.0V, V_{SYS} = 4.5V, V_{BATT} = 4.2V, limits are 100% production tested at T_A = +25°C, limits over the operating temperature range (T_A = -40°C to +85°C) are guaranteed by design and characterization, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Fast-Charge Current Accuracy		T_A = +25°C, V_{BATT} = $V_{FAST-CHG}$ - 300mV	$I_{FAST-CHG}$ = 15mA	-1.5		+1.5	%
			$I_{FAST-CHG}$ = 300mA	-1.5		+1.5	
Fast-Charge Current Accuracy over Temperature		Across all current settings, V_{BATT} = $V_{FAST-CHG}$ - 300mV, T_A = -40°C to +85°C		-10		+10	%
Fast-Charge Safety Timer Range	t_{FC}	Programmable in 2 hour increments or disabled with T_FAST_CHG[1:0], time measured from prequal done to timer fault		3		7	hours
Fast-Charge Safety Timer Accuracy		t_{FC} = 3 hours		-10		+10	%
Fast-Charge Safety Timer Suspend Threshold		Fast-charge CC mode, fast-charge safety timer paused when charge current drops below this threshold, expressed as a percentage of $I_{FAST-CHG}$			20		%
Junction Temperature Regulation Setting Range	T_{J-REG}	Programmable in 10°C steps with TJ_REG[2:0]		60		100	°C
Junction Temperature Regulation Loop Gain	G_{TJ-REG}	Rate at which $I_{FAST-CHG}/I_{PQ}$ is reduced to maintain T_{J-REG}, expressed a percentage of $I_{FAST-CHG}/I_{PQ}$ per degree centigrade rise			-5.4		%/°C
TERMINATION AND TOPOFF							
End-of-Charge Termination Current	I_{TERM}	I_TERM = 0b00 (expressed as a percentage of $I_{FAST-CHG}$)			5		%
		I_TERM = 0b01 (expressed as a percentage of $I_{FAST-CHG}$)			7.5		
		I_TERM = 0b10 (expressed as a percentage of $I_{FAST-CHG}$)		8.5	10	11.5	
		I_TERM = 0b11 (expressed as a percentage of $I_{FAST-CHG}$)			15		
Top-Off Timer Range	t_{TO}	I_{BATT} < I_{TERM}, programmable in 5 minute steps with T_TOPOFF[2:0]		0		35	minutes
Top-Off Timer Accuracy		t_{TO} = 10 minutes		-10		+10	%

Electrical Characteristics—Smart Power Selector Charger (continued)

(V_{CHGIN} = 5.0V, V_{SYS} = 4.5V, V_{BATT} = 4.2V, limits are 100% production tested at T_A = +25°C, limits over the operating temperature range (T_A = -40°C to +85°C) are guaranteed by design and characterization, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Charge Restart Threshold	$V_{RESTART}$	Charging is finished (CHG_DTLS[3:0] indicate done), charging resumes when $V_{BATT} < V_{FAST-CHG} - V_{RESTART}$		65	150		mV
End-of-Charge Termination Current Accuracy		$I_{FAST-CHG}$ = 15mA, I_{TERM} = 1.5mA (10% of $I_{FAST-CHG}$), T_A = +25°C		1.35	1.5	1.65	mA
		$I_{FAST-CHG}$ = 300mA, I_{TERM} = 30mA (10% of $I_{FAST-CHG}$), T_A = +25°C		27	30	33	
End-of-Charge Termination Current Glitch Filter					60		µs
DEVICE ON-RESISTANCE AND LEAKAGE							
BATT to SYS On-Resistance		V_{BATT} = 3.7V, I_{BATT} = 300mA, V_{CHGIN} = 0V, battery is discharging to SYS			100	150	mΩ
Charger FET Leakage Current		V_{SYS} = 4.5V, V_{BATT} = 0V, charger disabled	T_A = +25°C		0.1	1.0	µA
			T_A = +85°C		1		
		V_{SYS} = 0V, V_{BATT} = 4.2V, factory-ship mode	T_A = +25°C		0.1	1.0	
			T_A = +85°C		1		
CHGIN to SYS On-Resistance		V_{CHGIN} = 4.65V, I_{CHGIN} = 400mA			600		mΩ
Input FET Leakage Current		V_{CHGIN} = 0V, V_{SYS} = 4.2V, body-switched diode reverse biased	T_A = +25°C		0.1	1.0	µA
			T_A = +85°C		1		
SYSTEM NODE							
System Voltage Regulation Range	$V_{SYS-REG}$	Programmable in 25mV steps with VSYS_REG[4:0]		4.1		4.8	V
System Voltage Regulation Accuracy	V_{SYS}	$V_{SYS-REG}$ = 4.5V, I_{SYS} = 1mA	T_A = +25°C	4.41	4.50	4.59	V
		VSYS-REG = 4.5V, ISYS = 1mA	T_A = -40°C to +85°C	4.365	4.5	4.635	
Minimum System Voltage Regulation Loop Setpoint	$V_{SYS-MIN}$	V_{CHGIN} = 5V, $V_{SYS-REG}$ = 4.5V, $V_{SYS} < V_{SYS-REG}$ due to $I_{CHGIN} = I_{CHGIN-LIM}$ (input in current limit), battery charging, I_{BATT} reduced to 50% of $I_{FAST-CHG}$ (minimum system voltage regulation active)		4.34	4.4	4.45	V
Supplement Mode System Voltage Regulation		I_{SYS} = 150mA			V_{BATT} - 0.15V		V

Electrical Characteristics—Adjustable Thermistor Temperature Monitors

(V_{CHGIN} = 5.0V, V_{SYS} = 4.5V, V_{BATT} = 4.2V, limits are 100% production tested at T_A = +25°C, limits over the operating temperature range (T_A = -40°C to +85°C) are guaranteed by design and characterization, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
JEITA TEMPERATURE MONITORS						
TBIAS Voltage	V_{TBIAS}	THM_EN = 1, V_{CHGIN} = 5V		1.25		V
JEITA Cold Threshold Range	V_{COLD}	Voltage rising threshold, programmable with THM_COLD[1:0] in 5ºC increments when using an NTC β = 3380K	0.867		1.024	V
JEITA Cool Threshold Range	V_{COOL}	Voltage rising threshold, programmable with THM_COOL[1:0] in 5ºC increments when using an NTC β = 3380K	0.747		0.923	V
JEITA Warm Threshold Range	V_{WARM}	Voltage falling threshold, programmable with THM_WARM[1:0] in 5ºC increments when using an NTC β = 3380K	0.367		0.511	V
JEITA Hot Threshold Range	V_{HOT}	Voltage falling threshold, programmable with THM_HOT[1:0] in 5ºC increments when using an NTC β = 3380K	0.291		0.411	V
Temperature Threshold Accuracy		Voltage threshold accuracy expressed as temperature for an NTC β = 3380K		±3		°C
Temperature Threshold Hysteresis		Temperature hysteresis set on each voltage threshold for an NTC β = 3380K		3		°C
JEITA Modified Fast-Charge Voltage Range	$V_{FAST-CHG\_JEITA}$	I_{BATT} = 0mA, programmable in 25mV steps, battery is either cool or warm	3.6		4.6	V
JEITA Modified Fast-Charge Current Range	$I_{FAST-CHG\_JEITA}$	Programmable in 7.5mA steps, battery is either cool or warm	7.5		300	mA

Electrical Characteristics—Analog Multiplexer

(V_{CHGIN} = 5.0V, V_{SYS} = 4.5V, V_{BATT} = 4.2V, limits are 100% production tested at T_A = +25°C, limits over the operating temperature range (T_A = -40°C to +85°C) are guaranteed by design and characterization, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
ANALOG MULTIPLEXER							
Full-Scale Voltage	V_{FS}				1.25		V
Channel Switching Time					0.3		µs
Off Leakage Current		V_{AMUX} = 0V, AMUX is high impedance	T_A = +25°C		1	500	nA
			T_A = +85°C		1		µA
CHGIN POWER MEASUREMENT							
CHGIN Current Monitor Gain	G_{ICHGIN}	V_{FS} corresponds to maximum $I_{CHGIN-LIM}$ setting			2.632		V/A
CHGIN Voltage Monitor Gain	G_{VCHGIN}	V_{FS} corresponds to V_{CHGIN_OVP}			0.167		V/V
BATT AND SYS POWER MEASUREMENT							
Battery Charge Current Monitor Gain	$G_{IBATT-CHG}$	V_{FS} corresponds to 100% of $I_{FAST-CHG}$ setting (CHG_CC[5:0])			12.5		mV/%
Charge Current Monitor Accuracy		$I_{FAST-CHG}$ = 15mA, T_A = +25°C, V_{BATT} = $V_{FAST-CHG}$ - 300mV		-3.5		+3.5	%
		$I_{FAST-CHG}$ = 300mA, T_A = +25°C, V_{BATT} = $V_{FAST-CHG}$ - 300mV		-3.5		+3.5	
Charge Current Monitor Accuracy over Temperature		Across all current settings, V_{BATT} = $V_{FAST-CHG}$ - 300mV		-10		+10	%
Battery Discharge Monitor Full-Scale Current Range	$I_{DISCHG-SCALE}$	Programmable with IMON_DISCHG_SCALE[3:0]		8.2		300	mA
Battery Discharge Current Monitor Accuracy		15mA to 300mA battery discharge current, $I_{DISCHG-SCALE}$ = 300mA		-15		+15	%
Battery Discharge Current Monitor Offset		I_{BATT} = 0mA		-0.5		+0.8	mA
Battery-Voltage Monitor Gain	G_{VBATT}	V_{FS} corresponds to maximum $V_{FAST-CHG}$ setting			0.272		V/V
SYS Voltage Monitor Gain	G_{VSYS}	V_{FS} corresponds to maximum $V_{SYS-REG}$ setting			0.26		V/V
THM AND TBIAS VOLTAGE MEASUREMENT							
THM Voltage Monitor Gain	G_{VTHM}				1		V/V
TBIAS Voltage Monitor Gain	G_{VTBIAS}				1		V/V

Electrical Characteristics—Linear Regulator

(V_{SYS} = V_{INLDO} = 3.7V, C_{SYS} = 22µF, C_{LDO} = 2.2µF, limits are 100% production tested at T_A = +25°C, limits over the operating temperature range (T_A = -40°C to +85°C) are guaranteed by design and characterization, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
LDO							
INLDO Voltage Range	V_{INLDO}	INLDO cannot exceed V_{SYS} by 0.3V		1.7		5.5	V
INLDO Supply Current	$I_{INLDO-Q}$	V_{LDO} = 1.2V, no load	Low-power mode		1.5		µA
		V_{LDO} = 1.2V, no load	Normal mode		12		
LDO Output Voltage Range	$V_{LDO-REG}$	Target regulation voltage. Programmable in 25mV steps with LDO_VREG[6:0].		0.8		3.975	V
LDO Output Voltage Accuracy	V_{LDO}	V_{INLDO} = V_{LDO} + 0.3V to 5.5V, across all $V_{LDO-REG}$ settings, bias in normal mode	I_{LDO} = 0.1mA to 150mA, T_A = -5°C to +85°C, normal mode	-2		+2	%
			I_{LDO} = 0.1mA to 150mA, T_A = -40°C, normal mode	-3		+3	
			I_{LDO} = 0.1mA to 5mA, low-power mode	-6.5		+6.5	
LDO Maximum Output Current	I_{LDO}	Normal mode (Note 7)		150			mA
		Low-power mode (Note 7)		5			
Load Regulation		V_{INLDO} = V_{LDO} + 0.3V to 5.5V, across all $V_{LDO-REG}$ settings	I_{LDO} = 0.1mA to 150mA, normal mode		0.5		%
			I_{LDO} = 0.1mA to 5mA, low-power mode		0.5		
Line Regulation		I_{LDO} = 0.1mA, V_{INLDO} = V_{LDO} + 0.3V to 5.5V, across all $V_{LDO-REG}$ settings	Normal mode		0.05		%/V
			Low-power mode		0.05		
Dropout Voltage	V_{DO}	I_{LDO} = 150mA, normal mode (Note 6)	V_{INLDO} = 3.0V, $V_{LDO-REG}$ = 3.3V		60	150	mV
		I_{LDO} = 150mA, Normal Mode (Note 6)	V_{INLDO} = 1.7V, $V_{LDO-REG}$ = 1.85V		100		
LDO Current Limit	$I_{LDO-LIM}$	V_{LDO} = 90% of programmed target	Normal mode	160	300	560	mA
			Low-power mode		40		
LDO Output Capacitance for Stability	C_{LDO}	(Note 5)		1.1	2.2		µF
LDO Startup Ramp Rate	$\Delta V_{LDO}/\Delta t$	10% to 90% of final value			20		mV/µs

Electrical Characteristics—Linear Regulator (continued)

(V_{SYS} = V_{INLDO} = 3.7V, C_{SYS} = 22µF, C_{LDO} = 2.2µF, limits are 100% production tested at T_A = +25°C, limits over the operating temperature range (T_A = -40°C to +85°C) are guaranteed by design and characterization, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Output Noise		LDO and bias in normal mode, f = 10Hz to 100kHz, I_{LDO} = 15mA	V_{SYS} = V_{INLDO} = 2.7V, V_{LDO} = 0.8V		100		μV_{RMS}
			V_{SYS} = V_{INLDO} = 2.7V, V_{LDO} = 1.0V		150		
			V_{SYS} = V_{INLDO} = 2.7V, V_{LDO} = 2.0V		200		
			V_{SYS} = V_{INLDO} = 3.7V, V_{LDO} = 3.0V		300		
			V_{SYS} = V_{INLDO} = 5.5V, V_{LDO} = 3.975V		400		
Power-Supply Rejection Ratio	PSRR	LDO in normal-power mode, bias in low-power mode, V_{SYS} =3.6V, V_{INLDO} =2.8V+20mVpp, f = 10Hz to 1kHz, V_{LDO} =1.8V, I_{LDO} =15mA			60		dB
Active Discharge Resistance	R_{AD_LDO}				100		Ω
LDO POWER-OK OUTPUT (POKLDO)							
POKLDO Threshold	V_{POKLDO_R}	V_{LDO} rising, expressed as a percentage of $V_{LDO-REG}$		82.5	87.5	92.5	%
	V_{POKLDO_F}	V_{LDO} falling, expressed as a percentage of $V_{LDO-REG}$		79	84	89	
POKLDO Low Voltage	V_{POKLDO}	POKLDO = low, sinking 2mA				0.4	V
POKLDO Leakage Current	$I_{POKLDO-LKG}$	V_{SYS} = V_{IO} = 5.5V, POKLDO is high-Z, V_{POKLDO} = 0V or 5.5V	T_A = +25°C	-1	±0.001	+1	µA
			T_A = +85°C		±0.01		
LDO POWER-MODE INPUT (PMLDO)							
PMLDO Logic-High Threshold	V_{PMLDO_HI}			0.7 x V_{IO}			V
PMLDO Logic-Low Threshold	V_{PMLDO_LO}					0.3 x V_{IO}	V
PMLDO Debounce Timer	$t_{PMLDO-DB}$	(Note 3)			200		µs
PMLDO Leakage Current	$I_{PMLDO-LKG}$	V_{SYS} = V_{IO} = 5.5V, V_{PMLDO} = 0V or 5.5V	T_A = +25°C	-1	±0.001	+1	µA
			T_A = +85°C		±0.01		

Electrical Characteristics—Dual-Channel Current Sink Driver

(V_{SYS} = 3.7V, V_{SNKx} = 0.2V, limits are 100% production tested at T_A = +25°C, limits over the operating temperature range (T_A = -40°C to +85°C) are guaranteed by design and characterization, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
DUAL-CHANNEL CURRENT SINK DRIVER							
Current Sink Quiescent Current	ΔI_{BATT-Q}	Change in supply current when one channel is enabled and delivering 12.8mA, V_{SNKx} = 0.2V			6		µA
Current Sink Leakage		All current sink drivers combined, outputs disabled, V_{SNKx} = 5.5V,	T_A = +25ºC		+0.1	+1.0	µA
			T_A = +85ºC		+1.0		
Sink Current Range	I_{SNKx}	Programmable with BRT_SNKx[4:0]	SNK_FSx[1:0] = 0b01	0.1		3.2	mA
			SNK_FSx[1:0] = 0b10	0.2		6.4	
			SNK_FSx[1:0] = 0b11	0.4		12.8	
3.2mA CURRENT SINK RANGE (SNK_FSx[1:0]=0b01)							
Current Sink DAC Bits					5		bits
Current Sink Accuracy		BRT_SNKx[4:0] = 0b11111	SNK_FSx[1:0] = 0b01, T_A = +25ºC	3.10	3.20	3.25	mA
			SNK_FSx[1:0] = 0b01, T_A = -40ºC to +85ºC	2.975	3.20	3.425	
Dropout Voltage	V_{DO}	BRT_SNKx[4:0] = 0b11111	SNK_FSx[1:0] = 0b01, I_{SNKx} = 2.9mA		35	70	mV
6.4mA CURRENT SINK RANGE (SNK_FSx[1:0] =0b10)							
Current Sink Accuracy		BRT_SNKx[4:0] = 0b11111	SNK_FSx[1:0] = 0b10, T_A = +25ºC	6.30	6.40	6.50	mA
			SNK_FSx[1:0] = 0b10, T_A = -40ºC to +85ºC	5.95	6.40	6.85	
Dropout Voltage	V_{DO}	BRT_SNKx[4:0] = 0b11111	SNK_FSx[1:0] = 0b10, I_{SNKx} = 5.75mA		35	70	mV
12.8mA CURRENT SINK RANGE (SNK_FSx[1:0]=0b11)							
Current Sink Accuracy		BRT_SNKx[4:0] = 0b11111	SNK_FSx[1:0] = 0b11, T_A = +25ºC	12.6	12.8	13.0	mA
			SNK_FSx[1:0] = 0b11, T_A = -40ºC to +85ºC	11.9	12.8	13.7	
Dropout Voltage	V_{DO}	BRT_SNKx[4:0] = 0b11111	SNK_FSx[1:0] = 0b11, I_{SNKx} = 11.5mA		35	70	mV
TIMING CHARACTERISTICS							
Root Clock Frequency				25.6	32.0	38.4	Hz

Electrical Characteristics—Dual-Channel Current Sink Driver (continued)

(V_{SYS} = 3.7V, V_{SNKx} = 0.2V, limits are 100% production tested at T_A = +25°C, limits over the operating temperature range (T_A = -40°C to +85°C) are guaranteed by design and characterization, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
TIMING CHARACTERISTICS / BLINK PERIOD SETTINGS						
Minimum Blink Period		P_SNKx[3:0] = 0b0000		0.5		s
				16		clocks
Maximum Blink Period		P_SNKx[3:0] = 0b1111		8		s
				256		clocks
Blink Period LSB				0.5		s
				16		clocks
TIMING CHARACTERISTICS / BLINK DUTY CYCLE						
Minimum Blink Duty Cycle		D_SNKx[3:0] = 0b0000		6.25		%
Maximum Blink Duty Cycle		D_SNKx[3:0] = 0b1111		100		%
Blink Duty Cycle LSB				6.25		%

Electrical Characteristics—I²C Serial Interface

(V_{SYS} = 3.7V, V_{IO}= 1.8V, limits are 100% production tested at T_A = +25°C, limits over the operating temperature range (T_A= -40°C to +85°C) are guaranteed by design and characterization, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SERIAL INTERFACE/I/O STAGE						
V_{IO} Voltage Range	V_{IO}		1.7		3.6	V
V_{IO} Bias Current		T_A = +25°C	-1	0	+1	µA
SCL, SDA Input High Voltage	V_{IH}		0.7 x V_{IO}			V
SCL, SDA Input Low Voltage	V_{IL}				0.3 x V_{IO}	V
SCL, SDA Input Hysteresis	V_{HYS}			0.05 x V_{IO}		V
SCL, SDA Input Leakage Current	I_I	V_{IO} = 3.6V, V_{SCL} = V_{SDA} = 0V or 3.6V	-10		10	µA
SDA Output Low Voltage	V_{OL}	Sinking 20mA			0.4	V
SCL, SDA Pin Capacitance		(Note 8)		10		pF
Input Filter Suppressed Spike Maximum Pulse Width	t_{SP}	(Note 8)		50		ns

Electrical Characteristics—I²C Serial Interface (continued)

(V_{SYS} = 3.7V, V_{IO}= 1.8V, limits are 100% production tested at T_A = +25°C, limits over the operating temperature range (T_A= -40°C to +85°C) are guaranteed by design and characterization, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SERIAL INTERFACE/TIMING						
Clock Frequency	f_{SCL}				1	MHz
Bus Free Time between STOP and START Condition	t_{BUF}		0.5			µs
Setup Time REPEATED START Condition	$t_{SU;STA}$		260			ns
Hold Time REPEATED START Condition	$t_{HD;STA}$		260			ns
SCL Low Period	t_{LOW}		500			ns
SCL High Period	t_{HIGH}		260			ns
Data Setup Time	$t_{SU;DAT}$		50			ns
Data Hold Time	$t_{HD;DAT}$		0			µs
Setup Time for STOP Condition	$t_{SU;STO}$		260			ns

Note 2: See the *nENLDO Pullup Resistors to V_{CCINT} (V_{CC} Internal)* section of the data sheet.

Note 3: Digitally debounced for two consecutive 100µs clock periods. Typical debounce time is at least 200µs and up to 300µs due to synchronization to the digital clock.

Note 4: This is the amount of additional debounce time required to exit factory-ship mode (250ms, typ additional time).

Note 5: For stability, guaranteed by design and not production tested.

Note 6: The dropout voltage is the difference between the input voltage and the output voltage when the input voltage is within the valid input voltage range, but below the output voltage setpoint. For example, if the output voltage setpoint is 1.85V, the input voltage is 1.7V, and the actual output voltage is 1.65V, then the dropout voltage is 50mV (V_{DO} = V_{INLDO} - V_{LDO}).

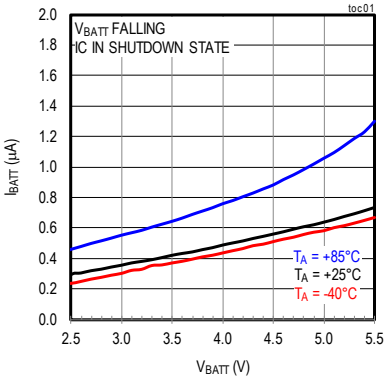
Note 7: The "Maximum Output Current" is guaranteed by the "Output Voltage Accuracy" tests.

Note 8: Design guidance only. Not production tested.

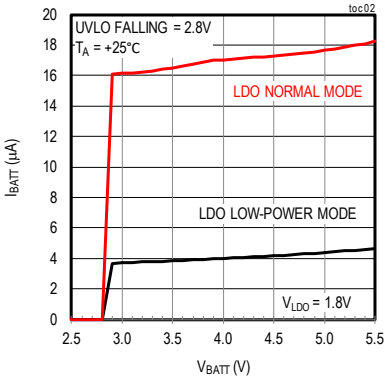
Typical Operating Characteristics

(*Typical Application Circuits*, V_{CHGIN} = 0V, V_{SYS} = V_{BATT} = V_{INLDO} = 3.7V, V_{IO} = 1.8V, $V_{SYS-REG}$ = 4.5V, BIAS in low-power mode, LDO in normal mode, T_A = +25°C, unless otherwise noted.) (T_A = +25°C, unless otherwise noted.)

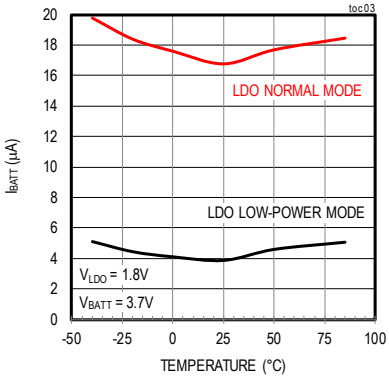
SHUTDOWN SUPPLY CURRENT vs. BATTERY VOLTAGE



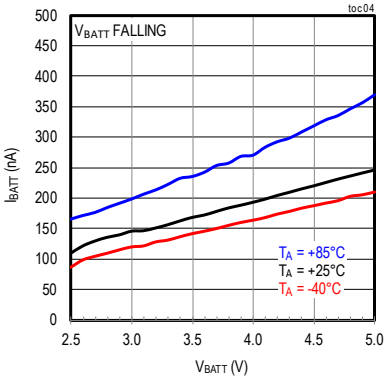
QUIESCENT SUPPLY CURRENT vs. BATTERY VOLTAGE



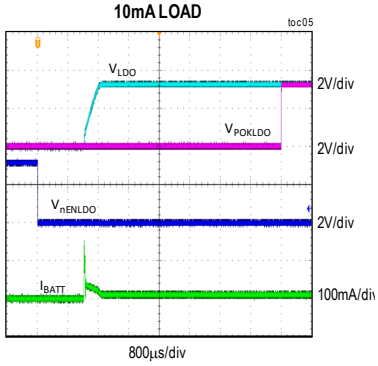
QUIESCENT SUPPLY CURRENT vs. TEMPERATURE



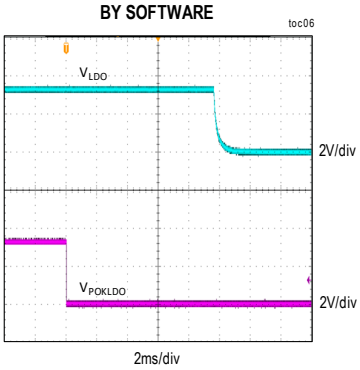
FACTORY-SHIP MODE CURRENT



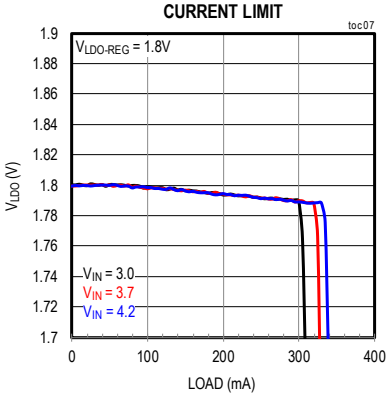
LDO POWER-UP CAUSED BY BUTTON PRESS (LDO_WAKE) 10mA LOAD



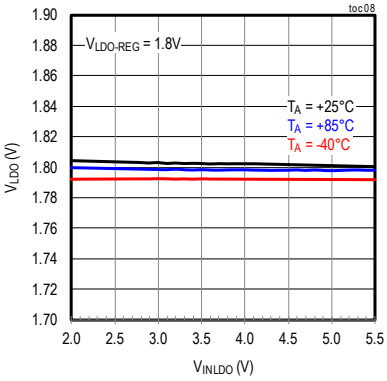
LDO POWER-DOWN CAUSED BY SOFTWARE



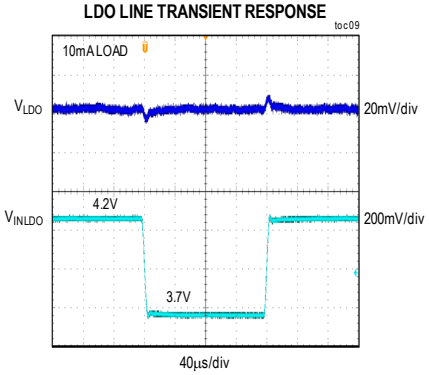
LDO LOAD REGULATION AND CURRENT LIMIT



LDO LINE REGULATION



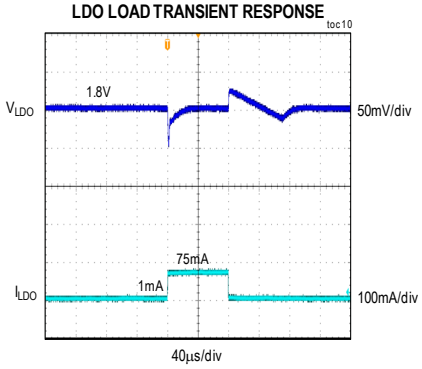
LDO LINE TRANSIENT RESPONSE



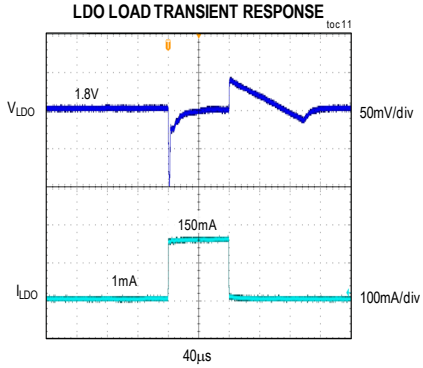
Typical Operating Characteristics (continued)

(*Typical Application Circuits*, V_{CHGIN} = 0V, V_{SYS} = V_{BATT} = V_{INLDO} = 3.7V, V_{IO} = 1.8V, $V_{SYS-REG}$ = 4.5V, BIAS in low-power mode, LDO in normal mode, T_A = +25°C, unless otherwise noted.) (T_A = +25°C, unless otherwise noted.)

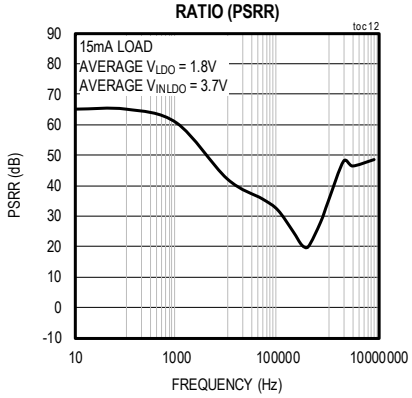
LDO LOAD TRANSIENT RESPONSE



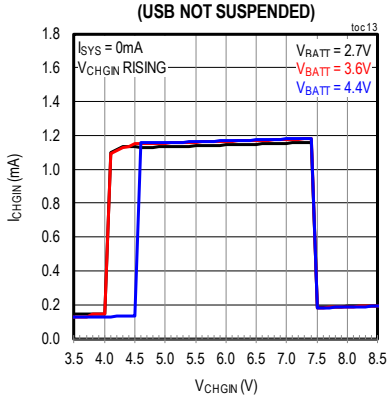
LDO LOAD TRANSIENT RESPONSE



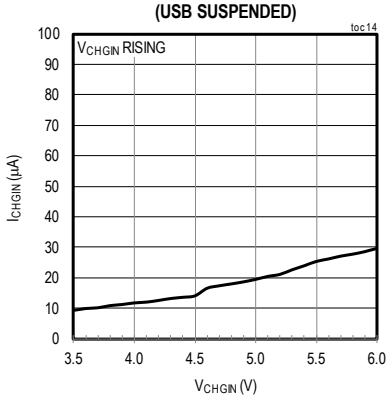
LDO POWER SUPPLY REJECTION RATIO (PSRR)



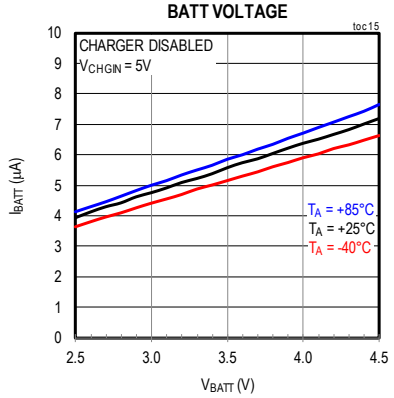
CHGIN SUPPLY CURRENT vs. CHGIN VOLTAGE (USB NOT SUSPENDED)



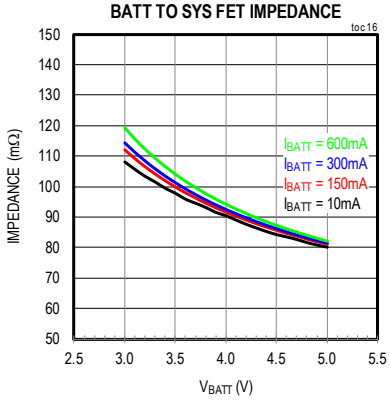
CHGIN SUPPLY CURRENT vs. CHGIN VOLTAGE (USB SUSPENDED)



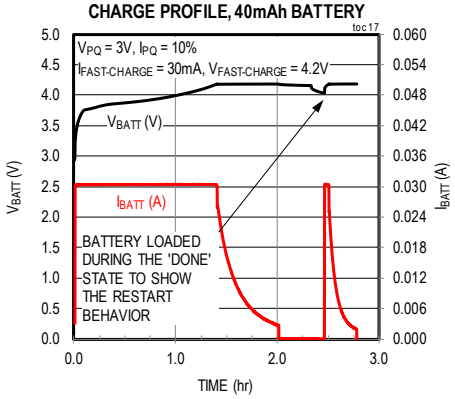
BATT BIAS CURRENT vs. BATT VOLTAGE



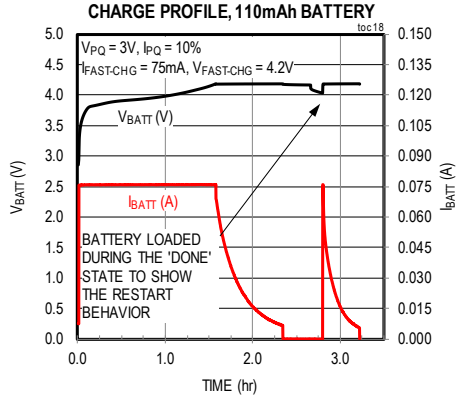
BATT TO SYS FET IMPEDANCE



CHARGE PROFILE, 40mAh BATTERY



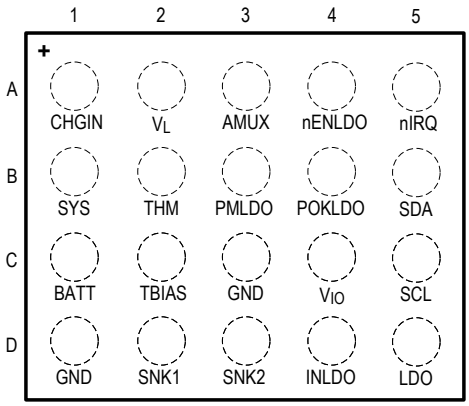
CHARGE PROFILE, 110mAh BATTERY



Bump Configuration

TOP VIEW
(BUMP SIDE DOWN)

MAX77734



WLP
(2.23mm x 1.97mm x 0.5mm, 0.4mm PITCH)

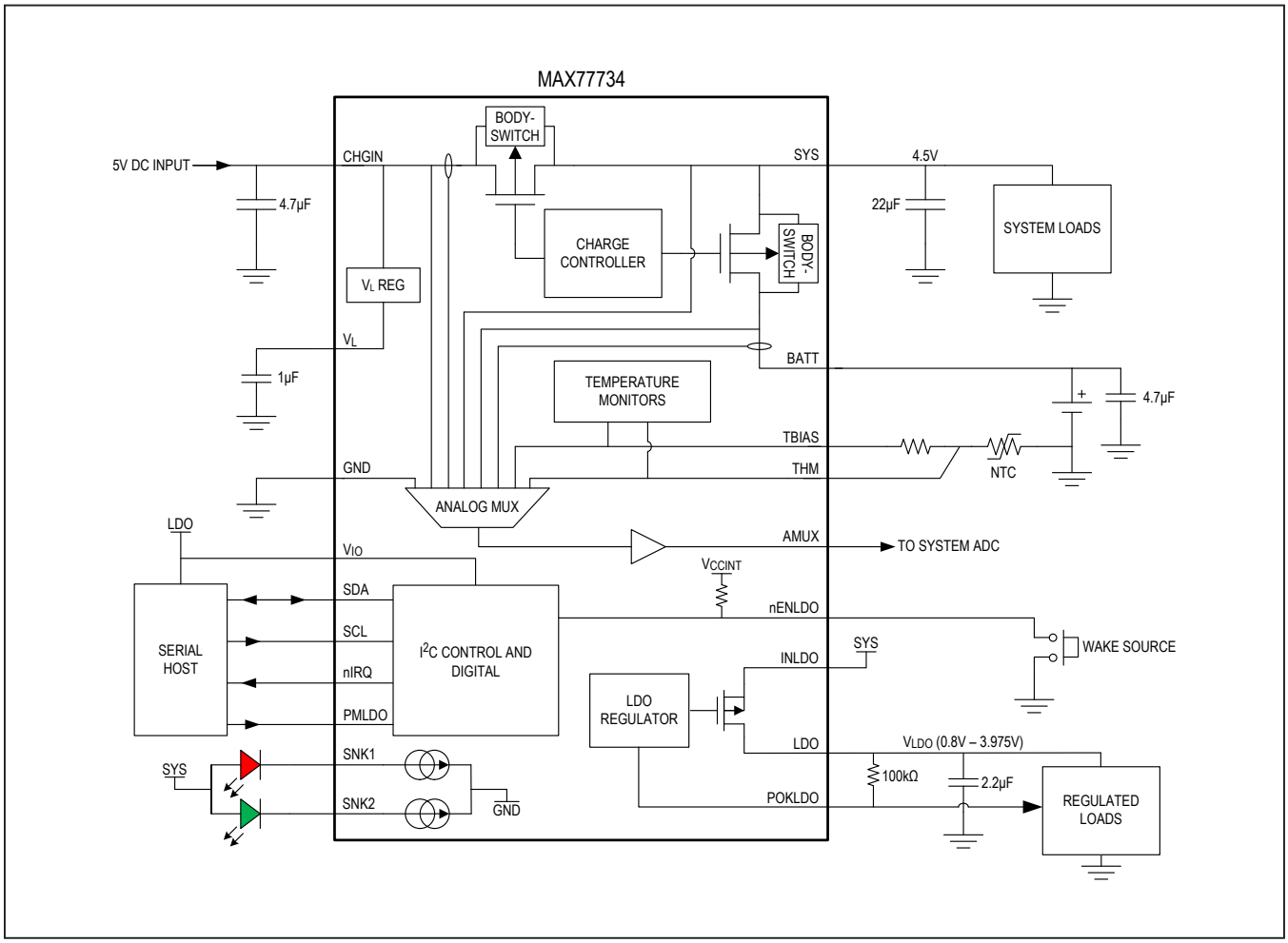
Bump Description

PIN	NAME	FUNCTION	TYPE
CHARGER			
A1	CHGIN	Charger Input. Connect to a 5V DC charging source. Bypass to GND with a 4.7µF ceramic capacitor.	power input
A2	V_L	Internal Charger 3V Logic Supply Powered from CHGIN. Bypass to GND with a 1µF ceramic capacitor. Do not load V_L externally.	power
A3	AMUX	Analog Multiplexer Output. Connect to system ADC to perform conversions on charger power signals. Leave this pin unconnected if unused.	analog output
B1	SYS	System Power Output. SYS provides power to the system resources as well as the control logic of the IC. Bypass to GND with a 22µF ceramic capacitor.	power output
B2	THM	Thermistor Monitor. Thermally couple an NTC to the battery and connect between THM and GND.	analog input
C1	BATT	Li+ Battery Connection. Connect to positive battery terminal. Bypass to GND with a 4.7µF ceramic capacitor.	power i/o
C2	TBIAS	Thermistor Bias Supply. Connect a resistor equal to the NTC's room temperature resistance between TBIAS and THM. Do not load TBIAS with other external circuitry.	analog
C3, D1	GND	Ground. Connect to the negative battery terminal and the low-impedance ground plane of the PCB.	ground

Bump Description (continued)

PIN	NAME	FUNCTION	TYPE
LINEAR REGULATOR			
A4	nENLDO	Active-Low LDO Enable Input. This digital input also causes the IC to exit factory-ship mode. Pulled up internally to V_{CCINT}. See the *Hardware Enable (nENLDO)* section.	digital input
B3	PMLDO	LDO Power-Mode Control Input. This digital input causes the LDO to change between low-power mode and normal mode when the MSB of LDO_PM[1:0] is set. See the *LDO Power Mode (PMLDO)* section.	digital input
B4	POKLDO	Open-Drain Linear Regulator Power-OK Output. Connect a 100kΩ pullup resistor between POKLDO and a voltage equal to or less than V_{SYS} if this pin is used. Leave unconnected if unused.	digital output
D4	INLDO	Linear Regulator Input. Connect to GND if unused.	power input
D5	LDO	Linear Regulator Output. Bypass to GND with a 2.2µF ceramic capacitor. Leave unconnected if unused.	power output
DUAL-CHANNEL CURRENT SINK			
D2	SNK1	Current Sink Port 1. SNK1 is typically connected to the cathode of an LED and is capable of sinking up to 12.8mA. Connect to GND if unused.	power
D3	SNK2	Current Sink Port 2. SNK2 is typically connected to the cathode of an LED and is capable of sinking up to 12.8mA. Connect to GND if unused.	power
I²C SERIAL INTERFACE			
A5	nIRQ	Active-Low, Open-Drain Interrupt Output. Connect a 100kΩ pullup resistor between nIRQ and a voltage equal to or less than V_{SYS}.	digital output
B5	SDA	I²C Serial Interface Data	digital i/o
C4	V_{IO}	I²C Serial Interface Voltage Supply	power input
C5	SCL	I²C Serial Interface Clock	digital input

Simplified Block Diagram



Detailed Description

The MAX77734 is a tiny power-management integrated circuit (PMIC) that integrates the following:

- Instant-on linear-mode lithium-ion/lithium-polymer (Li+) battery charger optimized for small battery cells (see *Detailed Description—Smart Power Selector Charger*)
- NTC thermistor monitor for automatic JEITA-safe-charging (see *Detailed Description—Adjustable Thermistor Temperature Monitors*)
- Analog Multiplexer (MUX) which enables an external ADC to monitor power (see *Detailed Description—Analog Multiplexer*)
- 150mA linear regulator (see *Detailed Description—Linear Regulator*)
- Dual-channel current sinks with individual pattern control (see *Detailed Description—Dual-Channel Current Sink Driver*)

The ICs internal top-level digital logic is described in the *On/Off Controller* section of the data sheet. The IC is fully configurable through I2C (see the *Register Map* and *Detailed Description—I2C Serial Interface*). The active-low nENLDO input can be used to wake-up the LDO using an external on-key. See *Hardware Enable (nENLDO)*.

A low-I_Q (0.2µA typ) factory-ship mode can be entered to isolate the battery node (BATT) from the system (SYS) to prevent slow cell discharge due to a high combined shutdown current of all external SYS loads (see *Factory-Ship Mode State*).

A watchdog timer can be enabled through I2C (or factory-enabled and locked) to provide supervisory reset in the event that serial activity from the host controller suddenly stops (see *Watchdog Timer*).

Additionally, a SYS voltage supervisory function is accomplished by the undervoltage (UVLO), overvoltage (OVLO), and power-on reset (POR) comparators.

On/Off Controller

The IC top-level on/off controller uses a synchronous digital state machine with a 100µs clock. Asynchronous inputs to the state machine can take up to 100µs to take effect due to clock synchronization.

The state machine is drawn in Figure 1 and Figure 2. State transition conditions are listed in Table 1.

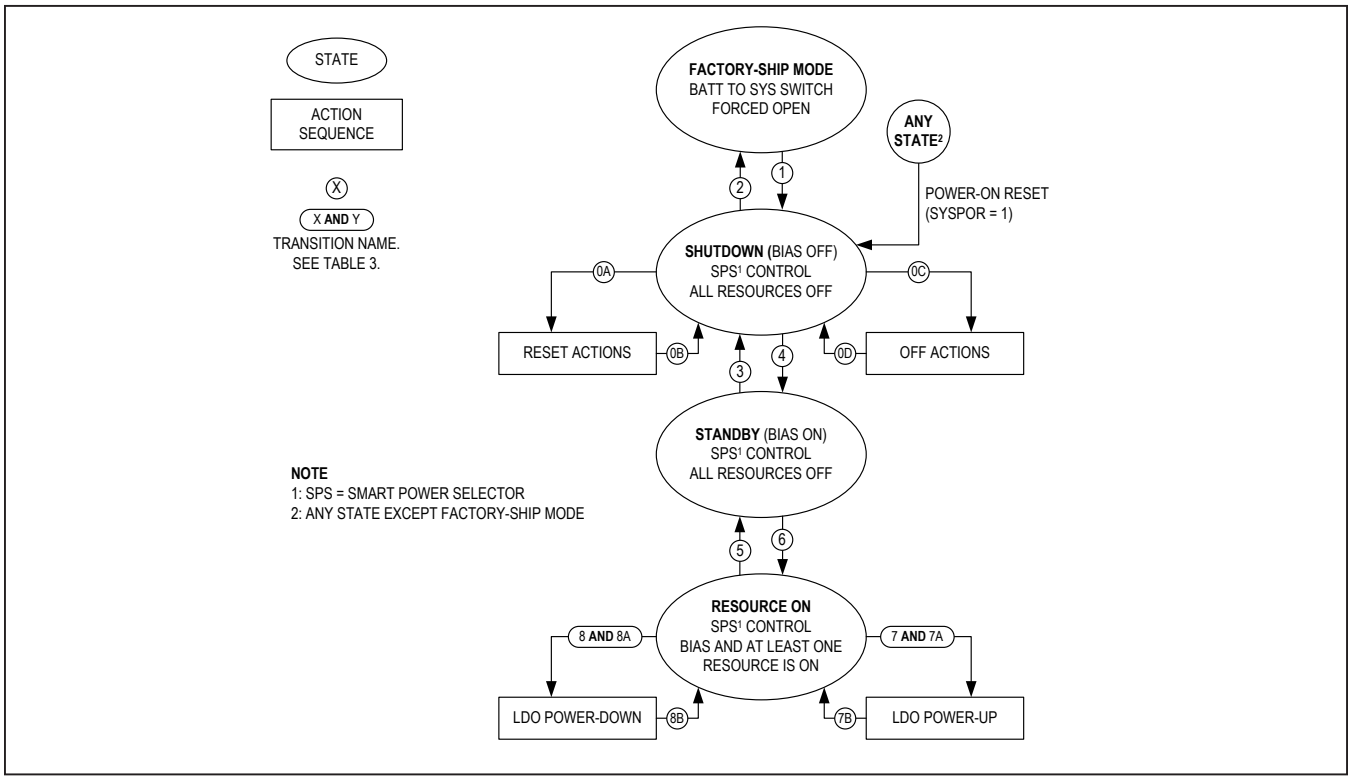


Figure 1. On/Off Controller State Machine

Table 1. On/Off Controller Transitions List

TRANSITION NUMBER	CONDITION (TRANSITION HAPPENS WHEN...)
0A	Software cold reset (SFT_CTRL[1:0] = 0b01) **OR** Watchdog timer expired causes reset (WDT_EXP = 1 and WDT_MODE = 1)
0B	Reset actions completed
0C	Software power-off (SFT_CTRL[1:0] = 0b10) **OR** Watchdog expired causes power-off (WDT_EXP = 1 and WDT_MODE = 0) **OR** Device over-temperature lockout ($T_J > T_{OTLO}$) **OR** SYS undervoltage lockout ($V_{SYS} < V_{SYSUVLO} + V_{SYSUVLO\_HYS}$) **OR** SYS overvoltage lockout ($V_{SYS} > V_{SYSOVLO}$) **OR** Manual reset occurred (MAN_RST = 1)
0D	Off Actions completed
1	CHGIN inserted and debounced valid (CHGIN_DTLS[1:0] = 0b11) **OR** nENLDO asserted for 250ms debounce timer (t_{FSM-DB}) **OR** Power to the IC is removed (V_{BATT} < approx. 1.8V) and then reapplied ($V_{BATT} > V_{POR}$)
2	Factory-ship mode requested (SFT_CTRL[1:0] = 0b11) **AND** CHGIN unplugged (CHGIN_DTLS[1:0] = 0b00)
3	NOT(4) **OR** Factory-ship mode requested (SFT_CTRL[1:0] = 0b11) **OR** Software cold reset (SFT_CTRL[1:0] = 0b01) **OR** Software power-off (SFT_CTRL[1:0] = 0b10) **OR** Watchdog timer expired (WDT_EXP = 1) **OR** Manual reset occurred (MAN_RST = 1) **OR** Device over-temperature lockout ($T_J > T_{OTLO}$) **OR** SYS undervoltage lockout ($V_{SYS} < V_{SYSUVLO} + V_{SYSUVLO\_HYS}$) **OR** SYS overvoltage lockout ($V_{SYS} > V_{SYSOVLO}$)
4	Main bias requested enabled through I^2C (BIAS_REQ = 1) **OR** 6
5	NOT(6) **OR** Factory-ship mode requested (SFT_CTRL[1:0] = 0b11) **OR** Software cold reset (SFT_CTRL[1:0] = 0b01) **OR** Software power-off (SFT_CTRL[1:0] = 0b10) **OR** Watchdog timer expired (WDT_EXP = 1) **OR** Manual reset occurred (MAN_RST = 1) **OR** Device over-temperature lockout ($T_J > T_{OTLO}$) **OR** SYS undervoltage lockout ($V_{SYS} < V_{SYSUVLO} + V_{SYSUVLO\_HYS}$) **OR** SYS overvoltage lockout ($V_{SYS} > V_{SYSOVLO}$)
6	At least one current sink is enabled (EN_SNK1 or EN_SNK2 = 1) **OR** AMUX is being used (MUX_SEL[3:0] ≠ 0b0000) **OR** CHGIN inserted and debounced valid (CHGIN_DTLS[1:0] = 0b11) **OR** LDO is forced enabled (LDO_EN[1:0] = 0b01) **OR** LDO wake-up flag is set (LDO_WAKE = 1) **OR** Internal wake-up flag is set (SFT_WAKE = 1)
7	LDO power-up sequence has not happened yet

Table 1. On/Off Controller Transitions List (continued)

TRANSITION NUMBER	CONDITION (TRANSITION HAPPENS WHEN...)
7A	LDO is forced enabled (LDO_EN[1:0] = 0b01) **OR** LDO wake-up flag is set (LDO_WAKE = 1) **OR** Internal wake-up flag is set (SFT_WAKE = 1)
7B	Done with LDO power-up
8	LDO power-down sequence has not happened yet
8A	LDO is forced disabled (LDO_EN[1:0] = 0b00) **OR** Software cold reset (SFT_CTRL[1:0] = 0b01) **OR** Software power-off (SFT_CTRL[1:0] = 0b10) **OR** Watchdog timer expired (WDT_EXP = 1) **OR** Factory-ship mode requested (SFT_CTRL[1:0] = 0b11) **OR** Manual reset occurred (MAN_RST = 1) **OR** Device over-temperature lockout ($T_J > T_{OTLO}$) **OR** SYS undervoltage lockout ($V_{SYS} < V_{SYSUVLO} + V_{SYSUVLO\_HYS}$) **OR** SYS overvoltage lockout ($V_{SYS} > V_{SYSOVLO}$)
8B	Done with LDO power-down

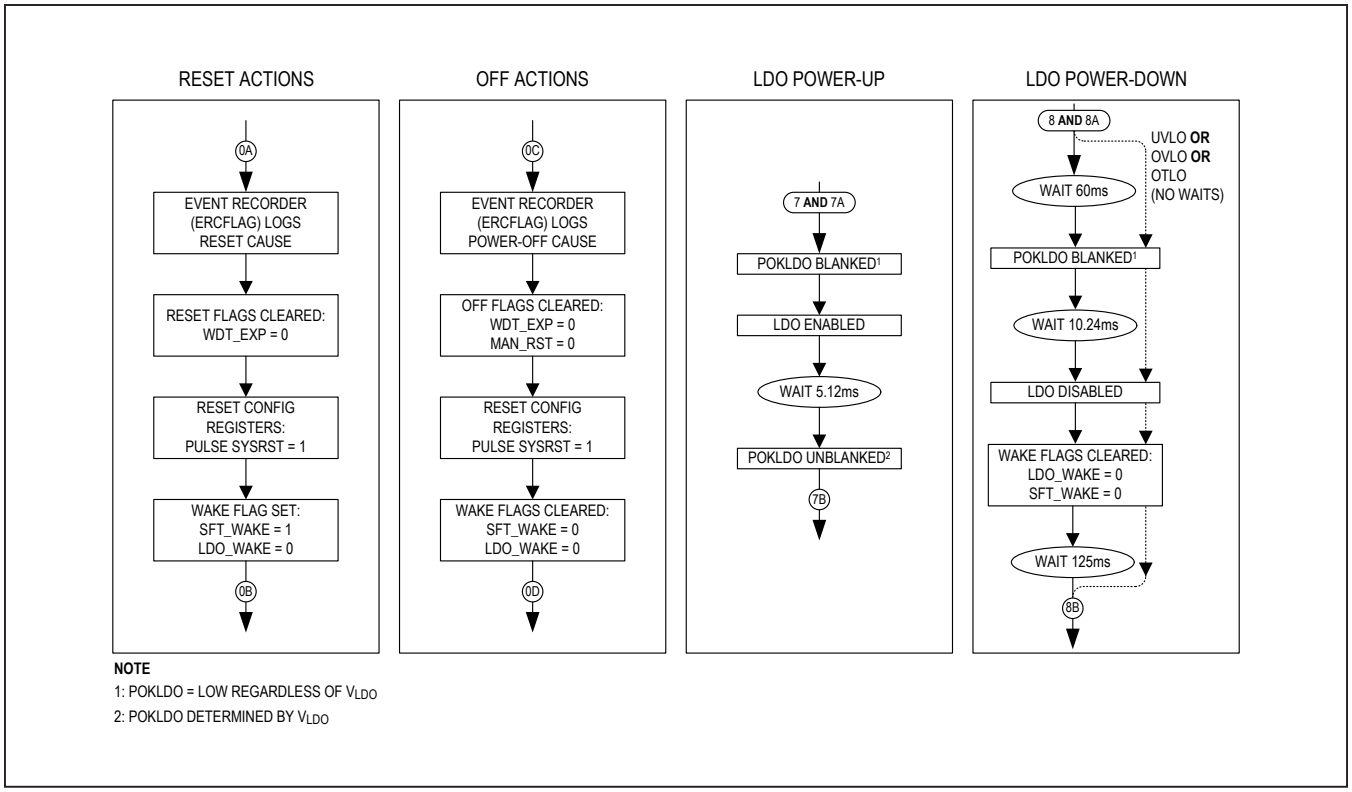


Figure 2. On/Off Controller Action Sequences

The on/off controller operates on internally latched signals decoded in Table 2.

Table 2. On/Off Controller Internal Signals

SIGNAL NAME	TYPE	DESCRIPTION	SET CONDITION	CLEAR CONDITION
WDT_EXP	Off/Reset Flag	Watchdog timer expired flag. See *Watchdog Timer*.	Watchdog timer expires	During Reset Actions, Off Actions
MAN_RST	Off/Reset Flag	Manual reset occurred. See *Manual Reset*.	nENLDO asserted for t_{MRST}	During Off Actions
LDO_WAKE	Wake Flag	LDO wakeup flag. See *LDO Enable Control*.	nENLDO debounced low or CHGIN debounced valid. LDO_EN[1:0] must be 0b10 for this flag to set.	During LDO Power-Down, Off Actions, Reset Actions
SFT_WAKE	Wake Flag	LDO software wakeup flag. See *LDO Enable Control*.	Software reset (Reset Actions) and LDO_EN[1:0] reset value is 0b10.	During Power-Down, Off Actions
EN_SNKx	Wake Flag	Final enable signal for current sink 1 and 2.	EN_SNK_MSTR = 1 and either SNK_FS1[1:0] ≠ 0b00 or SNK_FS2[1:0] ≠ 0b00	EN_SNK_MSTR = 0 or both SNK_FS1[1:0] = 0b00 and SNK_FS2[1:0] = 0b00

The state machine places a higher priority on events that cause shutdown versus events that cause power-on. In other words, moving the IC to a *lower-power* state is prioritized over moving the IC to a *higher-power* state. When two transitions are true at the same time, the state machine prioritizes action according to Table 3.

Table 3. On/Off Controller State Transition Priority

STATE	TRANSITION PRIORITY TO EXIT
FACTORY-SHIP MODE	N/A (single exit path)
SHUTDOWN	2 > 0C > 0A > 4
STANDBY	SYSPOR > 3 > 6
RESOURCE ON	SYSPOR > (8 **AND** 8A) > 5 >(7 **AND** 7A)

Factory-Ship Mode State

Factory-ship mode internally disconnects the battery (BATT) from the system (SYS). The battery does not power the system in this mode. Use this mode to preserve battery life if external circuits on SYS cause the battery to leak.

Write SFT_CTRL[1:0] = 0b11 using I²C to enter factory-ship mode. The IC responds in two different ways depending on the state of the charger input (CHGIN):

- If CHGIN is valid (CHGIN_DTLS[1:0] = 0b11) while SFT_CTRL[1:0] = 0b11, then the IC enters factory-ship mode (internally disconnects BATT from SYS) but SYS is still powered from CHGIN (regulating to $V_{SYS-REG}$). SYS decays to 0V when CHGIN is disconnected.
- If CHGIN is invalid (CHG_DTLS[1:0] ≠ 0b11) while SFT_CTRL[1:0] = 0b11, then the IC enters factory-ship mode and SYS decays to 0V.

Factory-ship mode causes many configuration registers to reset (SYSRST). Consult the *Register Map* section of the data sheet for details. I²C reads and writes can not happen in factory-ship mode.

Factory-ship mode only exits after SYS decays below approximately 1.8V. Once this condition is met, there are two ways to exit factory-ship mode:

- Apply a valid DC source at CHGIN for $t_{CHGIN-DB}$ (120ms typical). Factory-ship mode is unlatched (exited) when the charger input becomes valid from a previously invalid state (CHGIN_DTLS[1:0] = 0b00 → 0b11).
- Assert nENLDO for $t_{FSM-EXDB}$ (250ms typical) + $t_{DBNC-nENLDO}$ (0.2ms or 30ms typical).

Furthermore, this state is unlatched if power is removed from the IC (BATT voltage falls below approximately 1.8V). In all exit cases, the Smart Power Selector controls the interaction between BATT and SYS until factory-ship mode is entered again (see *Smart Power Selector*).

Shutdown (Bias Off) State

The on/off controller is in shutdown (bias off) state when no resources are enabled and CHGIN is invalid. I²C is still active as long as V_{IO} is valid.

When V_{SYS} becomes invalid ($<V_{SYSUVLO}$ or $>V_{SYSOVLO}$) or the ICs junction temperature exceeds approximately 165°C (T_{OTLO}), then the IC enters this state. This state is also entered if a manual reset event occurs (MAN_RST), the watchdog timer expires (WDT_EXP), or if software requests power-off through I²C (SFT_CTRL[1:0] = 0b10).

Shutdown state is automatically exited when a chip resource is enabled. See transition 4 in List of Transitions (Table 1).

Standby (Bias On) State

Standby state is a transitional state used to activate the IC's central bias supply before a resource is allowed to operate. Bias activation is automatically managed by the on/off controller.

Resource On State

The IC is in resource on state when at least one resource is enabled:

- CHGIN is valid (CHGIN_DTLS[1:0] = 0b11) indicating the charger resource is ready to be enabled through CHG_EN
- The analog multiplexer output buffer is being used (MUX_SEL[3:0] ≠ 0b0000)
- The LDO is enabled
- At least one of the current sinks is activated (EN_SNK_MSTR = 1 and SNK_FS1/2 ≠ 0b00)

The wake flags in Table 2 also cause the on/off controller to enter this state.

Hardware Enable (nENLDO)

nENLDO is an active-low, internally debounced digital input with internal pullup resistors. nENLDO's input signal typically comes from a physical on-key. Asserting nENLDO sets LDO_WAKE (see Table 2). This input is also used to exit factory-ship mode (see *Factory-Ship Mode State*).

The debounce time is programmable with DB_nENLDO to either 200µs or 30ms. Both rising and falling edges are debounced. Maskable rising and falling interrupts (nENLDO_R and nENLDO_F) are available to signal a change in nENLDO's status. The debounced status of this input is continuously mirrored by the STAT_ENLDO bit. Consult the *Register Map* for more details.

Manual Reset

Asserting nENLDO for an extended period of time causes the IC to shutdown (MAN_RST = 1).

If nENLDO is continuously asserted for t_{MRST} (8 or 16 seconds depending on T_MRST bit), then the on/off controller shuts down the IC and resets configuration registers (SYSRST). The default value of T_MRST can be factory-programmed. See the *Register Map* for additional details.

The manual reset function is useful for forcing a register reset and power-down in case communication with the host controller fails. End-applications frequently call this a "hard reset".

The manual reset timer counts differently based on the type of on-key (push-button or slide-switch). See *Push-Button vs. Slide-Switch Functionality*.

Push-Button vs. Slide-Switch Functionality

The nENLDO manual reset ("hard-reset") can be configured to work with a push-button switch or a slide-switch using the nENLDO_MODE bit.

Use nENLDO_MODE = 0 for normally-open, momentary, and push-buttons. In this mode, the manual reset timer counts t_{MRST} while nENLDO is low (a long button press and hold).

Use nENLDO_MODE = 1 for persistent slide-switches. In this mode, the manual reset timer counts t_{MRST} while nENLDO is high (switch in off position). If the host controller fails to issue a software shutdown command in t_{MRST} after nENLDO goes high, then the on/off controller automatically causes a register reset and shutdown.

The default value of nENLDO_MODE is factory-programmable. Figure 3 shows a visual example of how nENLDO_MODE changes how t_{MRST} is counted.

nENLDO Pullup Resistors to V_{CCINT} (V_{CC} Internal)

V_{CCINT} is an always-on internal voltage domain. The nENLDO logic thresholds are referenced to V_{CCINT}. There are internal pullup resistors between nENLDO and V_{CCINT} (R_{nEN-PU}). See Figure 4. The pullup strength can be modified with the PU_DIS bit. While PU_DIS = 0, the pullup value is approximately 200kΩ (typ). While PU_DIS = 1, the pullup value is 10MΩ (typ).

V_{CCINT} is defined by the following conditions:

- If CHGIN is valid (CHGIN_DTLS[1:0] = 0b11) and not USB suspended (USBS = 0), then V_{CCINT} equals V_L (3V typ).
- If CHGIN is invalid (CHGIN_DTLS[1:0] ≠ 0b11) or CHGIN is valid but USB suspended (USBS = 1) then V_{CCINT} equals V_{BATT}.

Applications using a slide-switch on-key connected to nENLDO can optimize quiescent current consumption by changing pullup strength to 10MΩ by setting PU_DIS to 1. This is because a slide-switch in the "on position" connects nENLDO to ground and creates a path for BATT to leak (since V_{CCINT} = V_{BATT} while CHGIN is not present). Applications using normally-open, momentary, and push-button on-keys (as shown in Figure 4) do not create this leakage path and should use the stronger 200kΩ pullup option (PU_DIS = 0).

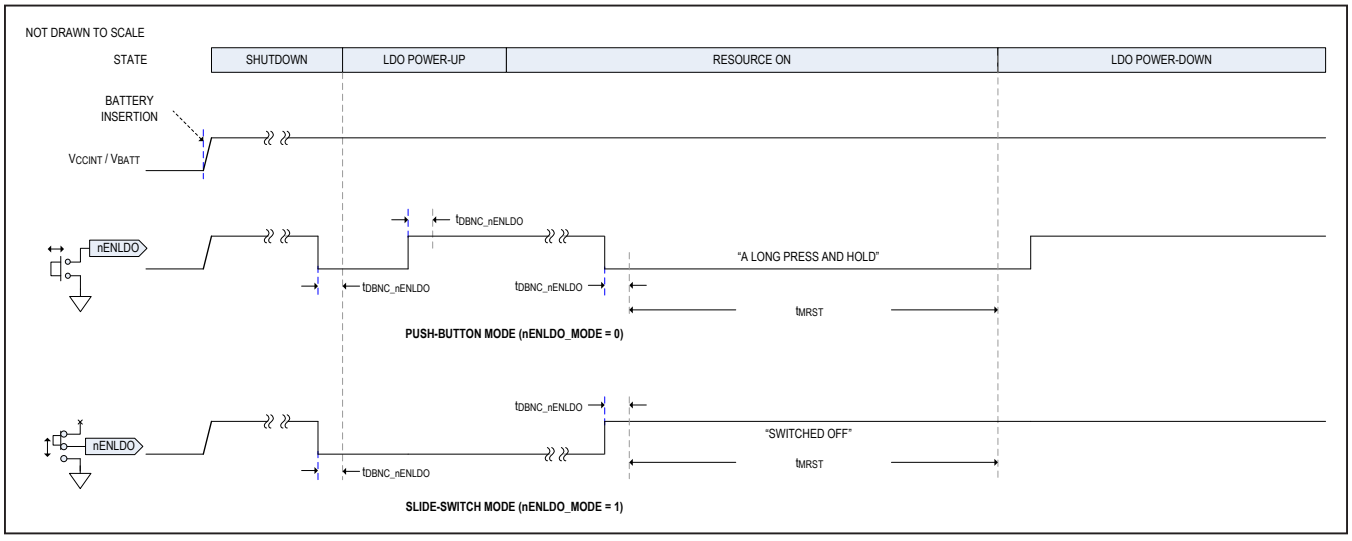


Figure 3. nENLDO Dual-Functionality Timing Diagram

Interrupts (nIRQ)

nIRQ is an active-low, open-drain output that is typically routed to the host processor's interrupt input to signal an important change in the ICs status. See the *Register Map* for a full list of available status and interrupt bits.

A pullup resistor to a voltage less than or equal to V_{SYS} is required for this node. nIRQ is the logical *NOR* of all unmasked interrupt bits in the ICs register map.

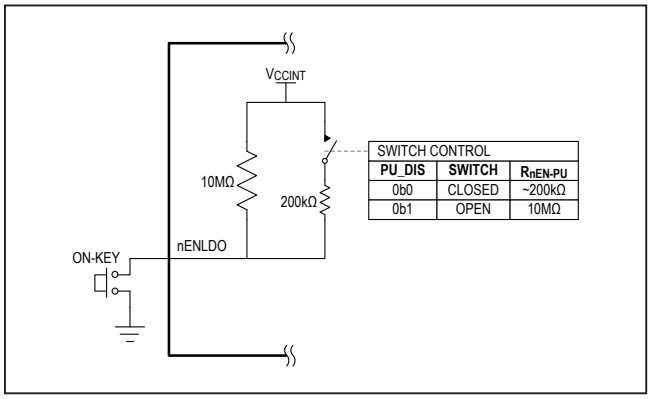


Figure 4. nENLDO Pullup Resistor Configuration

All interrupts are masked by default. Masked interrupt bits do not cause the nIRQ pin to change. Unmask the interrupt bits to allow nIRQ to assert.

Watchdog Timer

The IC features a watchdog timer function for operational safety. If this timer expires without being cleared, then an internal signal called WDT_EXP asserts and the on/off controller causes the IC to enter the shutdown state and resets configuration registers. See the *On/Off Controller* and *List of Transitions* (transitions 0A and 0C) for more details.

Write WDT_EN = 1 through I^2C to enable the timer. The watchdog timer period (t_{WD}) is configurable from 16 to 128 seconds in 4 steps with WDT_PER[1:0]. The default timer period is 128 seconds. The WDT_CLR bit must be set through I^2C periodically (within t_{WD}) to reset the timer and prevent shutdown. Consult the *Register Map* and *Watchdog Timer State Machine* (Figure 5) for additional details.

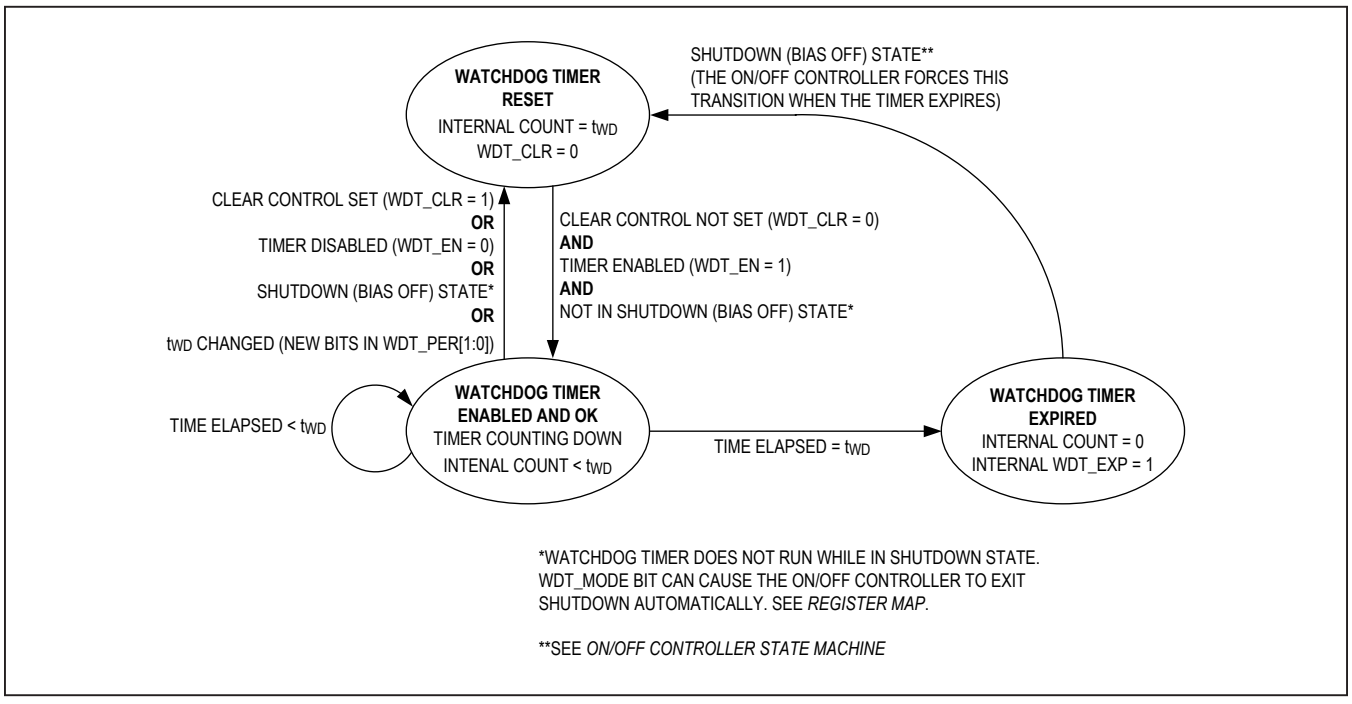


Figure 5. Watchdog Timer State Machine

The timer can be factory-programmed to be enabled by default, disabled by default, or locked from accidental disable. The WDT_LOCK bit is read-only and must be configured at the factory. See Table 4 for a full description.

Thermal Alarms and Protection

The IC has thermal alarms to monitor if the junction temperature rises above 80°C (T_{JAL1}) and 100°C (T_{JAL2}). Over-temperature lockout (OTLO) is entered if the junction temperature exceeds T_{OTLO} (approximately 165°C, typ). OTLO causes all resources to turn off immediately. Resources may not enable until the temperature falls below T_{OTLO} by approximately 15ºC.

The TJAL1_S and TJAL2_S status bits continuously indicate the junction temperature alarm status. Maskable interrupts are available to signal a change in either of these bits. Consult the *Register Map* for details.

Register Reset Conditions

The IC's registers reset to default values when the corresponding reset condition for each particular bit becomes true. Table 5 lists all register reset conditions. See the *Register Map* for a list of every configuration and status bit and the associated reset value and reset condition.

Factory Options

Table 6 shows the factory-programmable (OTP) options for the IC. Refer to the *Ordering Information* and *Register Map* for more information about the different default register functions.

Table 4. Watchdog Timer Factory-Programmed Safety Options

WDT_LOCK	WDT_EN	FUNCTION
0	0	Watchdog timer is disabled by default. Timer can be enabled or disabled by I²C writes.
0	1	Watchdog timer is enabled by default. Timer can be enabled or disabled by I²C writes.
1	0	Watchdog timer is disabled by default. Timer can be enabled by an I²C write, but only a SYSRST can reset the WDT_EN value back to 0. Timer can not be disabled by direct I²C writes to WDT_EN (write from 1 → 0 is ignored, write from 0 → 1 is accepted).
1	1	Watchdog timer is enabled by default. Nothing can disable the timer.

Table 5. Register Reset Conditions

RESET CONDITION	NAME	RESET CAUSE AND DETAILS
SYSPOR	System Power-On Reset	V_{SYS} < 1.9V (typ)
SYSRST	System Reset	SYSPOR **OR** On/off controller (see transitions 0A and 0C in Table 1)
CHGPOK	Charger Power-OK	CHGPOR **OR** USB suspend (USBS = 1) **OR** V_{CHGIN} < V_{CHGIN_UVLO} (typ. 4V rising, 3.5V falling)
CHGPOR	Charger Power-On Reset	V_{CHGIN} < 1.9V (typ)

Table 6. Factory-Programmed Defaults (OTP Options)

	MAX77734BENP	**MAX77734C**ENP
Option Letter	B	C
Chip Identification	CID[3:0] = 0x1	CID[3:0] = 0x3
I^2C Device Address (7-bit)	0x48	0x48
$V_{SYSUVLO}$ (falling UVLO threshold)	2.85V	2.85V
$V_{SYSUVLO\_HYS}$ (UVLO hysteresis)	0.15V	0.15V
CHG_EN (default charger enable bit)	0 (disabled)	0 (disabled)
$I_{CHGIN-LIM}$ (default input current limit)	475mA	95mA
LDO_VREG[6:0] (default LDO voltage)	0x28 (1.8V)	0x64 (3.3V)
LDO_EN[1:0] (default LDO enable)	0b00 (disabled)	0b10 (hardware enable)
DB_nENLDO (nENLDO input debounce time)	1 (30ms)	1 (30ms)
nENLDO_MODE (button type)	0 (push-button)	0 (push-button)
T_MRST (manual reset time)	0 (8s)	0 (8s)
WDT_EN (watchdog timer enable)	0 (disabled)	0 (disabled)
WDT_LOCK (watchdog timer enable lock)	0 (unlocked)	0 (unlocked)

Detailed Description—Smart Power Selector Charger

The linear Li+ charger implements power path with Maxim's Smart Power Selector. This allows separate input current limit and battery charge current settings. Batteries charge faster under the supervision of the Smart Power Selector because charge current is independently regulated and not shared with variable system loads. See the *Smart Power Selector* section for more information.

The programmable constant-current charge rate (7.5mA to 300mA) supports a wide range of battery capacities. The programmable input current limit (95mA to 475mA) supports a range of charge sources, including USB. The charger's programmable battery regulation voltage range (3.6V–4.6V) supports a wide variety of cell chemistries. Small battery capacities are supported; the charger accurately terminates charging by detecting battery currents as low as 0.375mA.

Additionally, the robust charger input withstands overvoltages up to 28V. To enhance charger safety, an NTC thermistor provides temperature monitoring in accordance with the JEITA recommendations. See the *Detailed Description—Adjustable Thermistor Temperature Monitors* section for more information.

Charger Symbol Reference Guide

Table 7 lists the names and functions of charger-specific signals and if they can be programmed through I^2C. Consult the *Electrical Characteristics* and *Register Map* for more information.

Figure 6 indicates the high-level functions of each control circuit within the linear charger.

Smart Power Selector

The Smart Power Selector seamlessly distributes power from the input (CHGIN) to the battery (BATT) and the system (SYS). The Smart Power Selector basic functions are:

- When the system load current is less than the input current limit, the battery is charged with residual power from the input.
- When a valid input source is connected, the system regulates to $V_{SYS-REG}$ to power system loads regardless of the battery's voltage (instant on).
- When the system load current exceeds the input current limit, the battery provides additional current to the system (supplement mode).
- When the battery is finished charging and an input source is present to power the system, the battery remains disconnected from the system.
- When the battery is connected and there is no input power, the system is powered from the battery.

Table 7. Charger Quick Symbol Reference Guide

SYMBOL	NAME	I²C PROGRAMMABLE?
V_{CHGIN_OVP}	CHGIN overvoltage threshold	No
V_{CHGIN_UVLO}	CHGIN undervoltage-lockout threshold	No
$V_{CHGIN-MIN}$	Minimum CHGIN voltage regulation setpoint	Yes, through VCHGIN_MIN[2:0]
$I_{CHGIN-LIM}$	CHGIN input current limit	Yes, through ICHGIN_LIM[2:0]
$V_{SYS-REG}$	SYS voltage regulation target	Yes, through VSYS_REG[4:0]
$V_{SYS-MIN}$	Minimum SYS voltage regulation setpoint	No, tracks $V_{SYS-REG}$
$V_{FAST-CHG}$	Fast-charge constant-voltage level	Yes, through CHG_CV[5:0]
$I_{FAST-CHG}$	Fast-charge constant-current level	Yes, through CHG_CC[5:0]
I_{PQ}	Prequalification current level	Yes, through I_PQ
V_{PQ}	Prequalification voltage threshold	Yes, through CHG_PQ[2:0]
I_{TERM}	Termination current level	Yes, through I_TERM[1:0]
T_{J-REG}	Die temperature regulation setpoint	Yes, through TJ_REG[2:0]
t_{PQ}	Prequalification safety timer	No
t_{FC}	Fast-charge safety timer	Yes, through T_FAST_CHG[1:0]
t_{TO}	Top-off timer	Yes, through T_TOPOFF[2:0]

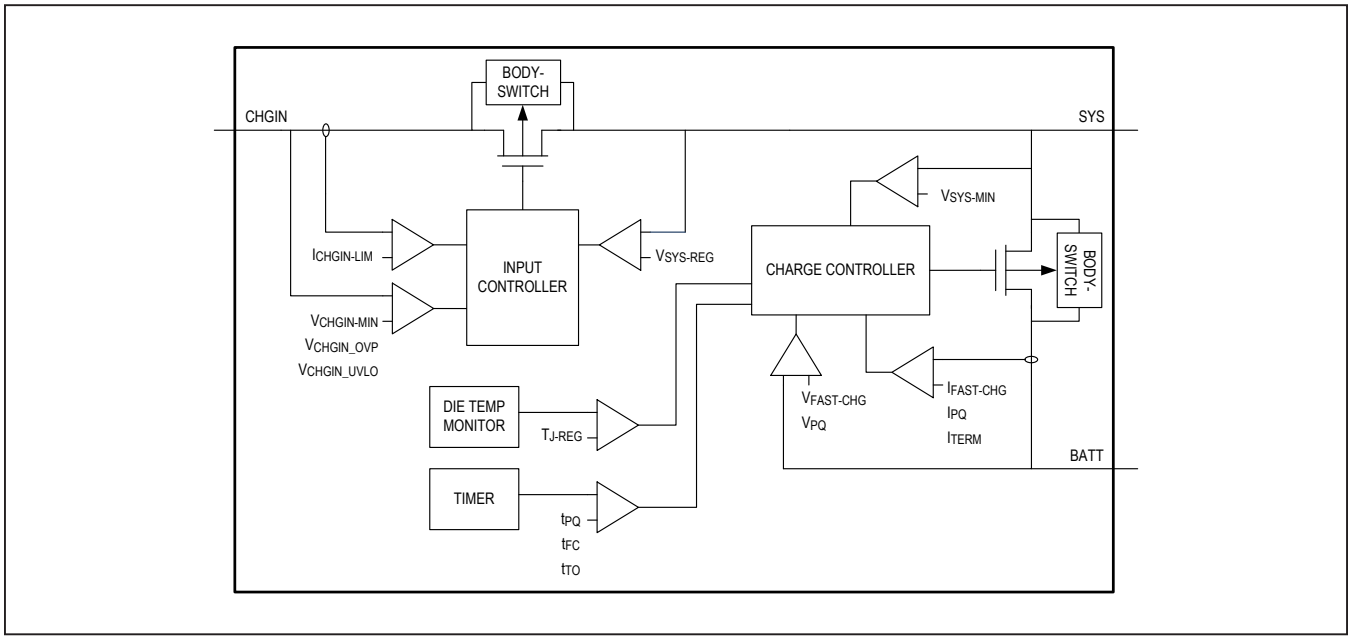


Figure 6. Charger Simplified Control Loops

Input Current Limiter

The input current limiter limits CHGIN current to not exceed $I_{CHGIN-LIM}$ (programmed by ICHGIN_LIM[2:0]). A maskable interrupt (CHGIN_CTRL_I) signals when the input current limit engages. The ICHGIN_LIM_STAT bit reflects the state of the current limiter loop.

The default value of $I_{CHGIN-LIM}$ is factory-programmable to either 95mA or 475mA. The decoding of the ICHGIN_LIM[2:0] bitfield changes depending on the factory-programmed default value (see Table 8). The reset value of this bitfield is always 0b000 regardless of factory option.

CHGIN is capable of standing off 28V from ground. CHGIN suspends power delivery to the system and battery when V_{CHGIN} exceeds V_{CHGIN_OVP} (7.5V, typ). The input circuit also suspends when V_{CHGIN} falls below V_{CHGIN_UVLO} minus 500mV of hysteresis (3.5V, typ). While in OVP or UVLO, the charger remains off and the battery provides power to the system.

Power transfer to SYS is delayed by a 120ms debounce timer ($t_{CHGIN-DB}$) after a valid DC source is connected to CHGIN. SYS does not begin regulating to $V_{SYS-REG}$ until after the timer expires.

The CHGIN_DTLS[1:0] bitfield continuously indicates the state of CHGIN's voltage quality. A maskable interrupt (CHGIN_I) asserts when CHGIN_DTLS[1:0] changes.

Minimum Input Voltage Regulation

In the event of a poor-quality charge source, the minimum input voltage regulation loop works to reduce input current if V_{CHGIN} falls below $V_{CHGIN-MIN}$ (programmed by VCHGIN_MIN[2:0]). This is important because many commonly used charge adapters feature foldback protection mechanisms where the adapter completely shuts off if its output drops too low. The minimum input voltage regulation loop also prevents V_{CHGIN} from dropping below V_{CHGIN_UVLO} if the cable between the charge source and the charger's input is long or highly resistive.

Table 8. Input Current Limit Factory Options

ICHGIN_LIM [2:0]	95mA FACTORY-DEFAULT	475mA FACTORY-DEFAULT
0b000	95mA	475mA
0b001	190mA	380mA
0b010	285mA	285mA
0b011	380mA	190mA
0b100 - 0b111	475mA	95mA

The input voltage regulation loop improves performance with current limited adapters. If the charger's input current limit is programmed above the current limit of the given adapter, the input voltage loop allows the input to regulate at the current limit of the adapter. The input voltage regulation loop also allows the charger to perform well with adapters that have poor transient load response times.

A maskable interrupt (CHGIN_CTRL_I) signals when the minimum input voltage regulation loop engages. The state of this loop is reflected by VCHGIN_MIN_STAT.

Minimum System Voltage Regulation

The minimum system voltage regulation loop ensures that the system rail remains close to the programmed SYS regulation voltage ($V_{SYS-REG}$) regardless of system loading. The loop engages when the combined battery charge current and system load current causes the CHGIN input to current limit at $I_{CHGIN-LIM}$. When this happens, the minimum system voltage loop reduces charge current in an attempt to keep the input out of current limit, thereby keeping the system voltage above $V_{SYS-MIN}$ ($V_{SYS-REG}$ - 100mV, typ). If this loop reduces battery current to 0 and the system is in need of more current than the input can provide, then the Smart Power Selector overrides the minimum system voltage regulation loop and allows SYS to collapse to BATT for the battery to provide supplement current to the system. The Smart Power Selector automatically reenables the minimum system voltage loop when the supplement event has ended.

A maskable interrupt (SYS_CTRL_I) asserts to signal a change in VSYS_MIN_STAT. This status bit asserts when the minimum system voltage regulation loop is active.

Die Temperature Regulation

If the die temperature exceeds T_{J-REG} (programmed by TJ_REG[2:0]) the charger attempts to limit the temperature increase by reducing battery charge current. The TJ_REG_STAT bit asserts whenever charge current is reduced due to this loop. The charger's current sourcing capability to SYS remains unaffected when TJ_REG_STAT is high. A maskable interrupt (TJ_REG_I) asserts to signal a change in TJ_REG_STAT. Use the TJ_REG_I interrupt to signal the system processor to reduce loads on SYS to reduce total system temperature.

Charger State Machine

The battery charger follows a strict state-to-state progression to ensure that a battery is charged safely. The status bitfield CHG_DTLS[3:0], reflects the charger's current operational state. A maskable interrupt (CHG_I) is available to signal a change in CHG_DTLS[3:0].

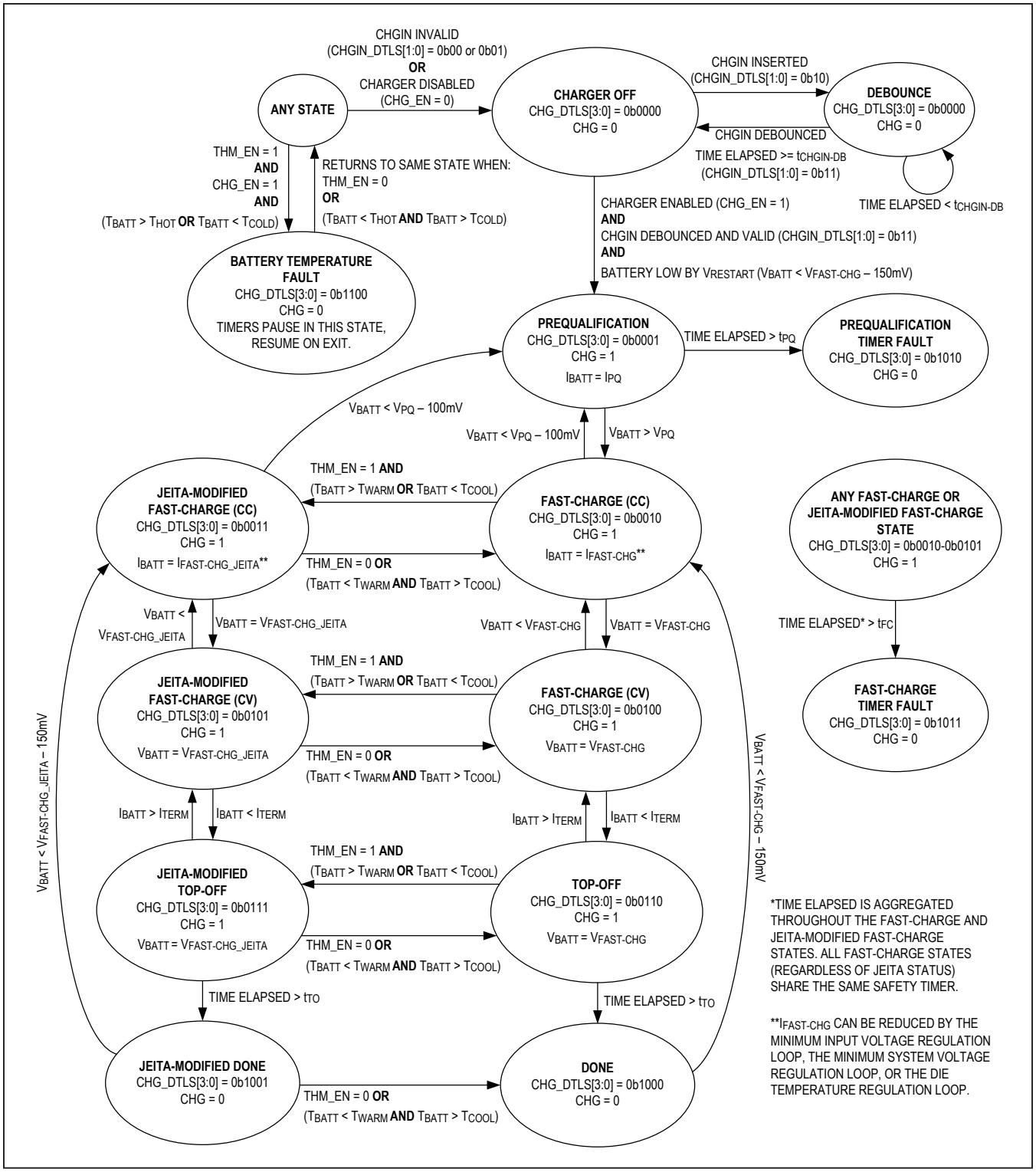


Figure 7. Charger State Diagram

Charger Off State

The charger is off when CHGIN is invalid, the charger is disabled, or the battery is fresh.

CHGIN is invalid when the CHGIN input is invalid ($V_{CHGIN} < V_{CHGIN\_UVLO}$ or $V_{CHGIN} > V_{CHGIN\_OVP}$). While CHGIN is invalid, the battery is connected to the system. CHGIN voltage quality can be separately monitored by the CHGIN_DTLS[1:0] status bitfield. Refer to the *Register Map* for details.

The charger is disabled when the charger enable bit is 0 (CHG_EN = 0). The battery is connected or disconnected to the system depending on the validity of V_{CHGIN} while CHG_EN = 0. See the *Smart Power Selector* section.

The battery is fresh when CHGIN is valid and the charger is enabled (CHG_EN = 1) and the battery is not low by $V_{RESTART}$ ($V_{BATT} > V_{FAST\text{-}CHG} - V_{RESTART}$). The battery is disconnected from the system and not charged while the battery is fresh. The charger state machine exits this state and begins charging when the battery becomes low by $V_{RESTART}$ (150mV, typ). This condition is functionally similar to done state. See *Done State* section.

Prequalification State

The prequalification state is intended to assess a low-voltage battery's health by charging at a reduced rate. If the battery voltage is less than the V_{PQ} threshold, the charger is automatically in prequalification. If the cell voltage does not exceed V_{PQ} in 30 minutes (t_{PQ}), the charger faults. The prequalification charge rate is a percentage of $I_{FAST\text{-}CHG}$ and is programmable with I_PQ. The prequalification voltage threshold (V_{PQ}) is programmable through CHG_PQ[2:0].

Fast-Charge States

When the battery voltage is above V_{PQ}, the charger transitions to the fast-charge (CC) state. In this state, the charger delivers a constant current ($I_{FAST\text{-}CHG}$) to the cell. The constant current level is programmable from 7.5mA to 300mA by CHG_CC[5:0].

When the cell voltage reaches $V_{FAST\text{-}CHG}$, the charger state machine transitions to fast-charge (CV). $V_{FAST\text{-}CHG}$ is programmable with CHG_CV[5:0] from 3.6V to 4.6V. The charger holds the battery's voltage constant at $V_{FAST\text{-}CHG}$ while in the fast-charge (CV) state. As the battery approaches full, the current accepted by the battery reduces. When the charger detects that battery charge current has fallen below I_{TERM}, the charger state machine enters the top-off state.

A fast-charge safety timer starts when the state machine enters fast-charge (CC) or JEITA-modified fast-charge (CC) from a non-fast-charge state. The timer continues to run through all fast-charge states regardless of JEITA status. The timer length (t_{FC}) is programmable from 3 hours to 7 hours in 2 hour increments with T_FAST_CHG[1:0]. If it is desired to charge without a safety timer, program T_FAST_CHG[1:0] with 0b00 to disable the feature. If the timer expires before the fast-charge states are exited, the charger faults. See the *Fast-Charge Timer Fault State* section for more information.

If the charge current falls below 20% of the programmed value during fast-charge (CC), the safety timer pauses. The timer also pauses for the duration of supplement mode events. The TIME_SUS bit indicates the status of the fast-charge safety timer. Refer to the *Register Map* for more details.

Top-Off State

Top-off state is entered when the battery charge current falls below I_{TERM} during the fast-charge (CV) state. I_{TERM} is a percentage of $I_{FAST\text{-}CHG}$ and is programmable through I_TERM[1:0]. While in the top-off state, the battery charger continues to hold the battery's voltage at $V_{FAST\text{-}CHG}$. A programmable top-off timer starts when the charger state machine enters the top-off state. When the timer expires, the charger enters the done state. The top-off timer value (t_{TO}) is programmable from 0 minutes to 35 minutes with T_TOPOFF[2:0]. If it is desired to stop charging as soon as battery current falls below I_{TERM}, program t_{TO} to 0 minutes.

Done State

The charger enters the done state when the top-off timer expires. The battery remains disconnected from the system during done. The charger restarts if the battery voltage falls more than $V_{RESTART}$ (150mV, typ) below the programmed $V_{FAST\text{-}CHG}$ value.

Prequalification Timer Fault State

The prequalification timer fault state is entered when the battery's voltage fails to rise above V_{PQ} in t_{TO} (30 minutes, typ) from when the prequalification state was first entered. If a battery is too deeply discharged, damaged, or internally shorted, the prequalification timer fault state can occur. During the timer fault state, the charger stops delivering current to the battery and the battery remains disconnected from the system. To exit the prequalification timer fault state, toggle the charger enable (CHG_EN) bit or unplug and replug the external voltage source connected to CHGIN.

Fast-Charge Timer Fault State

The charger enters the fast-charge timer fault state if the fast-charge safety timer expires. While in this state, the charger stops delivering current to the battery and the battery remains disconnected from the system. To exit the fast-charge timer fault state, toggle the charger enable bit (CHG_EN) or unplug and replug the external voltage source connected to CHGIN.

Battery Temperature Fault State

If the thermistor monitoring circuit reports that the battery is either too hot or too cold to charge (as programmed by THM_HOT[1:0] and THM_COLD[1:0]), the state machine enters the battery temperature fault state. While in this state, the charger stops delivering current to the battery and the battery remains disconnected from the system. This state can only be entered if the thermistor is enabled (THM_EN = 1). Battery temperature fault state has priority over any other fault state, and can be exited when the thermistor is disabled (THM_EN = 0) or when the battery returns to an acceptable temperature. When this fault state is exited, the state machine returns to the last state it was in before battery temperature fault state was entered.

All active charger timers (fast-charge safety timer, prequalification timer, or top-off timer) are paused in this state. Active timers resume when the state is exited.

The THM_DTLS[2:0] bitfield reports battery temperature status. See the *Electrical Characteristics—Adjustable Thermistor Temperature Monitors* section and refer to the *Register Map* for more information.

JEITA-Modified States

If the thermistor is enabled (THM_EN = 1), then the charger state machine is allowed to enter the JEITA-modified states. These states are entered if the charger's temperature monitors indicate that the battery temperature is either warm (greater than T_{WARM}) or cool (lesser than T_{COOL}). See the *Electrical Characteristics—Adjustable Thermistor Temperature Monitors* section for more information about setting the temperature thresholds.

The charger's current and voltage parameters change from $I_{FAST-CHG}$ and $V_{FAST-CHG}$ to $I_{FAST-CHG\_JEITA}$ and $V_{FAST-CHG\_JEITA}$ while in the JEITA-modified states. The JEITA modified parameters can be independently set to lower voltage and current values so that the battery can charge safely over a wide range of ambient temperatures. If the battery temperature returns to normal, or the thermistor is disabled (THM_EN = 0), the charger exits the JEITA-modified states.

Typical Charge Profile

A typical battery charge profile (and state progression) is illustrated in Figure 8.

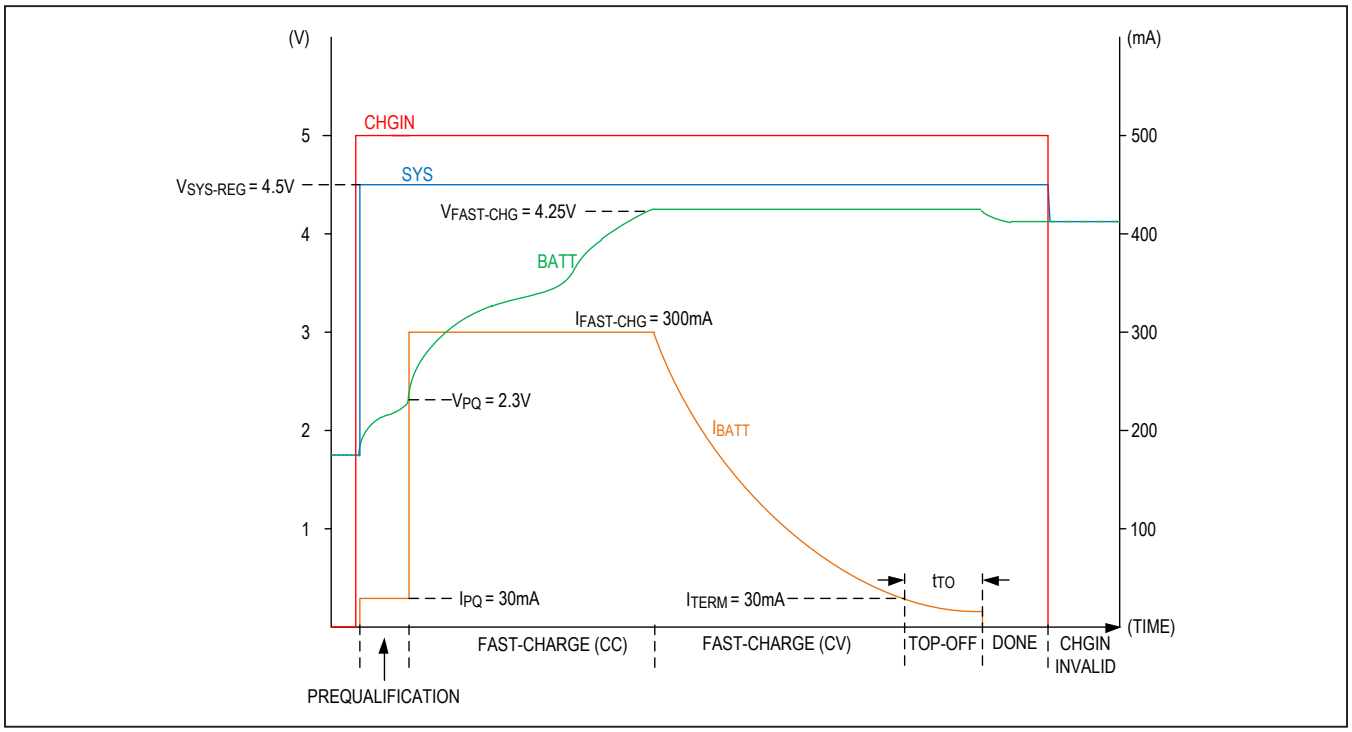


Figure 8. Example Battery Charge Profile

Charger Applications Information

Configuring a Valid System Voltage

The Smart Power Selector begins to regulate SYS to $V_{SYS-REG}$ when CHGIN is connected to a valid source. To ensure the charger's accuracy specified in the *Electrical Characteristics* table, the system voltage must always be programmed at least 200mV above the charger's constant-voltage level ($V_{FAST-CHG}$). If this condition is not met, then the charger's internal configuration logic forces $V_{FAST-CHG}$ to reduce to satisfy the 200mV requirement. If this happens, the charger asserts the SYS_CNFG_I interrupt to alert the user that a configuration error has been made and that the bits in CHG_CV[5:0] have changed to reduce $V_{FAST-CHG}$.

CHGIN/SYS/BATT Capacitor Selection

Bypass CHGIN to GND with a 4.7µF ceramic capacitor to minimize inductive kick caused by long cables between the DC charge source and the product/IC. Larger values increase decoupling for the linear charger, but increase inrush current from the DC charge source when the product/IC is first connected to a source through a cable/plug. If the DC charging source is an upstream USB device, limit the maximum CHGIN input capacitance based on the appropriate USB specification (i.e., typically no more than 10µF).

Bypass SYS to GND with a 22µF ceramic capacitor. This capacitor is needed to ensure stability of SYS while it is being regulated from CHGIN. Larger values of SYS capacitance increase decoupling for all SYS loads. The effective value of the SYS capacitor must be greater than 4µF and no more than 100µF. Bypass BATT to GND with a 4.7µF ceramic capacitor. This capacitor is required to ensure stability of the BATT voltage regulation loop. The effective value of the BATT capacitor must be greater than 1µF.

Ceramic capacitors with X5R or X7R dielectric are highly recommended due to their small size, low ESR, and small temperature coefficients. All ceramic capacitors derate with DC bias voltage (effective capacitance goes down as DC bias goes up). Generally, small case size capacitors derate heavily compared to larger case sizes (0603 case size performs better than 0402). Consider the effective capacitance value carefully by consulting the manufacturer's data sheet.

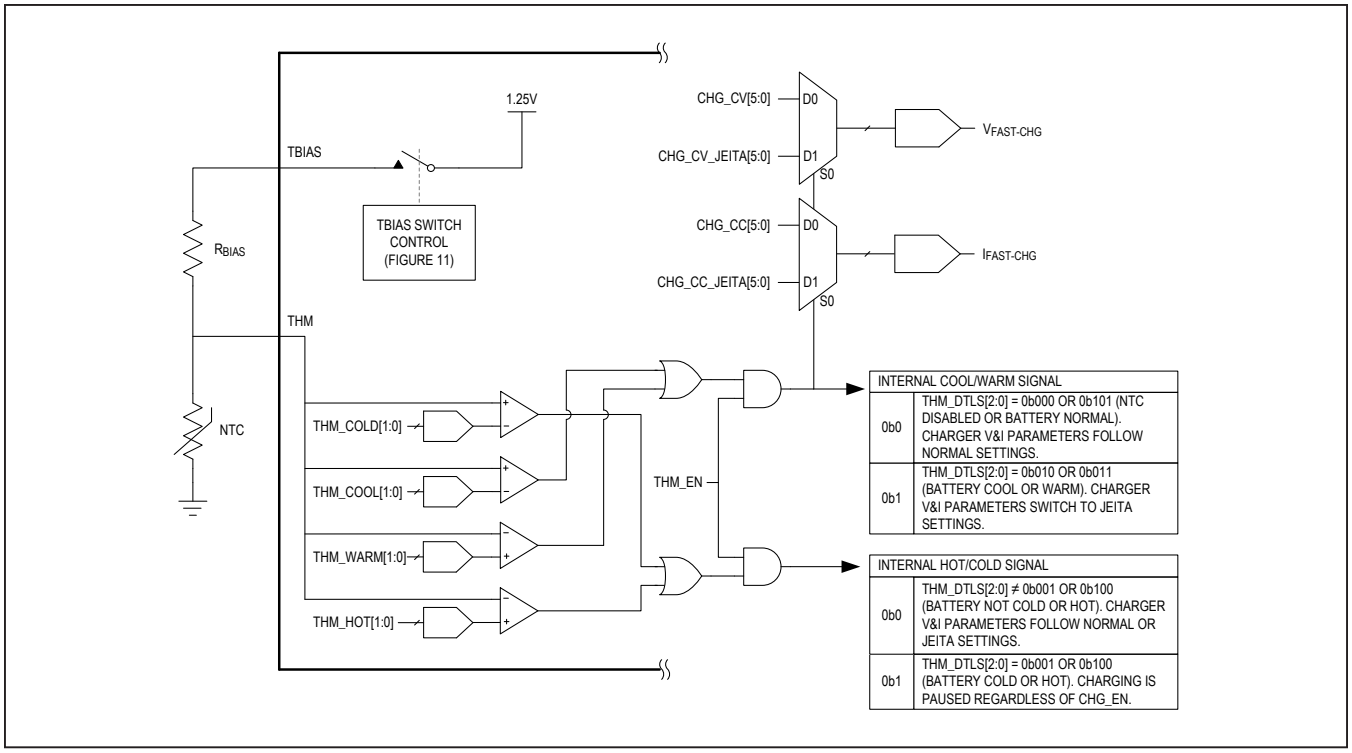


Figure 9. Thermistor Logic Functional Diagram

Detailed Description—Adjustable Thermistor Temperature Monitors

The optional use of a negative temperature coefficient (NTC) thermistor (thermally coupled to the battery) enables the charger to operate safely over the JEITA temperature range. When the thermistor is enabled (THM_EN = 1), the charger continuously monitors the voltage at the THM pin in order to sense the temperature of the battery being charged.

See Figure 10 for a visual example of the following text:

- If the battery temperature is higher than T_{COOL} and lower than T_{WARM}, the battery charges normally with the normal values for $V_{FAST-CHG}$ and $I_{FAST-CHG}$. The charger state machine does not enter JEITA-modified states while the battery temperature is normal.
- If the battery temperature is either above T_{WARM} but below T_{HOT}, or below T_{COOL} but above T_{COLD}, the battery charges with the JEITA-modified voltage and current values. These modified values, $V_{FAST-CHG\_JEITA}$ and $I_{FAST-CHG\_JEITA}$, are programmable through CHG_CV_JEITA[5:0] and CHG_CC_JEITA[5:0], respectively. These values are independently programmable from the nonmodified $V_{FAST-CHG}$ and $I_{FAST-CHG}$ values and can even be programmed to the same values if an automatic response to a warm or cool battery is not desired. The charger state machine enters JEITA-modified states while the battery temperature is outside of normal.
- If the battery temperature is either above T_{HOT} or below T_{COLD}, the charger follows the JEITA recommendation and pauses charging. The charger state machine enters battery temperature fault state while charging is paused due to extreme high or low temperatures.

The battery's temperature status is reflected by the THM_DTLS[2:0] status bitfield. A maskable interrupt (THM_I) signals a change in THM_DTLS[2:0]. Refer to the *Register Map* for more information. To completely disable the charger's automatic response to battery temperature, disable the feature by programming THM_EN = 0.

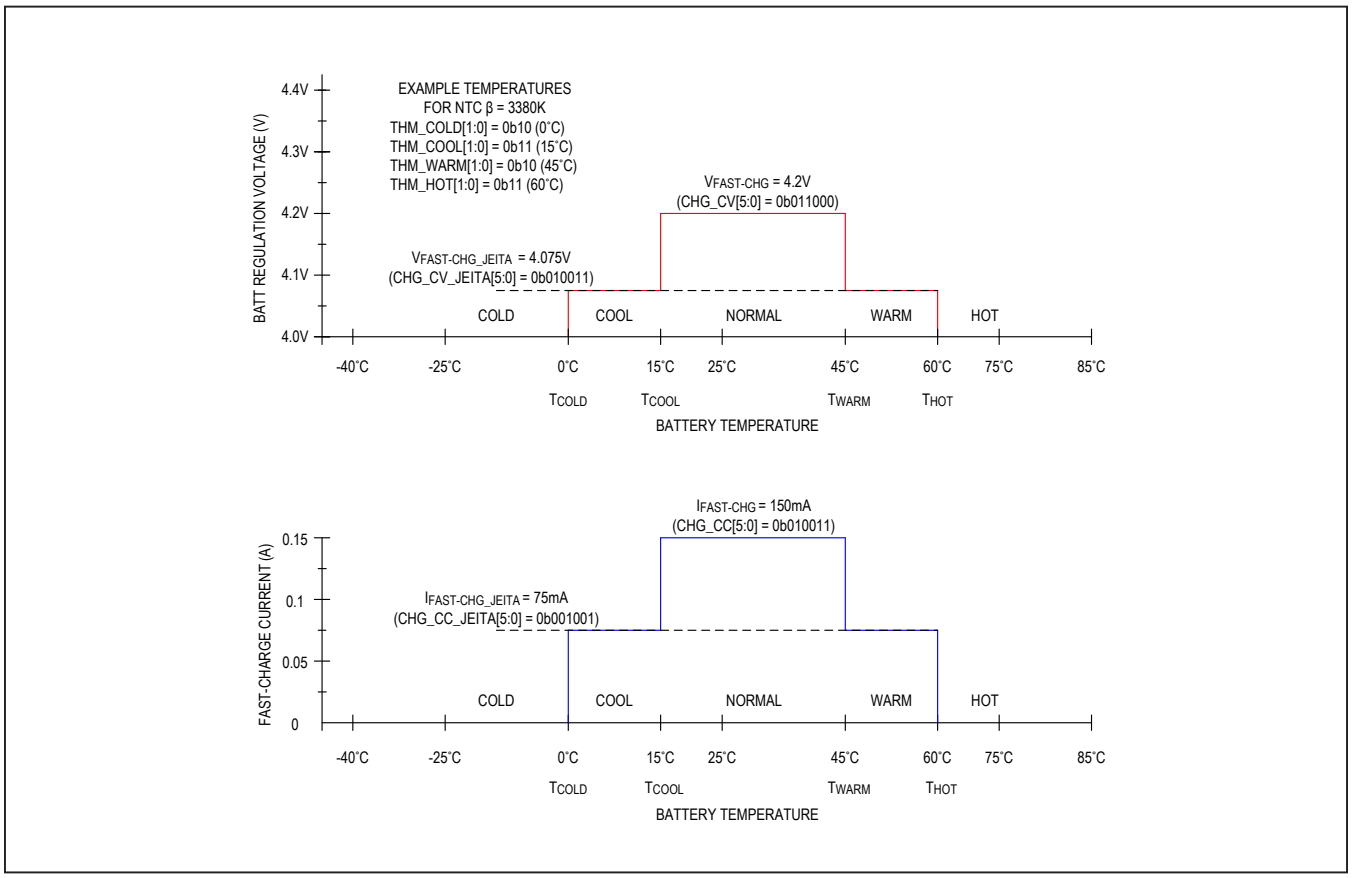


Figure 10. Safe-Charging Profile Example

The voltage thresholds corresponding to the JEITA temperature thresholds are independently programmable through THM_HOT[1:0], THM_WARM[1:0], THM_COOL[1:0], and THM_COLD[1:0]. Each threshold can be programmed to one of four voltage options spanning 15°C for an NTC beta of 3380K. See the *Configurable Temperature Thresholds* section and refer to the *Register Map* for more information.

Thermistor Bias

An external ADC can optionally perform conversions on the THM and TBIAS pins to measure the battery's temperature. An on-chip analog multiplexer is used to route these nodes to the AMUX pin. The operation of the analog multiplexer does not interfere with the charger's temperature monitoring comparators or the charger's automatic JEITA response. See the *Detailed Description—Analog Multiplexer* section for more information.

The NTC thermistor's bias source (TBIAS) follows the simple operation outlined as follows:

- If CHGIN is valid and the thermistor is enabled (THM_EN = 1), then the thermistor is biased so the charger can automatically respond to battery temperature changes.
- If the analog multiplexer is connecting THM or TBIAS to AMUX, then the thermistor is biased so an external ADC can perform a meaningful temperature conversion.

The AMUX pin is a buffered output. The operation of the analog multiplexer and external ADC does not collide with the function of the on-chip temperature monitors. Both functions can be used simultaneously with no ill effect.

Configurable Temperature Thresholds

Temperature thresholds for different NTC thermistor beta values are listed in Table 9. The largest possible programmable temperature range can be realized by using an NTC with a beta of 3380K. Using a larger beta compresses the temperature range. The trip voltage thresholds are programmable with the THM_HOT[1:0], THM_WARM[1:0], THM_COOL[1:0], and THM_COLD[1:0] bitfields. All possible programmable trip voltages are listed in Table 9.

These are theoretical values computed by a formula. Refer to the particular NTC's data sheet for more accurate measured data. In all cases, select the value of R_{BIAS} to be equal to the NTC's effective resistance at +25°C.

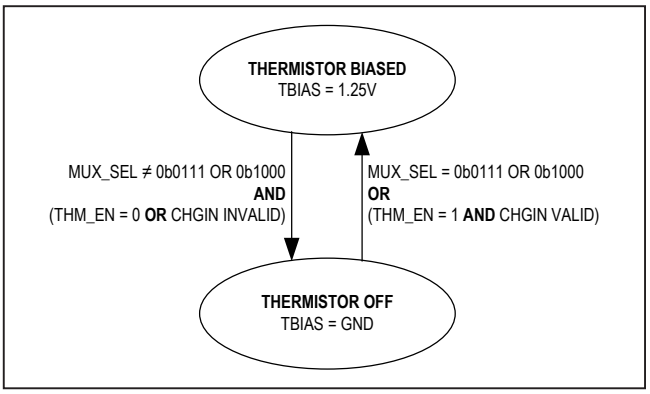


Figure 11. Thermistor Bias State Diagram

Table 9. Trip Temperatures vs. Trip Voltages for Different NTC β

TRIP VOLTAGE (V)	TRIP TEMPERATURES (°C)					
	3380K	3435K	3940K	4050K	4100K	4250K
1.024	-10.0	-9.5	-5.6	-4.8	-4.5	-3.5
0.976	-5.0	-4.6	-1.1	-0.5	-0.2	0.6
0.923	0.0	0.3	3.3	3.8	4.1	4.8
0.867	5.0	5.3	7.7	8.1	8.3	8.9
0.807	10.0	10.2	12.0	12.4	12.5	12.9
0.747	15.0	15.1	16.4	16.6	16.7	17.0
0.511	35.0	34.8	33.5	33.3	33.2	32.9
0.459	40.0	39.8	37.8	37.4	37.3	36.8
0.411	45.0	44.7	42.0	41.5	41.3	40.7
0.367	50.0	49.6	46.2	45.6	45.3	44.6
0.327	55.0	54.5	50.4	49.7	49.3	48.4
0.291	60.0	59.4	54.6	53.7	53.3	52.2

Thermistor Applications Information

Using Different Thermistor β

If an NTC with a beta larger than 3380K is used and the resulting available programmable temperature range is undesirably small, then two adjusting resistors can be used to expand the temperature range. R_S and R_P can be optionally added to the NTC thermistor circuit (shown in Figure 12) to expand the range of programmable temperature thresholds.

Select values for R_S and R_P based on the information shown in Table 10.

NTC Thermistor Selection

Popular NTC thermistor options are listed in Table 11.

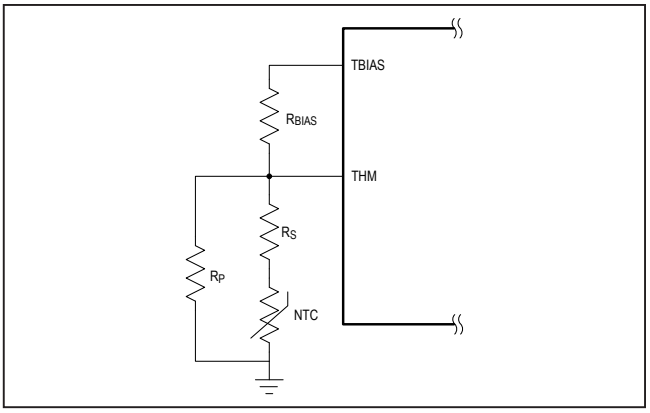


Figure 12. Thermistor Circuit with Adjusting Series and Parallel Resistors

Table 10. Example R_S and R_P Correcting Values for NTC β Above 3380K

PARAMETER	UNIT	DESIGN TARGET CASE	CASE 1		CASE 2		CASE 3	
NTC thermistor beta	K	3380	3940		4050		4250	
25°C NTC resistance	kΩ	10	10		47		100	
R_{BIAS}		10	10		47		100	
Adjusting parallel resistor, R_P		open	open	200	open	680	open	1300
Adjusting series resistor, R_S		short	short	0.62	short	3.3	short	9.1
R_{NTC} at 1.024V_{COLD} threshold		45.24	45.24	578.5	212.6	306.1	452.4	684.8
R_{NTC} at 0.867V_{COOL} threshold		22.61	22.61	248.8	106.3	122.7	226.1	264.7
R_{NTC} at 0.459V_{WARM} threshold		5.81	5.81	5.36	27.3	25.1	58.1	51.7
R_{NTC} at 0.291V_{HOT} threshold		3.04	3.04	2.46	14.3	112.7	30.4	22.0
T_{ACTUAL} at V_{COLD} (-10°C expected)	°C	-10.03	-5.56	-9.96	-4.82	-11.14	-3.55	-10.46
T_{ACTUAL} at V_{COOL} (5°C expected)		4.98	7.66	5.76	8.10	5.33	8.86	5.94
T_{ACTUAL} at V_{WARM} (40°C expected)		40.02	37.79	39.76	37.43	39.40	36.82	39.48
T_{ACTUAL} at V_{HOT} (60°C expected)		60.04	54.56	60.37	53.68	60.02	52.21	60.4

Table 11. NTC Thermistors

MANUFACTURER	PART#	B-CONSTANT (25°C/50°C)	R (Ω) AT 25°C	CASE SIZE
TDK	NTCG063JF223HTBX	3380K	22k	0201
Murata	NCP03XH103F05RL	3380K	10k	0201
Murata	NCP15XH103F03RC	3380K	10k	0402
TDK	NTCG103JX103DT1	3380K	10k	0402
Cantherm	CMFX3435103JNT	3435K	10k	0402
Murata	NCP15XV103J03RC	3900K	10k	0402
Panasonic	ERT-JZEP473J	4050K	47k	0201
Panasonic	ABNTC-0402-473J-4100F-T	4100K	47k	0402
Murata	NCP15WF104F03RC	4250K	100k	0402

Detailed Description—Analog Multiplexer

An external ADC can be used to measure the chip's various signals for general functionality or on-the-fly power monitoring. The MUX_SEL[3:0] bitfield controls the internal analog multiplexer responsible for connecting the proper channel to the AMUX pin. Each measurable signal is listed in Table 12 with its appropriate multiplexer channel.

The voltage on the AMUX pin is a buffered output that ranges from 0V to V_{FS} (1.25V, typ). The buffer has 50µA of quiescent current consumption and is only active when a channel is selected (MUX_SEL[3:0] ≠ 0b0000). Disable the buffer by programming MUX_SEL[3:0] to 0b0000 when not actively converting the voltage on AMUX. The AMUX output is high-impedance while MUX_SEL[3:0] is 0b0000.

Table 12 shows how to translate the voltage signal on the AMUX pin to the value of the parameter being measured. See the *Electrical Characteristics* table and refer to the *Register Map* for more details.

Table 12. AMUX Signal Transfer Functions

SIGNAL	MUX_SEL [3:0]	TRANSFER FUNCTION	FULL-SCALE SIGNAL MEANING (V_{AMUX} = 1.25V)	ZERO-SCALE SIGNAL MEANING (V_{AMUX} = 0V)
CHGIN pin voltage	0b0001	$V_{CHGIN} = \frac{V_{AMUX}}{G_{VCHGIN}}$	7.5V	0V
CHGIN pin current	0b0010	$I_{CHGIN} = \frac{V_{AMUX}}{G_{ICHGIN}}$	0.475A	0A
BATT pin voltage	0b0011	$I_{BATT} = \frac{V_{AMUX}}{G_{VBATT}}$	4.6V	0V
BATT pin charging current	0b0100	$I_{BATT(CHG)} = \frac{V_{AMUX}}{V_{FS}} \times I_{FAST-CHG}$	100% of $I_{FAST-CHG}$ (CHG_CC[5:0])	0% of $I_{FAST-CHG}$
BATT pin discharge current	0b0101	$I_{BATT(DISCHG)} = \frac{(V_{AMUX} - V_{NULL})}{(V_{FS} - V_{NULL})} \times I_{DISCHG-SCALE}$	100% of $I_{DISCHG-SCALE}$ (IMON_DISCHG_SCALE[3:0])	0% of $I_{DISCHG-SCALE}$
BATT pin discharge current NULL	0b0110	$V_{NULL} = V_{AMUX}$	1.25V	0V
THM pin voltage	0b0111	$V_{THM} = V_{AMUX}$	1.25V	0V
TBIAS pin voltage	0b1000	$V_{TBIAS} = V_{AMUX}$	1.25V	0V
AGND pin voltage*	0b1001	$V_{AGND} = V_{AMUX}$	1.25V	0V
SYS pin voltage	0b1010	$V_{SYS} = \frac{V_{AMUX}}{G_{VSYS}}$	4.8V	0V

**AGND pin voltage is accessed through a 100Ω (typ) pulldown resistor.*

Measuring Battery Current

It is possible to sample the current in the BATT pin at any time or in any mode with an external ADC. For improved accuracy, the analog circuitry used for monitoring battery discharge current is different from the circuitry monitoring battery charge current. Table 13 outlines how to determine the direction of battery current.

Method for Measuring Discharging Current

- Program the multiplexer to switch to the discharge NULL measurement by changing MUX_SEL[3:0] to 0b0110. A NULL conversion must always be performed first to cancel offsets.
- Wait the appropriate channel switching time (0.3µs, typ).
- Convert the voltage on the AMUX pin and store as V_{NULL}.
- Program the multiplexer to switch to the battery discharge current measurement by changing MUX_SEL[3:0] to 0b0101. A nonnulling conversion should be done immediately after a NULL conversion.
- Wait the appropriate channel switching time (0.3µs, typ).
- Convert the voltage on AMUX pin and use the following transfer function to determine the discharge current:

$$I_{BATT(DISCHG)} = \frac{(V_{AMUX} - V_{NULL})}{(V_{FS} - V_{NULL})} \times I_{DISCHG\text{-}SCALE*}$$

V_{FS} is 1.25V typical. $I_{DISCHG\text{-}SCALE}$ is programmable through IMON_DISCHG_SCALE[3:0]. The default value is 300mA. If smaller currents are anticipated, then $I_{DISCHG\text{-}SCALE}$ can be reduced for improved measurement accuracy.

Method for Measuring Charging Current

- Program the multiplexer to switch to the charge current measurement by changing MUX_SEL[3:0] to 0b0100.
- Wait the appropriate channel switching time (0.3µs, typ).
- Convert the voltage on the AMUX pin and use the following transfer function to determine charging current.

$$I_{BATT(DISCHG)} = \frac{V_{AMUX}}{V_{FS}} \times I_{FAST-CHG}$$

V_{FS} is 1.25V typical. $I_{FAST\text{-}CHG}$ the charger's fast-charge constant-current setting and is programmable through CHG_CC[5:0].

Table 13. Battery Current Direction Decode

MEASUREMENT	CHARGING OR DISCHARGING INDICATORS		
	CHG BIT	CHG_DTLS[3:0]	CHGIN_DTLS[1:0]
Discharging Battery Current (Positive Battery Terminal Sourcing Current)	*Don't care*	*Don't care*	0b00 0b01 0b10
Charging Battery Current (Positive Battery Terminal Sinking Current)	1	0b0001 - 0b0111	0b11

Detailed Description—Linear Regulator

The IC integrates a 150mA PMOS low-dropout linear voltage regulator (LDO). Output voltage is programmable through I2C between 0.8V and 3.975V in 25mV steps using the LDO_VREG[6:0] bitfield. The LDO features a low-I_Q (1.5µA, typ) low-power mode which reduces system idle power consumption. The LDO input (INLDO) can be connected directly to SYS or supplied by an external step-down regulator for increased power efficiency. A 100Ω (typ) active-discharge resistor is available to quickly discharge the LDO's output after the regulator has been disabled.

LDO Enable Control

Force the LDO on by writing LDO_EN[1:0] to 0b01 with I2C. The on/off controller begins the LDO power-up sequence when this bit combination is set.

Disable the LDO (force off) by writing LDO_EN[1:0] to 0b00 with I2C. This bit combination causes the LDO power-down sequence to happen.

Setting the bits in LDO_EN[1:0] to 0b10 causes the LDO to activate due to hardware inputs (nENLDO or CHGIN) or special software commands. This bit combination causes the on/off controller to begin the LDO power-up sequence when:

- nENLDO is asserted for t_{DBNC_nENLDO} (LDO_WAKE internal flag set)
- CHGIN is inserted and debounced valid (CHGIN_DTLS[1:0] = 0b11)
- Software caused a cold reset (SFT_CTRL[1:0] = 0b01) and the reset actions are finished and LDO_EN[1:0] is factory-programmed to 0b10 (SFT_WAKE internal flag set)

The LDO deactivates regardless of LDO_EN[1:0] when any of the following conditions are true:

- SYS undervoltage-lockout
- SYS overvoltage-lockout
- Chip over-temperature lockout
- Software causes a power-off (SFT_CTRL[1:0] = 0b10)
- Software causes a reset (SFT_CTRL[1:0] = 0b01)
- Software requests factory-ship mode (SFT_CTRL[1:0] = 0b11)
- The watchdog timer is enabled and expires (WDT_EXP internal flag set)
- Manual reset occurs (MAN_RST internal flag set)

Consult the *On/Off Controller* section and Table 1 of the data sheet for more details.

The reset value of the bits in LDO_EN[1:0] is factory-programmable. Consult the *Ordering Information* for details.

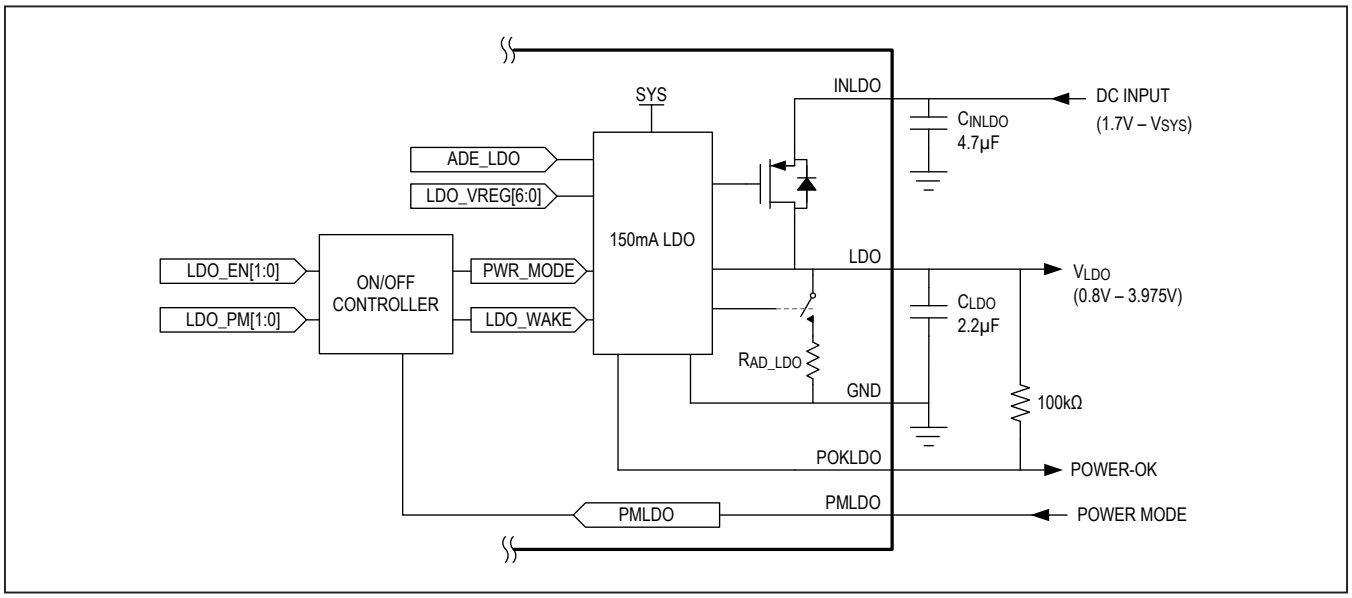


Figure 13. LDO Simplified Block Diagram

LDO Power Mode (PMLDO)

Program the LDO_PM[1:0] bitfield to 0b00 to configure the LDO in low-power mode. Program 0b01 to configure the LDO for normal mode. Program 0b10 or 0b11 to enable hardware control of the power mode through the PMLDO pin. Code 0b10 enables normal mode when PMLDO is logic-high. Code 0b11 enables normal mode when PMLDO is logic-low. If the MSB of LDO_PM[1:0] is set, then always drive the PMLDO pin to prevent mode chatter. If the MSB is not set, then the PMLDO pin is a *don't care*. See Table 14 for a truth table of this behavior.

The LDO can support loads of 150mA with an $I_{INLDO-Q}$ of 12µA ($1.8V_{LDO}$) in normal mode. Loads of 5mA with a reduced $I_{INLDO-Q}$ of 1.5µA ($1.8V_{LDO}$) are supported in low-power mode.

A system similar to the block diagram in Figure 14 can dynamically manage the LDO's power mode and minimize I_Q consumption. When the low-power microcontroller (U2) disables the dynamic load (U3) then the PMLDO pin is brought low indicating that the LDO goes to low-power mode. When the host enables the load, then the PMLDO pin becomes high and the LDO enters normal power mode to support the current demand of the dynamic load.

LDO Power-OK Output (POKLDO)

The IC features an open-drain LDO Power-OK (POKLDO) output to monitor the LDO output voltage. POKLDO requires an external pullup resistor to a voltage equal to or less than V_{SYS}. This node goes high when V_{LDO} rises above V_{POKLDO_R} (typically 87.5% of programmed $V_{LDO-REG}$) and goes low when V_{LDO} falls below V_{POKLDO_F} (typically 84% of $V_{LDO-REG}$).

POKLDO is blanked by the on/off controller during the LDO power-up and power-down sequences (Figure 2). The blanking signal holds POKLDO low regardless of V_{LDO}.

Table 14. LDO Power Mode Truth Table

PMLDO (PIN)	LDO_PM[1:0] (BITFIELD)	LDO POWER MODE
X	00	Low-Power
X	01	Normal
0	10	Low-Power
1	10	Normal
0	11	Normal
1	11	Low-Power

LDO Applications Information

Input/Output Capacitor Selection

Bypass INLDO to GND with a minimum 10µF ceramic capacitor. If INLDO is connected to SYS, then a single 22µF bypass capacitor to GND can be used for both pins.

Bypass the LDO output to GND with a minimum 2.2µF ceramic capacitor that maintains 1.1µF of effective capacitance at bias. Larger values of LDO capacitance improve decoupling but increase inrush current during LDO startup. Refer to *Startup Rate and Inrush Current* for guidance on managing startup inrush current.

Ceramic capacitors with X5R or X7R dielectric are highly recommended due to their small size, low ESR, and small temperature coefficients. All ceramic capacitors derate with DC bias voltage (effective capacitance goes down as DC bias goes up). Generally, small case size capacitors derate heavily compared to larger case sizes (0603 case size performs better than 0402). Consider the effective capacitance value carefully by consulting the manufacturer's data sheet.

Startup Rate and Inrush Current

The startup ramp rate of the LDO can be controlled using the following equation:

$$\frac{\Delta V_{LDO}}{\Delta t} = \frac{I_{LDO-LIM}}{8 \times C_{LDO}}$$

where $I_{LDO-LIM}$ is the output current limit of the LDO in normal mode (300mA, typ) and C_{LDO} is the LDO output capacitor (2.2µF minimum required).

Applications that are sensitive to inrush current from the battery should select an LDO output capacitor as close to the minimum stability requirement as possible (2.2µF), while at the same time, maximizing the INLDO and SYS capacitance to filter any large current spikes from BATT.

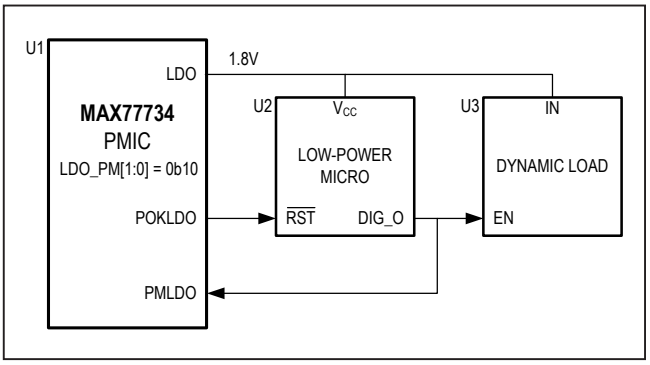


Figure 14. Dynamic LDO Power Mode Control Idea

PCB Layout Guidelines

Careful printed circuit board (PCB) layout is necessary to achieve optimal performance. Follow these guidelines when designing the PCB:

1) Place decoupling components (C_{CHGIN}, C_{SYS}, C_{BATT}, C_{INLDO}, C_{LDO}) close to the IC.
2) A single decoupling capacitor can be used to bypass both SYS and INLDO to GND. Use a short and wide copper flood to connect SYS and INLDO.
3) If INLDO has a different power source (other than SYS), then a separate INLDO decoupling capacitor (not drawn in Figure 15) is recommended.
4) The value of C_{INLDO} should be larger than C_{LDO}. If C_{LDO} = 2.2µF, then choose C_{INLDO} = 4.7µF or greater.

Figure 15 shows an example PCB top-metal layout with 0.2mm component-to-component spacing.

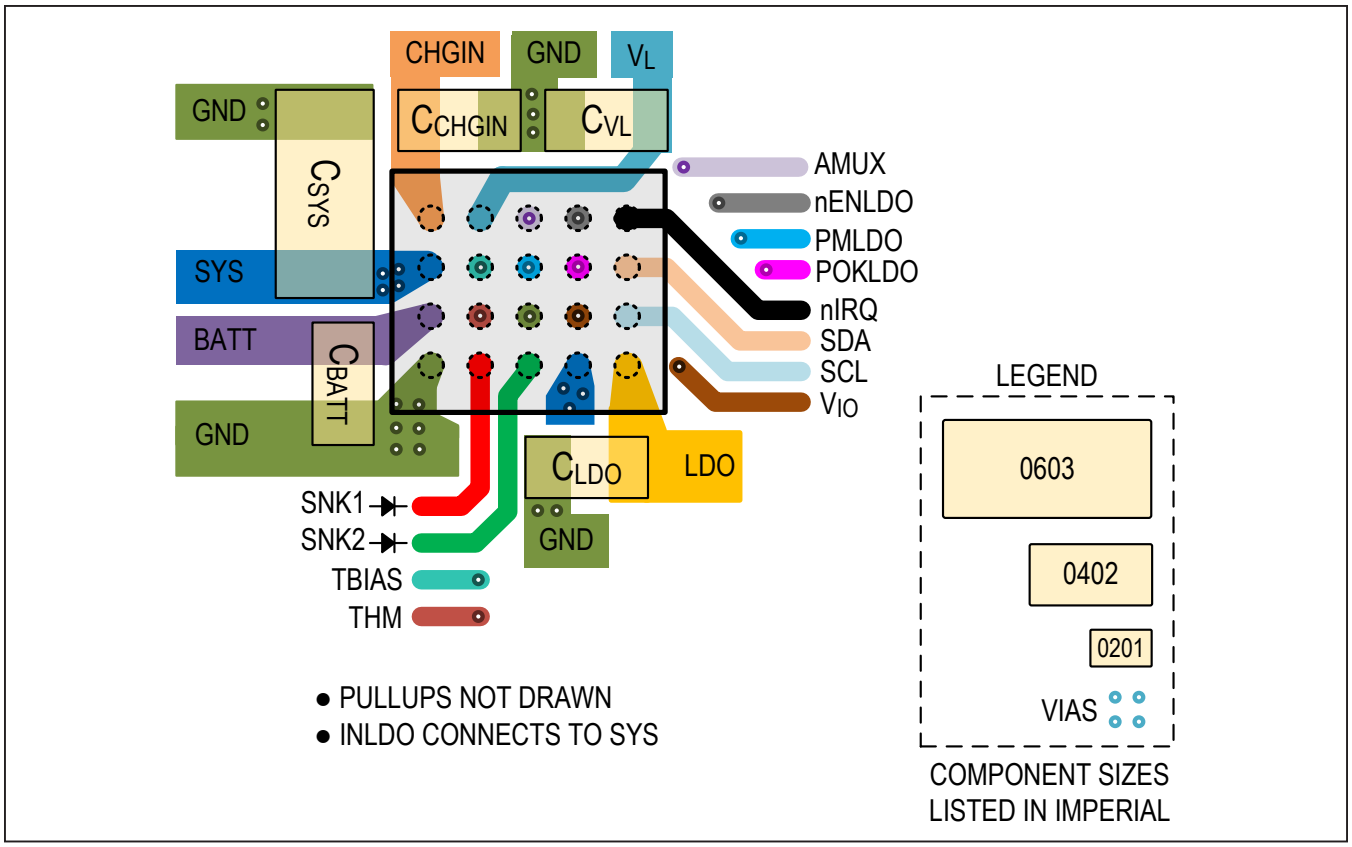


Figure 15. PCB Top-Metal and Component Layout Example

Detailed Description—Dual-Channel Current Sink Driver

The IC has a dual-channel current sink driver designed to drive LEDs in portable devices (see Figure 16). The circuit can also be used as a general-purpose current sink driver for other applications. The driver's on-time and frequency are independently programmable for each output to achieve a desired blink pattern. Alternatively, the LEDs can be continuously on (not blinking). The blink period is programmable from 0.5s to 8s, with an on-time duty cycle from 6.25% to 100%.

Detailed Description—I²C Serial Interface

The IC features a revision 3.0 I²C-compatible, 2-wire serial interface consisting of a bidirectional serial data line (SDA) and a serial clock line (SCL). The IC is a slave-only device that relies on an external bus master to generate SCL. SCL clock rates from 0Hz to 3.4MHz are supported. I²C is an open-drain bus and therefore SDA and SCL require pullups.

The device's I²C communication controller implements 7-bit slave addressing. An I²C bus master initiates communication with the slave by issuing a START condition followed by the slave address. The slave address is factory programmable to one of two options (Table 15). All slave addresses not mentioned in Table 15 are not acknowledged.

The IC uses 8-bit registers with 8-bit register addressing. They support standard communication protocols: (1) Writing to a single register (2) Writing to multiple sequential registers with an automatically incrementing data pointer (3) Reading from a single register (4) Reading from multiple sequential registers with an automatically incrementing data pointer. For additional information on the I²C protocols, refer to the **MAX77734 I²C Implementer's Guide** and/or the I²C specification that is freely available on the internet.

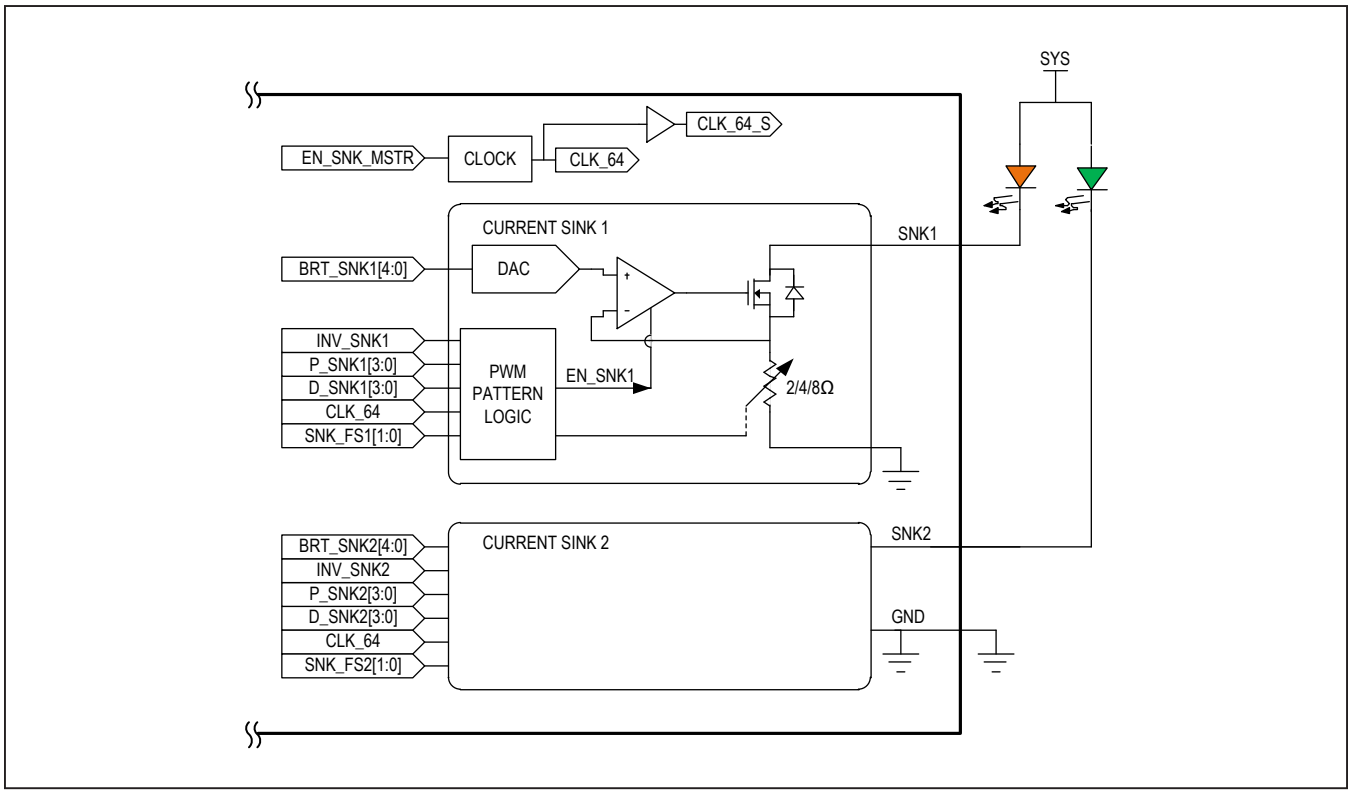


Figure 16. LED Current Sinks Functional Block Diagram

Table 15. I²C Slave Address Options

ADDRESS	7-BIT SLAVE ADDRESS	8-BIT WRITE ADDRESS	8-BIT READ ADDRESS
Main Address (ADDR = 1)*	0x48, 0b 100 1000	0x90, 0b 1001 0000	0x91, 0b 1001 0001
Main Address (ADDR = 0)*	0x40, 0b 100 0000	0x80, 0b 1000 0000	0x81, 0b 1000 0001
Test Mode**	0x49, 0b 100 1001	0x92, 0b 1001 0010	0x93, 0b 1001 0011

**Perform all reads and writes on the Main Address. ADDR is a factory one-time programmable (OTP) option, allowing for address changes in the event of a bus conflict. Contact Maxim for more information.*

***When test mode is unlocked, the additional address is acknowledged. Test mode details are confidential. If possible, leave the test mode address unallocated to allow for the rare event that debugging needs to be performed in cooperation with Maxim.*

Register Map

MAX77734

ADDRESS	NAME	MSB							LSB
GLOBAL CONFIGURATION									
0x00	INT_GLBL[7:0]	RSVD	POKLDO_I	TJAL2_R	TJAL1_R	nENLDO_R	nENLDO_F	RSVD	RSVD
0x01	INT_CHG[7:0]	RSVD	SYS_CNFG_I	SYS_CTRL_I	CHGIN_CTRL_I	TJ_REG_I	CHGIN_I	CHG_I	THM_I
0x02	STAT_CHG_A[7:0]	RSVD	VCHGIN_MIN_STAT	ICHGIN_LIM_STAT	VSYS_MIN_STAT	TJ_REG_STAT	THM_DTLS[2:0]		
0x03	STAT_CHG_B[7:0]	CHG_DTLS[3:0]				CHGIN_DTLS[1:0]		CHG	TIME_SUS
0x04	ERCFLAG[7:0]	WDT_RST	WDT_OFF	SFT_RST	SFT_OFF	MRST	SYSUVLO	SYS-OVLO	TOVLD
0x05	STAT_GLBL[7:0]	DIDM[1:0]		POKLDO_S	TJAL2_S	TJAL1_S	STAT_EN-LDO	BOK	STAT_IRQ
0x06	INTM_GLBL[7:0]	RSVD	POKLDO_IM	TJAL2_RM	TJAL1_RM	nENLDO_RM	nENLDO_FM	RSVD	RSVD
0x07	INT_M_CHG[7:0]	RSVD	SYS_CNFG_M	SYS_CTRL_M	CHGIN_CTRL_M	TJ_REG_M	CHGIN_M	CHG_M	THM_M
0x08	CNFG_GLBL[7:0]	PU_DIS	T_MRST	BIAS_LPM	BIAS_REQ	nENLDO_MODE	DB_nEN-LDO	SFT_CTRL[1:0]	
0x09	CID[7:0]	—	—	—	—	CID[3:0]			
0x0A	CNFG_WDT[7:0]	RSVD	RSVD	WDT_PER[1:0]		WDT_MODE	WDT_CLR	WDT_EN	WDT_LOCK

MAX77734 (continued)

ADDRESS	NAME	MSB							LSB
CHARGER CONFIGURATION									
0x20	CNFG_CHG_A[7:0]	THM_HOT[1:0]		THM_WARM[1:0]		THM_COOL[1:0]		THM_COLD[1:0]	
0x21	CNFG_CHG_B[7:0]	VCHGIN_MIN[2:0]			ICHGIN_LIM[2:0]			I_PQ	CHG_EN
0x22	CNFG_CHG_C[7:0]	CHG_PQ[2:0]			I_TERM[1:0]		T_TOPOFF[2:0]		
0x23	CNFG_CHG_D[7:0]	TJ_REG[2:0]			VSYS_REG[4:0]				
0x24	CNFG_CHG_E[7:0]	CHG_CC[5:0]						T_FAST_CHG[1:0]	
0x25	CNFG_CHG_F[7:0]	CHG_CC_JEITA[5:0]						THM_EN	RSVD
0x26	CNFG_CHG_G[7:0]	CHG_CV[5:0]						USBS	RSVD
0x27	CNFG_CHG_H[7:0]	CHG_CV_JEITA[5:0]						RSVD	RSVD
0x28	CNFG_CHG_I[7:0]	IMON_DISCHG_SCALE[3:0]				MUX_SEL[3:0]			
LDO CONFIGURATION									
0x30	CNFG_LDO_A[7:0]	ADE_LDO	LDO_VREG[6:0]						
0x31	CNFG_LDO_B[7:0]					LDO_PM[1:0]		LDO_EN[1:0]	
CURRENT SINKS CONFIGURATION									
0x40	CNFG_SNK1_A[7:0]	SNK_FS1[1:0]		INV_SNK1	BRT_SNK1[4:0]				
0x41	CNFG_SNK1_B[7:0]	P_SNK1[3:0]				D_SNK1[3:0]			
0x42	CNFG_SNK2_A[7:0]	SNK_FS2[1:0]		INV_SNK2	BRT_SNK2[4:0]				
0x43	CNFG_SNK2_B[7:0]	P_SNK2[3:0]				D_SNK2[3:0]			
0x44	CNFG_SNK_TOP[7:0]	—	—	—	—	—	—	CLK_64_S	EN_SNK_MSTR

INT_GLBL (0x00)

BIT	7	6	5	4	3	2	1	0
Field	RSVD	POKLDO_I	TJAL2_R	TJAL1_R	nENLDO_R	nENLDO_F	RSVD	RSVD
Reset	0b0	0b0	0b0	0b0	0b0	0b0	0b0	0b0
Access Type	Read Clears All	Read Clears All	Read Clears All	Read Clears All	Read Clears All	Read Clears All	Read Clears All	Read Clears All

BITFIELD	BITS	RESET-TYPE	DESCRIPTION	DECODE
RSVD	7	SYSRST	Reserved. Reads back 0.	N/A
POKLDO_I	6	SYSRST	POKLDO Interrupt	0 = POKLDO_S has not changed since the last time this bit was read. 1 = POKLDO_S has changed since the last time this bit ws read.
TJAL2_R	5	SYSRST	Thermal Alarm 2 Rising Interrupt	0 = The junction temperature has not risen above T_{JAL2} since the last time this bit was read. 1 = The junction temperature has risen above T_{JAL2} since the last time this bit was read.
TJAL1_R	4	SYSRST	Thermal Alarm 1 Rising Interrupt	0 = The junction temperature has not risen above T_{JAL1} since the last time this bit was read. 1 = The junction temperature has risen above T_{JAL1} since the last time this bit was read.
nENLDO_R	3	SYSRST	nENLDO Rising Interrupt	0 = No nENLDO rising edges have occurred since the last time this bit was read. 1 = A nENLDO rising edge as occurred since the last time this bit was read.
nENLDO_F	2	SYSRST	nENLDO Falling Interrupt	0 = No nENLDO falling edges have occurred since the last time this bit was read. 1 = A nENLDO falling edge as occurred since the last time this bit was read.
RSVD	1	SYSRST	Reserved. Reads back 0.	N/A
RSVD	0	SYSRST	Reserved. Reads back 0.	N/A

INT_CHG (0x01)

BIT	7	6	5	4	3	2	1	0
Field	RSVD	SYS_ CNFG_I	SYS_ CTRL_I	CHGIN_ CTRL_I	TJ_REG_I	CHGIN_I	CHG_I	THM_I
Reset	0b1	0b0	0b0	0b0	0b0	0b0	0b0	0b0
Access Type	Read Clears All	Read Clears All	Read Clears All	Read Clears All	Read Clears All	Read Clears All	Read Clears All	Read Clears All

BITFIELD	BITS	RESET-TYPE	DESCRIPTION	DECODE
RSVD	7	SYSRST	Reserved. Reads back 0.	N/A
SYS_CNFG_I	6	SYSRST	System Voltage Configuration Error Interrupt. Goes high when $V_{SYS-REG}$ and $V_{FAST-CHG}$ are programmed too close to each other. Reads back 1 when the bit combination in CHG_CV[5:0] or CHG_CV_JEITA[5:0] has been forced to change (reduce) to ensure $V_{SYS-REG} = V_{FAST-CHG} + 200mV$.	0 = No configuration error since the last time this bit was read. 1 = The bits in CHG_CV[5:0] have been forced to change to ensure $V_{SYS-REG}$ is 200mV above $V_{FAST-CHG}$.
SYS_CTRL_I	5	SYSRST	Minimum System Voltage Regulation Loop Related Interrupt. Signals a change in VSYS_MIN_STAT.	0 = VSYS_MIN_STAT has not changed since the last time this bit was read. 1 = VSYS_MIN_STAT has changed.
CHGIN_ CTRL_I	4	SYSRST	CHGIN Control-Loop Related Interrupt. Signals a change in the minimum input voltage regulation loop (VCHGIN_MIN_ STAT) or the input current-limit loop (ICHGIN_LIM_STAT).	0 = Neither VCHGIN_MIN_STAT nor ICHGIN_LIM_STAT has changed since the last time this bit was read. 1 = VCHGIN_MIN_STAT or ICHGIN_LIM_STAT has changed.
TJ_REG_I	3	SYSRST	Die Junction Temperature Regulation Interrupt. Signals a change in the die temperature regulation loop (TJ_REG_STAT).	0 = TJ_REG_STAT has not changed since the last time this bit was read. 1 = TJ_REG_STAT has changed.
CHGIN_I	2	SYSRST	CHGIN Related Interrupt. Signals a change in CHGIN_DTLS[1:0].	0 = The bits in CHGIN_DTLS[1:0] have not changed since the last time this bit was read. 1 = The bits in CHGIN_DTLS[1:0] have changed.
CHG_I	1	SYSRST	Charger Related Interrupt. Signals a change in CHG_DTLS[3:0].	0 = The bits in CHG_DTLS[3:0] have not changed since the last time this bit was read. 1 = The bits in CHG_DTLS[3:0] have changed.
THM_I	0	SYSRST	Thermistor Related Interrupt. Signals a change in THM_DTLS[2:0].	0 = The bits in THM_DTLS[2:0] have not changed since the last time this bit was read. 1 = The bits in THM_DTLS[2:0] have changed.

STAT_CHG_A (0x02)

BIT	7	6	5	4	3	2	1	0
Field	RSVD	VCHGIN_ MIN_STAT	ICHGIN_ LIM_STAT	VSYS_ MIN_STAT	TJ_REG_ STAT	THM_DTLS[2:0]		
Reset	0b0	0b0	0b0	0b0	0b0	0b000		
Access Type	Read Only	Read Only	Read Only	Read Only	Read Only	Read Only		

BITFIELD	BITS	RESET-TYPE	DESCRIPTION	DECODE
RSVD	7	CHGPOK	Reserved. Reads back 0.	N/A
VCHGIN_ MIN_STAT	6	CHGPOK	Minimum Input Voltage Regulation Loop Status	0 = The minimum CHGIN voltage regulation loop has not engaged. 1 = The loop has engaged to reduce CHGIN current to regulate $V_{CHGIN} \geq V_{CHGIN-MIN}$.
ICHGIN_ LIM_STAT	5	CHGPOK	Input Current-Limit Loop Status	0 = The CHGIN current-limit loop is not engaged. 1 = The loop has engaged to regulate $I_{CHGIN} \leq I_{CHGIN-LIM}$
VSYS_ MIN_STAT	4	CHGPOK	Minimum System Voltage Regulation Loop Status	0 = The minimum system voltage regulation loop is not engaged. 1 = The loop has engaged to regulate $V_{SYS} \geq V_{SYS-MIN}$.
TJ_REG_ STAT	3	CHGPOK	Maximum Junction Temperature Regulation Loop Status	0 = The maximum junction temperature regulation loop is not engaged. 1 = The loop has engaged and is reducing charge current to limit die temperature.
THM_DTLS	2:0	CHGPOK	Battery Temperature Details	0b000 = Thermistor is diabled (THM_EN = 0). 0b001 = Battery is cold as programmed by THM_COLD[1:0]. 0b010 = Battery is cool as programmed by THM_COOL[1:0]. 0b011 = Battery is warm as programmed by THM_WARM[1:0]. 0b100 = Battery is hot as programmed by THM_HOT[1:0]. 0b101 = Battery temperature is normal as programmed by CNFG_CHG_A register. 0b110-0b111 = Reserved.

STAT_CHG_B (0x03)

BIT	7	6	5	4	3	2	1	0
Field	CHG_DTLS[3:0]				CHGIN_DTLS[1:0]		CHG	TIME_SUS
Reset	0b0000				0b00		0b0	0b0
Access Type	Read Only				Read Only		Read Only	Read Only

BITFIELD	BITS	RESET-TYPE	DESCRIPTION	DECODE
CHG_DTLS	7:4	CHGPOK	Charger Details. Indicates the current state of the charger.	0b0000 = Charger off. 0b0001 = Prequalification mode. 0b0010 = Fast-charge constant-current (CC) mode. 0b0011 = JEITA-modified fast-charge constant-current mode. 0b0100 = Fast-charge constant-voltage (CV) mode. 0b0101 = JEITA-modified fast-charge constant-voltage mode. 0b0110 = Top-off mode. 0b0111 = JEITA-modified top-off mode. 0b1000 = Done. 0b1001 = JEITA-modified done (done was entered through the JEITA-modified fast-charge states). 0b1010 = Prequalification timer fault. 0b1011 = Fast-charge timer fault. 0b1100 = Battery temperature fault. 0b1101-0b1111 = Reserved.
CHGIN_ DTLS	3:2	CHGPOK	CHGIN Status Details	0b00 = CHGIN voltage is below the UVLO threshold (V_{CHGIN_UVLO}) or USB suspended (USBS = 1). 0b01 = CHGIN voltage is above the OVP threshold (V_{CHGIN_OVP}). 0b10 = The CHGIN input is being debounced (no power drawn from CHGIN during debounce). 0b11 = The CHGIN input is debounced and valid.
CHG	1	CHGPOK	Quick Charger Status	0 = Charging is not happening. 1 = Charging is happening.
TIME_SUS	0	CHGPOK	Time Suspend Indicator. The fast-charge safety timer susepnds if any of the following are true: charge current has dropped below 20% of $I_{FAST-CHG}$ while the charger state machine is in FAST CHARGE (CC) state, the charger is in suppliment mode, or the charger state machine is in BATTERY TEMPERATURE FAULT mode.	0 = Charger's timers are not active or not suspended. 1 = Charger's active timer suspended.

ERCFLAG (0x04)

BIT	7	6	5	4	3	2	1	0
Field	WDT_RST	WDT_OFF	SFT_RST	SFT_OFF	MRST	SYSUVLO	SYSOVLO	TOVLD
Reset	0b0	0b0	0b0	0b0	0b0	0b0	0b0	0b0
Access Type	Read Clears All	Read Clears All	Read Clears All	Read Clears All	Read Clears All	Read Clears All	Read Clears All	Read Clears All

BITFIELD	BITS	RESET-TYPE	DESCRIPTION	DECODE
WDT_RST	7	SYSPOR	Watchdog Timer Reset Flag. This bit sets when the watchdog timer expires and causes a power-reset (WTD_EXP = 1 and WTD_MODE = 1).	0 = Watchdog timer has not caused a power-reset since the last time this bit was read. 1 = Watchdog timer has expired and caused a power-reset since the last time this bit was read.
WDT_OFF	6	SYSPOR	Watchdog Timer OFF Flag. This bit sets when the watchdog timer expires and causes a power-off (WDT_EXP = 1 and WDT_MODE = 0).	0 = Watchdog timer has not caused a power-off since the last time this bit was read. 1 = Watchdog timer has expired and caused a power-off since the last time this bit was read.
SFT_RST	5	SYSPOR	Software Reset Flag. This bit sets when an I²C write causes a power-reset (SFT_RST[1:0] = 0b01).	0 = No software caused power-reset since the last time this bit was read. 1 = Software has caused a power-reset since the last time this bit was read.
SFT_OFF	4	SYSPOR	Software OFF Flag. This bit sets when an I²C write causes a power-off (SFT_CTRL[1:0] = 0b10).	0 = No software caused power-off since the last time this bit was read. 1 = Software has caused a power-off since the last time this bit was read.
MRST	3	SYSPOR	Manual Reset Timer Flag. This bit sets when a manual reset event (MAN_RST = 1) causes a power reset.	0 = Manual reset has not caused power-reset since the last time this bit was read. 1 = Manual reset has caused power-reset since the last time this bit ws read.
SYSUVLO	2	SYSPOR	SYS Domain Undervoltage-Lockout Flag. This bit sets when the SYS domain voltage falls below $V_{SYSUVLO}$ and causes a power-off.	0 = SYS domain undervoltage lockout has not caused a power-off since the last time this bit was read. 1 = SYS domain undervoltage lockout has caused a power-off since the last time this bit was read.
SYSOVLO	1	SYSPOR	SYS Domain Overvoltage-Lockout Flag. This bit sets when the SYS domain voltage rises above $V_{SYSOVLO}$ and causes a power-off.	0 = SYS domain overvoltage lockout has not caused a power-off since the last time this bit was read. 1 = SYS domain overvoltage lockout has caused a power-off since the last time this bit was read.
TOVLD	0	SYSPOR	Thermal Overload Flag. This bit sets when the junction temperature exceeds 165°C and causes a power-off.	0 = Thermal overload has not caused a power-off since the last time this bit was read. 1 = Thermal overload has caused a power-off since the last time this bit was read.

STAT_GLBL (0x05)

BIT	7	6	5	4	3	2	1	0
Field	DIDM[1:0]		POKLDO_S	TJAL2_S	TJAL1_S	STAT_ ENLDO	BOK	STAT_IRQ
Reset	0b10		0b0	0b0	0b0	0b0	0b0	0b0
Access Type	Read Only		Read Only	Read Only	Read Only	Read Only	Read Only	Read Only

BITFIELD	BITS	RESET-TYPE	DESCRIPTION	DECODE
DIDM	7:6	SYSRST	Device Identification Bits for Metal Options	0b00 = Reserved for future use. 0b01 = Reserved for future use. 0b10 = MAX77734 0b11 = Reserved for future use.
POKLDO_S	5	SYSRST	LDO Power-OK Status. Continuous software mirror of the POKLDO pin.	0 = POKLDO is low 1 = POKLDO is high (Hi-Z)
TJAL2_S	4	SYSRST	Thermal Alarm 2 Status	0 = The junction temperature is less than T_{JAL2} 1 = The junction temperature is greater than T_{JAL2}
TJAL1_S	3	SYSRST	Thermal Alarm 1 Status	0 = The junction temperature is less than T_{JAL1} 1 = The junction temperature is greater than T_{JAL1}
STAT_ ENLDO	2	SYSRST	Debounced Status for the nENLDO input	0 = nENLDO is not asserted (logic high) 1 = nENLDO is asserted (logic low)
BOK	1	SYSRST	System Bias OK Status Bit	0 = Bias not ready or not enabled. 1 = Bias enabled and ready.
STAT_IRQ	0	SYSRST	Interrupt Status. Continuous *inverted* software mirror of the nIRQ pin as if all interrupts were unmasked.	0 = No interrupts pending. nIRQ would be high if all interrupts were unmasked. 1 = Interrupts pending. nIRQ would be low if all interrupts were unmasked.

INTM_GLBL (0x06)

BIT	7	6	5	4	3	2	1	0
Field	RSVD	POKLDO_IM	TJAL2_RM	TJAL1_RM	nENLDO_RM	nENLDO_FM	RSVD	RSVD
Reset	0b0	0b1	0b1	0b1	0b1	0b1	0b0	0b0
Access Type	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	RESET-TYPE	DESCRIPTION	DECODE
RSVD	7	SYSRST	Reserved. Bit is a *don't care.*	N/A
POKLDO_IM	6	SYSRST	POKLDO_I Interrupt Mask. Setting this bit prevents the POKLDO_I bit from causing hardware interrupts.	0 = POKLDO_I is not masked. 1 = POKLDO_I is masked.
TJAL2_RM	5	SYSRST	Thermal Alarm 2 Rising Interrupt Mask. Setting this bit prevents the TJAL2_R bit from causing hardware interrupts.	0 = TJAL2_R is not masked. 1 = TJAL2_R is masked.
TJAL1_RM	4	SYSRST	Thermal Alarm 1 Rising Interrupt Mask. Setting this bit prevents the TJAL1_R bit from causing hardware interrupts.	0 = TJAL1_R is not masked. 1 = TJAL1_R is masked.
nENLDO_RM	3	SYSRST	nENLDO Rising Interrupt Mask. Setting this bit prevents the nENLDO_R bit from causing hardware interrupts.	0 = nENLDO_R is unmasked. 1 = nENLDO_R is masked.
nENLDO_FM	2	SYSRST	nENLDO Falling Interrupt Mask. Setting this bit prevents the nENLDO_F bit from causing hardware interrupts.	0 = nENLDO_F is not masked. 1 = nENLDO_F is masked.
RSVD	1	SYSRST	Reserved. Bit is a *don't care.*	N/A
RSVD	0	SYSRST	Reserved. Bit is a *don't care.*	N/A

INT_M_CHG (0x07)

BIT	7	6	5	4	3	2	1	0
Field	RSVD	SYS_ CNFG_M	SYS_ CTRL_M	CHGIN_ CTRL_M	TJ_REG_M	CHGIN_M	CHG_M	THM_M
Reset	0b1	0b1	0b1	0b1	0b1	0b1	0b1	0b1
Access Type	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	RESET-TYPE	DESCRIPTION	DECODE
RSVD	7	SYSRST	Reserved. Bit is a *don't care.*	N/A
SYS_ CNFG_M	6	SYSRST	Setting this bit prevents the SYS_CNFG_I bit from causing hardware interrupts.	0 = SYS_CNFG_I is not masked. 1 = SYS_CNFG_I is masked.
SYS_ CTRL_M	5	SYSRST	Setting this bit prevents the SYS_CTRL_I bit from causing hardware interrupts.	0 = SYS_CTRL_I is not masked. 1 = SYS_CTRL_I is masked.
CHGIN_ CTRL_M	4	SYSRST	Setting this bit prevents the CHGIN_ CTRL_I bit from causing hardware interrupts.	0 = CHGIN_CTRL_I is not masked. 1 = CHGIN_CTRL_I is masked.
TJ_REG_M	3	SYSRST	Setting this bit prevents the TJ_REG_I bit from causing hardware interrupts.	0 = TJ_REG_I is not masked. 1 = TJ_REG_I is masked.
CHGIN_M	2	SYSRST	Setting this bit prevents the CHGIN_I bit from causing hardware interrupts.	0 = CHGIN_I is not masked. 1 = CHGIN_I is masked.
CHG_M	1	SYSRST	Setting this bit prevents the CHG_I bit from causing hardware interrupts.	0 = CHG_I is not masked. 1 = CHG_I is masked.
THM_M	0	SYSRST	Setting this bit prevents the THM_I bit from causing hardware interrupts.	0 = THM_I is not masked. 1 = THM_I is masked.

CNFG_GLBL (0x08)

BIT	7	6	5	4	3	2	1	0
Field	PU_DIS	T_MRST	BIAS_LPM	BIAS_REQ	nENLDO_ MODE	DB_nEN-LDO	SFT_CTRL[1:0]	
Reset	0b0	OTP	0b1	0b0	OTP	OTP	0b00	
Access Type	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	

BITFIELD	BITS	RESET-TYPE	DESCRIPTION	DECODE
PU_DIS	7	SYSRST	nENLDO Internal Pullup Resistor Control to VCCINT	0 = nENLDO pullup resistor enabled 1 = nENLDO pullup resistor disabled
T_MRST	6	SYSRST	Sets the Manual Reset Time (t_{MRST})	0 = 8 seconds 1 = 16 seconds
BIAS_LPM	5	SYSRST	System Bias Low-Power Mode Software Request	0 = Bias requested to be in normal-power mode whenever it is enabled. 1 = Bias requested to be in low-power mode whenever it is enabled.
BIAS_REQ	4	SYSRST	System Bias Enable Software Request	0 = Bias not requested on by software. 1 = Bias forced on by software.
nENLDO_ MODE	3	SYSRST	nENLDO (ONKEY) Default Configuration Mode	0 = Push-button mode 1 = Slide-switch mode
DB_nENLDO	2	SYSRST	Debounce Timer for the nENLDO pin	0 = 200µs debounce 1 = 30ms debounce
SFT_CTRL	1:0	SYSRST	Software Control Functions	0b00 = No Action 0b01 = Software Reset. Causes a power-reset. The IC powers down, configuration registers reset (SYSRST), and the IC powers up and turns the LDO on again. 0b10 = Software Off. The IC powers down, configuration registers reset, and the IC remains off and waits for a wake-up event to turn on again. 0b11 = Factory-Ship Mode Enter (FSM). The IC powers down, configuration registers reset, and the internal BATT to SYS switch opens. The device remains this way until a factory-ship mode exit event occurs.

CID (0x09)

BIT	7	6	5	4	3	2	1	0
Field	—	—	—	—	CID[3:0]			
Reset	—	—	—	—	OTP			
Access Type	—	—	—	—	Read Only			

BITFIELD	BITS	RESET-TYPE	DESCRIPTION	DECODE
CID	3:0	SYSPOR	Chip Identification Code for OTP Options	Varies depending on *Factory Options*.

CNFG_WDT (0x0A)

BIT	7	6	5	4	3	2	1	0
Field	RSVD	RSVD	WDT_PER[1:0]		WDT_MODE	WDT_CLR	WDT_EN	WDT_LOCK
Reset	0b0	0b0	0b11		0b0	0b0	OTP	OTP
Access Type	Write, Read	Write, Read	Write, Read		Write, Read	Write 1 to Clear, Read	Write, Read	Read Only

BITFIELD	BITS	RESET-TYPE	DESCRIPTION	DECODE
RSVD	7	SYSRST	Reserved. Bit is a *don't care.*	N/A
RSVD	6	SYSRST	Reserved. Bit is a *don't care.*	N/A
WDT_PER	5:4	SYSRST	Watchdog Timer Period. Sets t_{WD}. Watchdog timer is reset to the programmed value as soon as this bitfield is changed.	0b00 = 16 seconds 0b01 = 32 seconds 0b10 = 64 seconds 0b11 = 128 seconds
WDT_MODE	3	SYSRST	Watchdog Timer Expired Action. Determines what the IC does after the watchdog timer expires.	0 = Watchdog timer expire causes power-off. 1 = Watchdog timer expire causes power-reset.
WDT_CLR	2	SYSRST	Watchdog Timer Clear Control. Set this bit to feed (reset) the watchdog timer.	0 = Watchdog timer period is not reset. 1 = Watchdog timer is reset back to t_{WD}.
WDT_EN	1	SYSRST	Watchdog Timer Enable. Write protected depending on WDT_LOCK.	0 = Watchdog timer is not enabled. WDT_EXP = 0 always. 1 = Watchdog timer is enabled. If the timer expires without being fed (reset) then WDT_EXP = 1.
WDT_LOCK	0	SYSRST	Factory-Set Safety Bit for the Watchdog Timer. Determines if the timer can be disabled through WTD_EN or not.	0 = Watchdog timer can be enabled and disabled with WDT_EN. 1 = Watchdog timer can not be disabled with WDT_EN. (WDT_EN can still be used to enable the watchdog timer.)

CNFG_CHG_A (0x20)

BIT	7	6	5	4	3	2	1	0
Field	THM_HOT[1:0]		THM_WARM[1:0]		THM_COOL[1:0]		THM_COLD[1:0]	
Reset	0b00		0b00		0b11		0b11	
Access Type	Write, Read		Write, Read		Write, Read		Write, Read	

BITFIELD	BITS	RESET-TYPE	DESCRIPTION	DECODE
THM_HOT	7:6	SYSRST	Sets the V_{HOT} JEITA Temperature Threshold	0b00 = 0.411V 0b01 = 0.367V 0b10 = 0.327V 0b11 = 0.291V
THM_WARM	5:4	SYSRST	Sets the V_{WARM} JEITA Temperature Threshold	0b00 = 0.511V 0b01 = 0.459V 0b10 = 0.411V 0b11 = 0.367V
THM_COOL	3:2	SYSRST	Sets the V_{COOL} JEITA Temperature Threshold	0b00 = 0.923V 0b01 = 0.867V 0b10 = 0.807V 0b11 = 0.747V
THM_COLD	1:0	SYSRST	Sets the V_{COLD} JEITA Temperature Threshold	0b00 = 1.024V 0b01 = 0.976V 0b10 = 0.923V 0b11 = 0.867V

CNFG_CHG_B (0x21)

BIT	7	6	5	4	3	2	1	0
Field	VCHGIN_MIN[2:0]			ICHGIN_LIM[2:0]			I_PQ	CHG_EN
Reset	0b000			0b000			0b0	OTP
Access Type	Write, Read			Write, Read			Write, Read	Write, Read

BITFIELD	BITS	RESET-TYPE	DESCRIPTION	DECODE
VCHGIN_MIN	7:5	SYSRST	Sets the Minimum CHGIN Regulation Voltage ($V_{CHGIN-MIN}$)	0b000 = 4.0V 0b001 = 4.1V 0b010 = 4.2V 0b011 = 4.3V 0b100 = 4.4V 0b101 = 4.5V 0b110 = 4.6V 0b111 = 4.7V
ICHGIN_LIM	4:2	CHGPOK	Sets the CHGIN Input Current Limit ($I_{CHGIN-LIM}$)	This bitfield decoding changes depending on factory option. See Table 8 for details. 0b000 = 95mA/475mA 0b001 = 190mA/380mA 0b010 = 285mA 0b011 = 380mA/190mA 0b100-0b111 = 475mA/95mA
I_PQ	1	SYSRST	Sets the prequalification charge current (I_{PQ}) as a percentage of $I_{FAST-CHG}$.	0 = 10% 1 = 20%
CHG_EN	0	SYSRST	Charger enable	0 = Disabled 1 = Enabled

CNFG_CHG_C (0x22)

BIT	7	6	5	4	3	2	1	0
Field	CHG_PQ[2:0]			I_TERM[1:0]		T_TOPOFF[2:0]		
Reset	0b111			0b11		0b000		
Access Type	Write, Read			Write, Read		Write, Read		

BITFIELD	BITS	RESET-TYPE	DESCRIPTION	DECODE
CHG_PQ	7:5	SYSRST	Sets the Battery Prequalification Voltage Threshold (V_{PQ})	0b000 = 2.3V 0b001 = 2.4V 0b010 = 2.5V 0b011 = 2.6V 0b100 = 2.7V 0b101 = 2.8V 0b110 = 2.9V 0b111 = 3.0V
I_TERM	4:3	SYSRST	Sets the Battery Charge Termination Current (I_{TERM}) as a Percentage of $I_{FAST-CHG}$	0b00 = 5% 0b01 = 7.5% 0b10 = 10% 0b11 = 15%
T_TOPOFF	2:0	SYSRST	Sets the Top-Off Timer Value (t_{TO})	0b000 = 0 minutes 0b001 = 5 minutes 0b010 = 10 minutes 0b011 = 15 minutes 0b100 = 20 minutes 0b101 = 25 minutes 0b110 = 30 minutes 0b111 = 35 minutes

CNFG_CHG_D (0x23)

BIT	7	6	5	4	3	2	1	0
Field	TJ_REG[2:0]			VSYS_REG[4:0]				
Reset	0b000			0b10000				
Access Type	Write, Read			Write, Read				

BITFIELD	BITS	RESET-TYPE	DESCRIPTION	DECODE
TJ_REG	7:5	SYSRST	Sets the Die Junction Temperature Regulatoin Point (T_{J-REG})	0b000 = 60°C 0b001 = 70°C 0b010 = 80°C 0b011 = 90°C 0b100-0b111 = 100°C
VSYS_REG	4:0	SYSRST	Sets the System Voltage Regulation Point While CHGIN is Valid ($V_{SYS-REG}$). This 5-bit configuration is a linear transfer function that starts at 4.1V and ends at 4.8V, with 25mV increments.	0b00000 = 4.100V 0b00001 = 4.125V 0b00010 = 4.150V ... 0b10000 = 4.500V ... 0b11010 = 4.750V 0b11011 = 4.775V 0b11100-0b11111 = 4.800V

CNFG_CHG_E (0x24)

BIT	7	6	5	4	3	2	1	0
Field	CHG_CC[5:0]						T_FAST_CHG[1:0]	
Reset	0b000001						0b01	
Access Type	Write, Read						Write, Read	

BITFIELD	BITS	RESET-TYPE	DESCRIPTION	DECODE
CHG_CC	7:2	SYSRST	Sets the Fast-Charge Constant Current Value ($I_{FAST-CHG}$). This 6-bit configuration is a linear transfer function that starts at 7.5mA and ends at 300mA, with 7.5mA increments.	0b000000 = 7.5mA 0b000001 = 15mA ... 0b100111-0b111111 = 300mA
T_FAST_CHG	1:0	SYSRST	Sets the Fast-Charge Safety Timer (t_{FC})	0b00 = timer disabled 0b01 = 3 hours 0b10 = 5 hours 0b11 = 7 hours

CNFG_CHG_F (0x25)

BIT	7	6	5	4	3	2	1	0
Field	CHG_CC_JEITA[5:0]						THM_EN	RSVD
Reset	0b000001						0b0	0b0
Access Type	Write, Read						Write, Read	Write, Read

BITFIELD	BITS	RESET-TYPE	DESCRIPTION	DECODE
CHG_CC_JEITA	7:2	SYSRST	Sets $I_{FAST-CHG\_JEITA}$ for when the battery is either cool or warm as defined by the T_{COOL} and T_{WARM} temperature thresholds. This register is a *don't care* if the battery temperature is normal or if THM_EN = 0. This 6-bit configuration is a linear transfer function that starts at 7.5mA and ends at 300mA, with 7.5mA increments.	0b000000 = 7.5mA 0b000001 = 15mA ... 0b100111-0b111111 = 300mA
THM_EN	1	SYSRST	Thermistor Enable. Setting this bit causes the charger to enable the thermistor bias (TBIAS) and continuously monitor battery temperature. Does not collide with MUX_SEL[3:0] settings 0x7 or 0x8.	0 = Disabled 1 = Enabled
RSVD	0	SYSRST	Reserved Control Bit. Write to 0.	N/A

CNFG_CHG_G (0x26)

BIT	7	6	5	4	3	2	1	0
Field	CHG_CV[5:0]						USBS	RSVD
Reset	0b000000						0b0	0b0
Access Type	Write, Read						Write, Read	Write, Read

BITFIELD	BITS	RESET-TYPE	DESCRIPTION	DECODE
CHG_CV	7:2	SYSRST	Sets fast-charge battery regulation voltage ($V_{FAST-CHG}$). Internal logic clamps the maximum $V_{FAST-CHG}$ value to 200mV less than $V_{SYS-REG}$. This 6-bit configuration is a linear transfer function that starts at 3.6V and ends at 4.6V, with 25mV increments.	0b000000 = 3.600V 0b000001 = 3.625V ... 0b1010000-0b111111 = 4.6V
USBS	1	CHGPOR	Setting this bit places CHGIN in USB suspend mode. CHGIN can not draw power from an external source while in USB suspend mode.	0 = CHGIN is not suspended. 1 = CHGIN is suspended.
RSVD	0	SYSRST	Reserved. Bit is a *don't care.*	N/A

CNFG_CHG_H (0x27)

BIT	7	6	5	4	3	2	1	0
Field	CHG_CV_JEITA[5:0]						RSVD	RSVD
Reset	0b000000						0b0	0b0
Access Type	Write, Read						Write, Read	Write, Read

BITFIELD	BITS	RESET-TYPE	DESCRIPTION	DECODE
CHG_ CV_JEITA	7:2	SYSRST	Sets $V_{FAST-CHG\_JEITA}$ for when the battery is either cool or warm as defined by the T_{COOL} and T_{WARM} temperature thresholds. This register is a *don't care* if the battery temperature is normal or if THM_EN = 0. Internal logic clamps the maximum $V_{FAST-CHG\_JEITA}$ value to 200mV less than $V_{SYS-REG}$. This 6-bit configuration is a linear transfer function that starts at 3.6V and ends at 4.6V, with 25mV increments.	0b000000 = 3.600V 0b000001 = 3.625V ... 0b1010000-0b111111 = 4.6V
RSVD	1	SYSRST	Reserved. Bit is a *don't care.*	N/A
RSVD	0	SYSRST	Reserved. Bit is a *don't care.*	N/A

CNFG_CHG_I (0x28)

BIT	7	6	5	4	3	2	1	0
Field	IMON_DISCHG_SCALE[3:0]				MUX_SEL[3:0]			
Reset	0b1111				0b0000			
Access Type	Write, Read				Write, Read			

BITFIELD	BITS	RESET-TYPE	DESCRIPTION	DECODE
IMON_ DISCHG_ SCALE	7:4	SYSRST	Selects the battery discharge current full-scale current value. This 4-bit configuration starts at 8.2 and ends at 300mA.	0b0000 = 8.2mA 0b0001 = 40.5mA 0b0010 = 72.3mA 0b0011 = 103.4mA 0b0100 = 134.1mA 0b0101 = 164.1mA 0b0110 = 193.7mA 0b0111 = 222.7mA 0b1000 = 251.2mA 0b1001 = 279.3mA 0b1010-0b1111 = 300mA
MUX_SEL	3:0	SYSRST	Selects the analog channel to connect to AMUX. The AMUX output buffer consumes current unless it is in the 0b0000 state. When measurements are not needed, configure MUX_SEL[3:0] = 0b0000.	0b0000 = Multiplexer is disabled and AMUX is high-impedance. 0b0001 = CHGIN voltage monitor. 0b0010 = CHGIN current monitor. 0b0011 = BATT voltage monitor. 0b0100 = BATT charge current monitor. Valid only while battery charging is happening (CHG = 1). 0b0101 = BATT discharge current monitor normal measurement. 0b0110 = BATT discharge current monitor nulling measurement. 0b0111 = THM voltage monitor. 0b1000 = TBIAS voltage monitor. 0b1001 = AGND voltage monitor (through 100Ω pulldown resistor). 0b1010-0b1111 = SYS voltage monitor.

CNFG_LDO_A (0x30)

BIT	7	6	5	4	3	2	1	0
Field	ADE_LDO	LDO_VREG[6:0]						
Reset	0b1	OTP						
Access Type	Write, Read	Write, Read						

BITFIELD	BITS	RESET-TYPE	DESCRIPTION	DECODE
ADE_LDO	7	SYSRST	LDO Active Discharge Resistor Control	0 = Disabled 1 = Enabled
LDO_VREG	6:0	SYSRST	LDO Target Regulation Voltage ($V_{LDO-REG}$). This 7-bit configuration is a linear transfer function that starts at 0.8V and ends at 3.975V, with 25mV increments.	0x00 = 0.800V 0x01 = 0.825V ... 0x27 = 1.775V 0x28 = 1.800V ... 0x7E = 3.950V 0x7F = 3.975V

CNFG_LDO_B (0x31)

BIT		3	2	1	0
Field		LDO_PM[1:0]		LDO_EN[1:0]	
Reset		0b01		OTP	
Access Type		Write, Read		Write, Read	

BITFIELD	BITS	RESET-TYPE	DESCRIPTION	DECODE
LDO_PM	3:2	SYSRST	LDO Power Mode Control	0b00 = Forced low-power mode 0b01 = Forced normal mode 0b10 = Pin-controlled, active high (normal mode when PMLDO pin is high) 0b11 = Pin-controlled, active low (normal mode when PMLDO pin is low)
LDO_EN	1:0	SYSRST	LDO Enable Control	0b00 = LDO is forced disabled 0b01 = LDO is forced enabled 0b10 = LDO enables when nENLDO asserts or when CHGIN is valid. 0b11 = Same as 0b10.

CNFG_SNK1_A (0x40)

BIT	7	6	5	4	3	2	1	0
Field	SNK_FS1[1:0]		INV_SNK1	BRT_SNK1[4:0]				
Reset	0b00		0b0	0b00100				
Access Type	Write, Read		Write, Read	Write, Read				

BITFIELD	BITS	RESET-TYPE	DESCRIPTION	DECODE
SNK_FS1	7:6	SYSRST	SNK1 Enable and Full-Scale Range Control	0b00 = Disabled 0b01 = Enabled with 3.2mA full-scale range (0.1mA LSB) 0b10 = Enabled with 6.4mA full-scale range (0.2mA LSB) 0b11 = Enabled with 12.8mA full-scale range (0.4mA LSB)
INV_SNK1	5	SYSRST	SNK1 Invert Control	0 = Positive-Duty Operation. SNK1 is on during the beginning of each period for the programmed duty length. 1 = Negative-Duty Operation. SNK1 is off during the beginning of each period for the programmed duty length.
BRT_SNK1	4:0	SYSRST	SNK1 Current (Brightness) Control **SNK_FS1[1:0] = 0b00** *don't care* **SNK_FS1[1:0] = 0b11** 0.1mA–3.2mA in 0.1mA steps **SNK_FS1[1:0] = 0b10** 0.2mA–6.4mA in 0.2mA steps **SNK_FS1[1:0] = 0b11** 0.4mA–12.8mA in 0.4mA steps	0x00 = 0.1mA/0.2mA/0.4mA 0x01 = 0.2mA/0.4mA/0.8mA ... 0x1F = 3.2mA/6.4mA/12.8mA

CNFG_SNK1_B (0x41)

BIT	7	6	5	4	3	2	1	0
Field	P_SNK1[3:0]				D_SNK1[3:0]			
Reset	0b0000				0b1111			
Access Type	Write, Read				Write, Read			

BITFIELD	BITS	RESET-TYPE	DESCRIPTION	DECODE
P_SNK1	7:4	SYSRST	SNK1 Period Control	0x0 = 0.5s 0x1 = 1.0s 0x2 = 1.5s 0x3 = 2.0s 0x4 = 2.5s 0x5 = 3.0s 0x6 = 3.5s 0x7 = 4.0s 0x8 = 4.5s 0x9 = 5.0s 0xA = 5.5s 0xB = 6.0s 0xC = 6.5s 0xD = 7.0s 0xE = 7.5s 0xF = 8s
D_SNK1	3:0	SYSRST	SNK1 Duty Cycle Control	0x0 = 6.25% 0x1 = 12.5% 0x2 = 18.75% 0x3 = 25% 0x4 = 31.25% 0x5 = 37.5% 0x6 = 43.75% 0x7 = 50% 0x8 = 56.25% 0x9 = 62.5% 0xA = 68.75% 0xB = 75% 0xC = 81.25% 0xD = 87.5% 0xE = 93.75% 0xF = 100%

CNFG_SNK2_A (0x42)

BIT	7	6	5	4	3	2	1	0
Field	SNK_FS2[1:0]		INV_SNK2	BRT_SNK2[4:0]				
Reset	0b00		0b0	0b00100				
Access Type	Write, Read		Write, Read	Write, Read				

BITFIELD	BITS	RESET-TYPE	DESCRIPTION	DECODE
SNK_FS2	7:6	SYSRST	SNK2 Enable and Full-Scale Range Control	0b00 = Disabled 0b01 = Enabled with 3.2mA full-scale range (0.1mA LSB) 0b10 = Enabled with 6.4mA full-scale range (0.2mA LSB) 0b11 = Enabled with 12.8mA full-scale range (0.4mA LSB)
INV_SNK2	5	SYSRST	SNK2 Invert Control	0 = Positive-Duty Operation. SNK2 is on during the beginning of each period for the programmed duty length. 1 = Negative-Duty Operation. SNK2 is off during the beginning of each period for the programmed duty length.
BRT_SNK2	4:0	SYSRST	SNK2 Current (Brightness) Control **SNK_FS2[1:0] = 0b00** *don't care* **SNK_FS2[1:0] = 0b11** 0.1mA–3.2mA in 0.1mA steps **SNK_FS2[1:0] = 0b10** 0.2mA–6.4mA in 0.2mA steps **SNK_FS2[1:0] = 0b11** 0.4mA–12.8mA in 0.4mA steps	0x00 = 0.1mA/0.2mA/0.4mA 0x01 = 0.2mA/0.4mA/0.8mA ... 0x1F = 3.2mA/6.4mA/12.8mA

CNFG_SNK2_B (0x43)

BIT	7	6	5	4	3	2	1	0
Field	P_SNK2[3:0]				D_SNK2[3:0]			
Reset	0b0000				0b1111			
Access Type	Write, Read				Write, Read			

BITFIELD	BITS	RESET-TYPE	DESCRIPTION	DECODE
P_SNK2	7:4	SYSRST	SNK2 Period Control	0x0 = 0.5s 0x1 = 1.0s 0x2 = 1.5s 0x3 = 2.0s 0x4 = 2.5s 0x5 = 3.0s 0x6 = 3.5s 0x7 = 4.0s 0x8 = 4.5s 0x9 = 5.0s 0xA = 5.5s 0xB = 6.0s 0xC = 6.5s 0xD = 7.0s 0xE = 7.5s 0xF = 8s
D_SNK2	3:0	SYSRST	SNK2 Duty Cycle Control	0x0 = 6.25% 0x1 = 12.5% 0x2 = 18.75% 0x3 = 25% 0x4 = 31.25% 0x5 = 37.5% 0x6 = 43.75% 0x7 = 50% 0x8 = 56.25% 0x9 = 62.5% 0xA = 68.75% 0xB = 75% 0xC = 81.25% 0xD = 87.5% 0xE = 93.75% 0xF = 100%

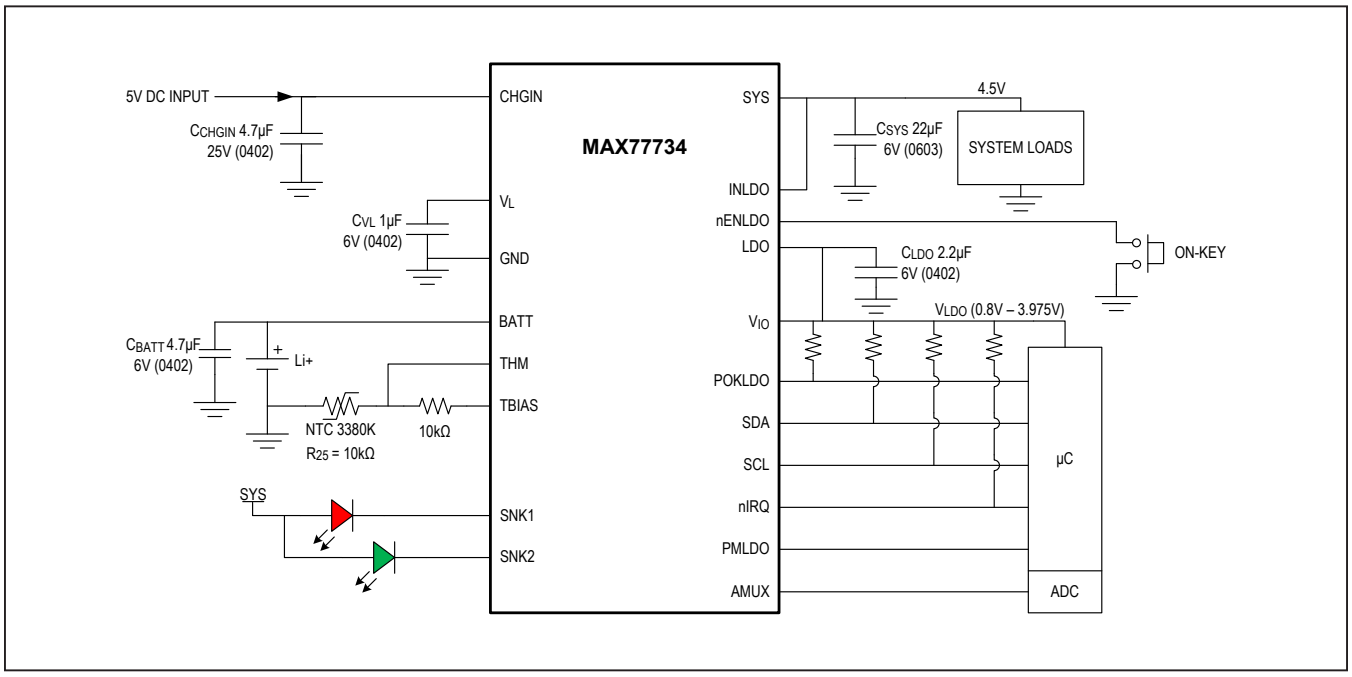
CNFG_SNK_TOP (0x44)

BIT	7	6	5	4	3	2	1	0
Field	—	—	—	—	—	—	CLK_64_S	EN_SNK_ MSTR
Reset	—	—	—	—	—	—	0b0	0b0
Access Type	—	—	—	—	—	—	Read Only	Write, Read

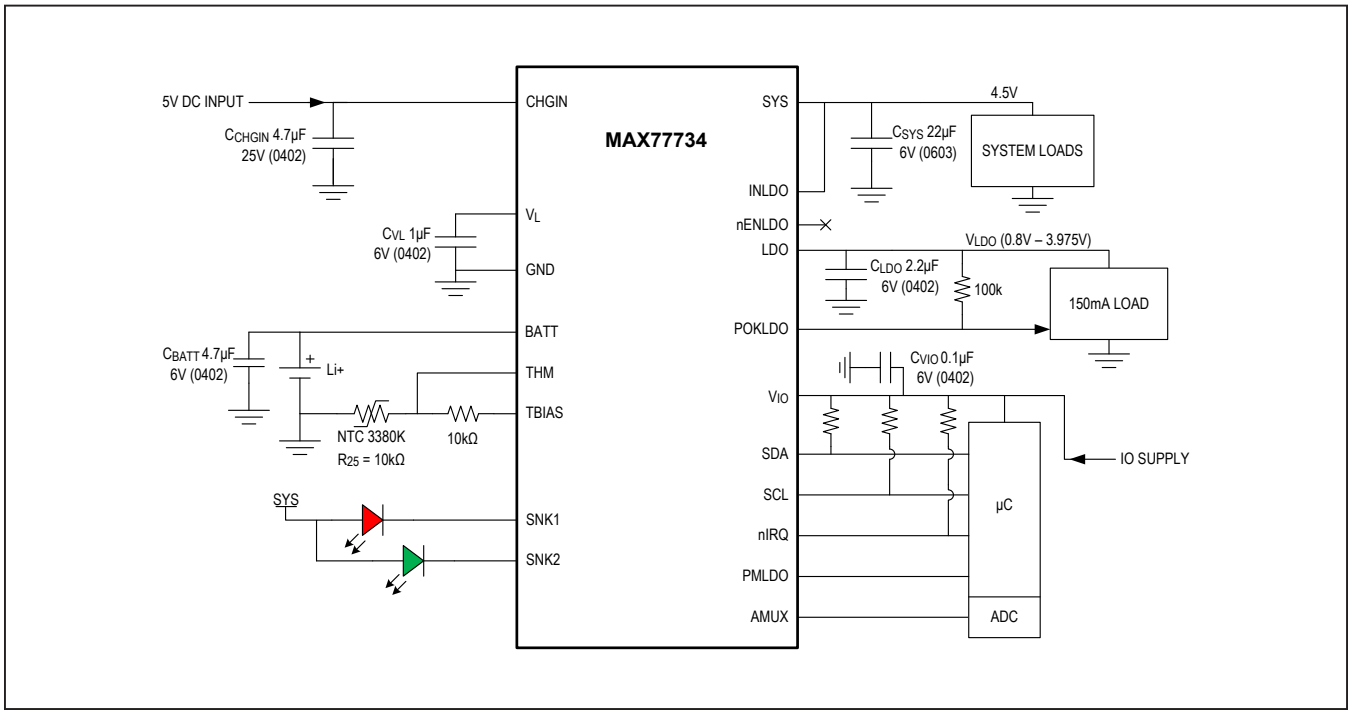
BITFIELD	BITS	RESET-TYPE	DESCRIPTION	DECODE
RSVD	7:2	—		
CLK_64_S	1	SYSRST	64Hz Clock Mirror. CLK_64_S is internally driven by the same clock that drives the current sink PWM logic. This signal has a 10% duty cycle. Allows software to align LED blink patterns between SNK1 and SNK2.	0 = Root clock is low. 1 = Root clock is high.
EN_SNK_ MSTR	0	SYSRST	Master Sink Enable Bit	0 = Current sinks disabled. 1 = Current sinks enabled.

Typical Application Circuits

Battery Charger using LDO Hardware Enable Key



Battery Charger using LDO Software Enable



Ordering Information

PART NUMBER	TEMP RANGE	PIN-PACKAGE	FACTORY OPTIONS
MAX77734ENP+*	-40°C to +85°C	20 WLP	Various OTP options for sampling
MAX77734AENP+T**	-40°C to +85°C	20 WLP	A
MAX77734BENP+T	-40°C to +85°C	20 WLP	B
MAX77734CENP+T	-40°C to +85°C	20 WLP	C

+Denotes a lead(Pb)-free/RoHS-compliant package.

T = Tape and reel.

**Custom samples only. Not for production or stock. Contact factory for information.*

***Future product—contact factory for availability.*

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	6/17	Initial release	—
1	9/17	Updated *General Description* and *Applications* sections, replaced Simplified Application Circuit, Figure 5, Figure 8, Figure 13, and Figure 15, updated *Typical Operating Characteristics*, Table 1 changed to Table 3, Table 3 changed to Table 1, corrected symbology	1, 15, 17, 20, 21, 25−28, 30−33, 38, 39, 45, 47, 73, 74
2	5/18	Updated *Electrical Characteristics* tables, updated TOC6, replaced Table 10, updated Figure 13, added new section called *PCB Layout Guidelines*, updated CNFG_CHG_I (0x28) in Register Map, updated *Ordering Information* table	1, 3, 7, 9, 19, 20, 26, 29, 30, 33, 42, 45-47, 66, 73, 74

