Freescale Semiconductor
Product Brief

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MCF5216 Integrated Microcontroller Product Brief

The MCF5216 is a highly-integrated implementation of the ColdFire® family of reduced instruction set computing (RISC) microprocessors. This document provides an overview of the 32-bit MCF5216 microcontroller, focusing on its highly integrated and diverse feature set.

NOTE

Unless otherwise noted, information in this document also applies to the MCF5214.

This 32-bit device is based on the version 2 ColdFire reduced instruction set computer (RISC) core operating at a core/bus frequency up to 66 MHz. On-chip memories connected tightly to the processor core include 512 Kbytes of Flash (256 Kbytes on the MCF5214), 64 Kbytes of static random access memory (SRAM) and 2 Kbytes of configurable-cache SRAM. On-chip modules include:

- V2 ColdFire core with enhanced multiply-accumulate engine and support for separate user/supervisor stack pointer registers,

Contents

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providing 58.9 Dhrystone 2.1 MIPS @ 66.7 MHz executing out of on-chip Flash and SRAM.

- FlexCAN controller area network (CAN) module
- Three universal asynchronous/synchronous receiver/transmitters (UARTs)
- Inter-integrated circuit (I^2C™) bus controller
- Queued serial peripheral interface (QSPI) module
- Queued analog-to-digital converter (QADC)
- Four channel direct memory access (DMA) controller
- Four 32-bit input capture/output compare timers with DMA support
- Two general-purpose timers (GPTs) with four independent channels capable of input capture/output compare, pulse width modulation (PWM) and pulse accumulation
- Four 16-bit periodic interrupt timers (PITs)
- Programmable software watchdog timer
- Interrupt controller capable of handling 126 selectable-priority interrupt sources
- Clock module with integrated phase locked loop (PLL)
- External-bus interface module including a synchronous DRAM controller
- Test access/debug port
- Up to seven chip-select signals
- Enhanced Multiply Accumulate Unit (EMAC) and hardware divide module

1.1 Block Diagram

The MCF5216 comes in a 256 mold array process ball grid array (MAPBGA) package and can be configured for either single-chip operation or external bus, master mode operation. Figure 1 shows a top-level block diagram of the MCF5216.

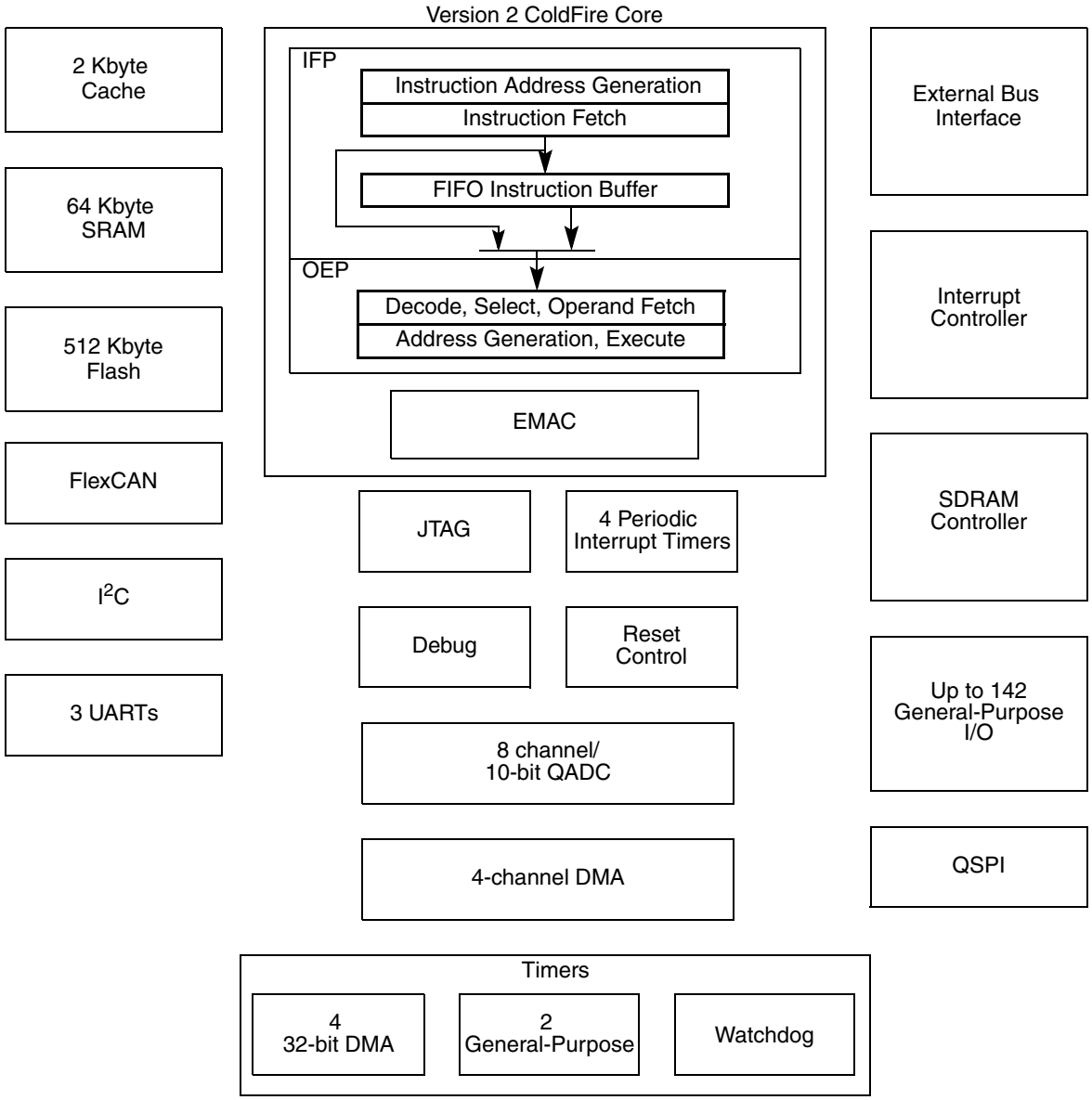

Figure 1. MCF5216 Block Diagram

1.2 Features

1.2.1 Feature Overview

- Version 2 ColdFire variable-length RISC processor core
  - Static operation
  - 32-bit address and data path on-chip
  - 66 MHz processor core and bus frequency
  - Sixteen general-purpose 32-bit data and address registers
  - Implements ColdFire ISA_A with extensions to support the user stack pointer register, and 4 new instructions for improved bit processing
  - Enhanced Multiply-Accumulate (EMAC) unit with four 48-bit accumulators to support 32-bit signal processing algorithms
  - Illegal instruction decode that allows for 68K emulation support
- System debug support
  - Real time trace for determining dynamic execution path
  - Background debug mode (BDM) for in-circuit debugging
  - Real time debug support, with two user-visible hardware breakpoint registers (PC and address with optional data) that can be configured into a 1- or 2-level trigger
- On-chip memories
  - 2 Kbyte cache, configurable as instruction-only, data-only, or split I-/D-cache
  - 64 Kbyte dual-ported SRAM on CPU internal bus, accessible by core and non-core bus masters (e.g., DMA, FEC) with standby power supply support
  - 512 Kbytes of interleaved Flash memory supporting 2-1-1-1 accesses
- Power management
  - Fully static operation with processor sleep and whole chip stop modes
  - Very rapid response to interrupts from the low-power sleep mode (wake-up feature)
  - Clock enable/disable for each peripheral when not used
- Fast Ethernet Controller (FEC)
  - 10 BaseT capability, half or full duplex
  - 100 BaseT capability, half duplex or full duplex
  - On-chip transmit and receive FIFOs
  - Built-in dedicated DMA controller
  - Memory-based flexible descriptor rings
  - Media independent interface (MII) to transceiver (PHY)

- FlexCAN 2.0B Module
  - Based on and includes all existing features of the Freescale TOUCAN module
  - Full implementation of the CAN protocol specification version 2.0B
    - Standard Data and Remote Frames (up to 109 bits long)
    - Extended Data and Remote Frames (up to 127 bits long)
    - 0-8 bytes data length
    - Programmable bit rate up to 1 Mbit/sec
  - Flexible Message Buffers (MBs), totalling up to 16 message buffers of 0–8 byte data length each, configurable as Rx or Tx, all supporting standard and extended messages
  - Unused MB space can be used as general purpose RAM space
  - Listen only mode capability
  - Content-related addressing
  - No read/write semaphores
  - Three programmable mask registers: global (for MBs 0-13), special for MB14 and special for MB15
  - Programmable transmit-first scheme: lowest ID or lowest buffer number
  - "Time stamp" based on 16-bit free-running timer
  - Global network time, synchronized by a specific message
  - Programmable I/O modes
  - Maskable interrupts
- Three Universal Asynchronous/synchronous Receiver Transmitters (UARTs)
  - 16-bit divider for clock generation
  - Interrupt control logic
  - Maskable interrupts
  - DMA support
  - Data formats can be 5, 6, 7 or 8 bits with even, odd or no parity
  - Up to 2 stop bits in 1/16 increments
  - Error-detection capabilities
  - Modem support includes request-to-send ($\overline{\text{URTS}}$) and clear-to-send ($\overline{\text{UCTS}}$) lines for two UARTs
  - Transmit and receive FIFO buffers
- I^2C Module
  - Interchip bus interface for EEPROMs, LCD controllers, A/D converters, and keypads
  - Fully compatible with industry-standard I^2C bus
  - Master or slave modes support multiple masters
  - Automatic interrupt generation with programmable level

- Queued Serial Peripheral Interface (QSPI)
  - Full-duplex, three-wire synchronous transfers
  - Up to four chip selects available
  - Master mode operation only
  - Programmable master bit rates
  - Up to 16 pre-programmed transfers
- Queued Analog-to-Digital Converter (QADC)
  - 8 direct, or up to 18 multiplexed, analog input channels
  - 10-bit resolution +/- 2 counts accuracy
  - Minimum 7 μS conversion time
  - Internal sample and hold
  - Programmable input sample time for various source impedances
  - Two conversion command queues with a total of 64 entries
  - Sub-queues possible using pause mechanism
  - Queue complete and pause software interrupts available on both queues
  - Queue pointers indicate current location for each queue
  - Automated queue modes initiated by:
    - External edge trigger and gated trigger
    - Periodic/interval timer, within QADC module [Queue 1 and 2]
    - Software command
  - Single-scan or continuous-scan of queues
  - Output data readable in three formats:
    - Right-justified unsigned
    - Left-justified signed
    - Left-justified unsigned
  - Unused analog channels can be used as digital I/O
  - Low pin-count configuration implemented
- Four 32-bit DMA Timers
  - 15-ns resolution at 66.7 MHz
  - Programmable sources for clock input, including an external clock option
  - Programmable prescaler
  - Input-capture capability with programmable trigger edge on input pin
  - Output-compare with programmable mode for the output pin
  - Free run and restart modes
  - Maskable interrupts on input capture or reference-compare
  - DMA trigger capability on input capture or reference-compare

- Two 4-channel General Purpose Timers
  - Four 16-bit input capture/output compare channels per timer
  - 16-bit architecture
  - Programmable prescaler
  - Pulse widths variable from microseconds to seconds
  - Single 16-bit pulse accumulator
  - Toggle-on-overflow feature for pulse-width modulator (PWM) generation
  - One dual-mode pulse accumulation channel per timer
- Four Periodic Interrupt Timers (PITs)
  - 16-bit counter
  - Selectable as free running or count down
- Software Watchdog Timer
  - 16-bit counter
  - Low power mode support
- Phase Locked Loop (PLL)
  - Crystal or external oscillator reference
  - 2 to 10 MHz reference frequency for normal PLL mode
  - 33 to 66 MHz oscillator reference frequency for 1:1 mode
  - Low power modes supported
  - Separate clock output pin
- Interrupt Controllers (x2)
  - Support for up to 63 interrupt sources per interrupt controller (total for two controllers: 126), organized as follows:
    - 56 fully-programmable interrupt sources
    - 7 fixed-level interrupt sources
  - Seven external interrupt signals
  - Unique vector number for each interrupt source
  - Ability to mask any individual interrupt source or all interrupt sources (global mask-all)
  - Support for hardware and software interrupt acknowledge (IACK) cycles
  - Combinatorial path to provide wake-up from low power modes
- DMA Controller
  - Four fully programmable channels
  - Dual-address and single-address transfer support with 8-, 16- and 32-bit data capability along with support for 16-byte (4 x 32-bit) burst transfers
  - Source/destination address pointers that can increment or remain constant
  - 24-bit byte transfer counter per channel
  - Auto-alignment transfers supported for efficient block movement
  - Bursting and cycle steal support

- Software-programmable connections between the 11 DMA requesters in the UARTs (3), 32-bit timers (4) plus external logic (4) and the four DMA channels

- External Bus Interface
  - Glueless connections to external memory devices (e.g., SRAM, Flash, ROM, etc.)
  - SDRAM controller supports 8-, 16-, and 32-bit wide memory devices
  - Glueless interface to SRAM devices with or without byte strobe inputs
  - Programmable wait state generator
  - 32-bit bidirectional data bus
  - 24-bit address bus
  - Up to seven chip selects available
  - Byte/write enables (byte strobes)
  - Ability to boot from internal Flash memory or external memories that are 8, 16, or 32 bits wide
- Reset
  - Separate reset in and reset out signals
  - Seven sources of reset:
    - Power-on reset (POR)
    - External
    - Software
    - Watchdog
    - Loss of clock
    - Loss of lock
    - Low-voltage detection (LVD)
  - Status flag indication of source of last reset
- Chip Integration Module (CIM)
  - System configuration during reset
  - Support for single chip, master, and test modes
  - Selects one of four clock modes
  - Sets boot device and its data port width
  - Configures output pad drive strength
  - Unique part identification number and part revision number
- General Purpose I/O interface
  - Up to 142 bits of general purpose I/O
  - Coherent 32-bit control
  - Bit manipulation supported via set/clear functions
  - Unused peripheral pins may be used as extra GPIO
- JTAG support for system level board testing

1.2.2 V2 Core Overview

The processor core is comprised of two separate pipelines that are decoupled by an instruction buffer. The two-stage Instruction Fetch Pipeline (IFP) is responsible for instruction-address generation and instruction fetch. The instruction buffer is a first-in-first-out (FIFO) buffer that holds prefetched instructions awaiting execution in the Operand Execution Pipeline (OEP). The OEP includes two pipeline stages. The first stage decodes instructions and selects operands (DSOC); the second stage (AGEX) performs instruction execution and calculates operand effective addresses, if needed.

The V2 core implements the ColdFire Instruction Set Architecture Revision A with added support for a separate user stack pointer register and four new instructions to assist in bit processing. Additionally, the MCF5216 core includes the enhanced multiply-accumulate unit (EMAC) for improved signal processing capabilities. The EMAC implements a 4-stage execution pipeline, optimized for 32 x 32 bit operations, with support for four 48-bit accumulators. Supported operands include 16- and 32-bit signed and unsigned integers as well as signed fractional operands as well as a complete set of instructions to process these data types. The EMAC provides superb support for execution of DSP operations within the context of a single processor at a minimal hardware cost.

1.2.3 Debug Module

The ColdFire processor core debug interface is provided to support system debugging in conjunction with low-cost debug and emulator development tools. Through a standard debug interface, users can access real-time trace and debug information. This allows the processor and system to be debugged at full speed without the need for costly in-circuit emulators. The debug interface is a superset of the BDM interface provided on Freescale's 683xx family of parts.

The on-chip breakpoint resources include a total of 6 programmable registers—a set of address registers (with two 32-bit registers), a set of data registers (with a 32-bit data register plus a 32-bit data mask register), and one 32-bit PC register plus a 32-bit PC mask register. These registers can be accessed through the dedicated debug serial communication channel or from the processor's supervisor mode programming model. The breakpoint registers can be configured to generate triggers by combining the address, data, and PC conditions in a variety of single or dual-level definitions. The trigger event can be programmed to generate a processor halt or initiate a debug interrupt exception.

To support program trace, the Version 2 debug module provides processor status (PST[3:0]) and debug data (DDATA[3:0]) ports. These buses and the PSTCLK output provide execution status, captured operand data, and branch target addresses defining processor activity at the CPU's clock rate.

1.2.4 JTAG

The MCF5216 supports circuit board test strategies based on the Test Technology Committee of IEEE and the Joint Test Action Group (JTAG). The test logic includes a test access port (TAP) consisting of a 16-state controller, an instruction register, and three test registers (a 1-bit bypass register, a 256-bit boundary-scan register, and a 32-bit ID register). The boundary scan register links the device's pins into one shift register. Test logic, implemented using static logic design, is independent of the device system logic.

The MCF5216 implementation can do the following:

- Perform boundary-scan operations to test circuit board electrical continuity
- Sample MCF5216 system pins during operation and transparently shift out the result in the boundary scan register
- Bypass the MCF5216 for a given circuit board test by effectively reducing the boundary-scan register to a single bit
- Disable the output drive to pins during circuit-board testing
- Drive output pins to stable levels

1.2.5 On-chip Memories

1.2.5.1 Cache

The 2-Kbyte cache can be configured into one of three possible organizations: a 2-Kbyte instruction cache, a 2-Kbyte data cache or a split 1-Kbyte instruction/1-Kbyte data cache. The configuration is software-programmable by control bits within the privileged Cache Configuration Register (CACR). In all configurations, the cache is a direct-mapped single-cycle memory, organized as 128 lines, each containing 16 bytes of data. The memories consist of a 128-entry tag array (containing addresses and control bits) and a 2 KByte data array, organized as 512 x 32 bits. The tag and data arrays are accessed in parallel using the following address bits:

Configuration Tag Address Data Array Address

2 Kbyte I-Cache [10:4] [10:2]

2 Kbyte D-Cache [10:4] [10:2]

Split I-/D-Cache 0, [9:4] 0, [9:4] for instruction fetches 1, [9:4] 1, [9:4] for operand accesses

If the desired address is mapped into the cache memory, the output of the data array is driven onto the ColdFire core's local data bus, completing the access in a single cycle. If the data is not mapped into the tag memory, a cache miss occurs and the processor core initiates a 16-byte line-sized fetch. The cache module includes a 16-byte line fill buffer used as temporary storage during miss processing. For all data cache configurations, the memory operates in write-through mode and all operand writes generate an external bus cycle.

1.2.5.2 SRAM

The SRAM module provides a general-purpose 64-Kbyte memory block that the ColdFire core can access in a single cycle. The location of the memory block can be set to any 64-Kbyte boundary within the 4-Gbyte address space. The memory is ideal for storing critical code or data structures, for use as the system stack, or for storing FEC data buffers. Because the SRAM module is physically connected to the processor's high-speed local bus, it can quickly service core-initiated accesses or memory-referencing commands from the debug module.

The SRAM module is also accessible by non-core bus masters, for example the DMA and/or the FEC. The dual-ported nature of the SRAM makes it ideal for implementing applications with double-buffer schemes, where the processor and a DMA device operate in alternate regions of the SRAM to maximize system

performance. As an example, system performance can be increased significantly if Ethernet packets are moved from the FEC into the SRAM (rather than external memory) prior to any processing.

1.2.5.3 Flash

The ColdFire Flash Module (CFM) is a non-volatile memory (NVM) module for integration with the processor core. The CFM is constructed with eight banks of 32K x 16-bit Flash arrays to generate 512 Kbytes of 32-bit Flash memory. These arrays serve as electrically erasable and programmable, non-volatile program and data memory. The Flash memory is ideal for program and data storage for single-chip applications allowing for field reprogramming without requiring an external programming voltage source. The CFM interfaces to the V2 ColdFire core through an optimized read-only memory controller which supports interleaved accesses from the 2-cycle Flash arrays. A "backdoor" mapping of the Flash memory is used for all program, erase, and verify operations as well as providing a read datapath for non-core masters (e.g., DMA).

NOTE

The CFM on the MCF5214 is constructed with four banks of 32K x 16-bit Flash arrays to generate 256 Kbytes of 32-bit Flash memory.

1.2.6 Power Management

The MCF5216 incorporates several low power modes of operation which are entered under program control and exited by several external trigger events. An integrated Power-On Reset (POR) circuit monitors the input supply and forces an MCU reset as the supply voltage rises. The Low Voltage Detect (LVD) section monitors the supply voltage and is configurable to force a reset or interrupt condition if it falls below the LVD trip point. The RAM standby switch provides power to RAM when the supply voltage is higher than the standby voltage. If the supply voltage to chip falls below the standby battery voltage, the RAM is switched over to the standby supply.

1.2.7 FlexCAN

The FlexCAN module is a communication controller implementing the CAN protocol. The CAN protocol can be used as an industrial control serial data bus, meeting the specific requirements of real-time processing, reliable operation in a harsh EMI environment, cost-effectiveness, and required bandwidth. FlexCAN contains 16 message buffers.

1.2.8 UARTs

The MCF5216 contains three full-duplex UARTs that function independently. The three UARTs can be clocked by the system bus clock, eliminating the need for an external crystal.

1.2.9 I^2C Bus

The I^2C bus is a two-wire, bidirectional serial bus that provides a simple, efficient method of data exchange, minimizing the interconnection between devices. This bus is suitable for applications requiring occasional communications over a short distance between many devices.

1.2.10 QSPI

The queued serial peripheral interface module provides a synchronous serial peripheral interface with queued transfer capability. It allows up to 16 transfers to be queued at once, eliminating CPU intervention between transfers.

1.2.11 QADC

The QADC is a 10-bit, unipolar, successive approximation converter. A maximum of 8 analog input channels can be supported using internal multiplexing. A maximum of 18 input channels can be supported in the internal/external multiplexed mode.

The QADC consists of an analog front-end and a digital control subsystem. The analog section includes input pins, an analog multiplexer, and sample and hold analog circuits. The analog conversion is performed by the digital-to-analog converter (DAC) resistor-capacitor array and a high-gain comparator.

The digital control section contains queue control logic to sequence the conversion process and interrupt generation logic. Also included are the periodic/interval timer, control and status registers, the 64-entry conversion command word (CCW) table, and the 64-entry result table.

1.2.12 DMA Timers (DTIM0-DTIM3)

There are four independent, DMA-transfer-generating 32-bit timers (DTIM0, DTIM1, DTIM2, DTIM3) on the MCF5216. Each timer module incorporates a 32-bit timer with a separate register set for configuration and control. The timers can be configured to operate from the system clock or from an external clock source using one of the DTINx signals. If the system clock is selected, it can be divided by 16 or 1. The input clock is further divided by a user-programmable 8-bit prescaler which clocks the actual timer counter register (TCRn). Each of these timers can be configured for input capture or reference compare mode. By configuring the internal registers, each timer may be configured to assert an external signal, generate an interrupt on a particular event or cause a DMA transfer.

1.2.13 General Purpose Timers (GPTA/GPTB)

The two general purpose timers (GPTA and GPTB) are 4-channel timer modules. Each timer consists of a 16-bit programmable counter driven by a 7-stage programmable prescaler. Each of the four channels for each timer can be configured for input capture or output compare. Additionally, one of the channels, channel 3, can be configured as a pulse accumulator.

A timer overflow function allows software to extend the timing capability of the system beyond the 16-bit range of the counter. The input capture and output compare functions allow simultaneous input waveform measurements and output waveform generation. The input capture function can capture the time of a selected transition edge. The output compare function can generate output waveforms and timer software delays. The 16-bit pulse accumulator can operate as a simple event counter or a gated time accumulator.

1.2.14 Periodic Interrupt Timers (PIT0-PIT3)

The four periodic interrupt timers (PIT0, PIT1, PIT2, PIT3) are 16-bit timers that provide precise interrupts at regular intervals with minimal processor intervention. Each timer can either count down from the value written in its PIT modulus register, or it can be a free-running down-counter.

1.2.15 Software Watchdog Timer

The watchdog timer is a 16-bit timer that facilitates recovery from runaway code. The watchdog counter is a free-running down-counter that generates a reset on underflow. To prevent a reset, software must periodically restart the countdown.

1.2.16 Phase Locked Loop (PLL)

The clock module contains a crystal oscillator (OSC), phase-locked loop (PLL), reduced frequency divider (RFD), status/control registers, and control logic. To improve noise immunity, the PLL and OSC have their own power supply inputs, VDDPLL and VSSPLL. All other circuits are powered by the normal supply pins, VDD and VSS.

1.2.17 Interrupt Controllers (INTC0/INTC1)

There are two interrupt controllers on the MCF5216, each of which can support up to 63 interrupt sources each for a total of 126. Each interrupt controller is organized as 7 levels with 9 interrupt sources per level. Each interrupt source has a unique interrupt vector, and 56 of the 63 sources of a given controller provide a programmable level [1-7] and priority within the level.

1.2.18 DMA Controller

The Direct Memory Access (DMA) Controller Module provides an efficient way to move blocks of data with minimal processor interaction. The DMA module provides four channels (DMA0-DMA3) that allow byte, word, longword or 16-byte burst line transfers. These transfers are triggered by software explicitly setting a DCRn[START] bit or the occurrence of a capture event or an output reference event in the corresponding DMA timer (DTIM0-DTIM3) for each channel. The DMA controller supports single or dual address to off-chip devices or dual address to on-chip devices.

1.2.19 External Bus Interface Module (EBI)

The external bus interface handles the transfer of information between the internal core and memory, peripherals, or other processing elements in the external address space.

Programmable chip-select outputs provide signals to enable external memory and peripheral circuits, providing all handshaking and timing signals for automatic wait-state insertion and data bus sizing.

Base memory address and block size are programmable, with some restrictions. For example, the starting address must be on a boundary that is a multiple of the block size. Each chip select can be configured to provide read and write enable signals suitable for use with most popular static RAMs and peripherals. Data

bus width (8-bit, 16-bit, or 32-bit) is programmable on all chip selects, and further decoding is available for protection from user mode access or read-only access.

1.2.20 SDRAM Controller

The SDRAM controller provides all required signals for glueless interfacing to a variety of JEDEC-compliant SDRAM devices. SRAS/SCAS address multiplexing is software configurable for different page sizes. To maintain refresh capability without conflicting with concurrent accesses on the address and data buses, $\overline{\text{SRAS}}$, $\overline{\text{SCAS}}$, $\overline{\text{SDWE}}$, $\overline{\text{RAS}}$[1:0] and SCKE are dedicated SDRAM signals.

1.2.21 Reset

The reset controller is provided to determine the cause of reset, assert the appropriate reset signals to the system, and keep track of what caused the last reset. The power management registers for the internal low-voltage detect (LVD) circuit are implemented in the reset module. There are seven sources of reset:

- External
- Power-on reset (POR)
- Watchdog timer
- Phase locked-loop (PLL) loss of lock
- PLL loss of clock
- Software
- Low-voltage detection (LVD) reset

External reset on the $\overline{\text{RSTOUT}}$ pin is software-assertable independent of chip reset state. There are also software-readable status flags indicating the cause of the last reset, and LVD control and status bits for setup and use of LVD reset or interrupt.

1.2.22 GPIO

All of the pins associated with the external bus interface may be used for several different functions. Their primary function is to provide an external memory interface to access off-chip resources. When not used this, all of the pins may be used as general-purpose digital I/O pins. In some cases, the pin function is set by the operating mode, and the alternate pin functions are not supported.

The digital I/O pins on the MCF5216 are grouped into 8-bit ports. Some ports do not use all eight bits. Each port has registers that configure, monitor, and control the port pins.

1.3 Development Tools

For an up-to-date list of development tools for the MCF5216, see the MCF5216 product page at the Freescale web site: http://www.freescale.com/coldfire.

1.4 Documentation

Documentation is available from a local Freescale distributor, a Freescale sales office, the Freescale Literature Distribution Center, or through the Freescale world-wide web address at http://www.freescale.com/coldfire.

1.5 Document Revision History

Table 1 provides a revision history for this hardware specification.

Table 1. Document Revision History

Rev. No.	Substantive Change(s)
0	Initial release
1	Removed Preliminary text. Replaced instances of Motorola with Freescale. Replaced documentation and development tools tables with a link to the Freescale web site as it has the most up-to-date list of available documentation and tools.

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